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PROGRAMMABLE FILTER FOR ULTRASONIC NDE SYSTEMS

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ABSTRACT

Transversal filters based on the charge-coupled device (CCD) technology may be applied to processing received signals in an ultrasonic NDE system. Filters having a fixed response (fixed tap weightings) could be used to compensate for the characteristics of a given ultrasonic transducer. A more flexible arrangement allowing programmability employs a CCD delay line whose tap electrodes are accessible externally for weighting. The response of this device can be altered by changing a set of resistors mounted on a printed circuit board which can be plugged into a socket connected to the CCD. Proper response for a given ultrasonic transducer is obtained by plugging in the proper circuit board. Because present commercial CCD's allowing programmability have clock frequencies too low for direct processing of ultrasonic NDE signals, the filter is preceded by a CCD video delay line which quickly stores the return signal and then outputs it more slowly for processing during the time between successive excitations of the ultrasonic transducer.

Burst Processor System

The filter system that has been designed and constructed is illustrated schematically in Fig. 1. The signal from the NDE ultrasonic transducer is input to the "Analog Data Acquisition System" which consists of the Fairchild CCD321 analog shift register, a driver circuit board, and the necessary integrated circuitry to generate charge-transfer clocks of the desired frequencies. The NDE transducer signal is sampled at a high rate and stored in the CCD video delay line while the fast clock is supplied to the line. After storage, the clock generator drops to a lower rate and the stored signal is clocked out of the delay line and into the CCD transversal filter whose charge transfer is at the slow clock rate. As shown in the timing diagram at the bottom of Fig. 1, this entire sequence occurs between successive excitations of the ultrasonic system.

Analog Data Acquisition System - The heart of this system is the Fairchild 321 CCD analog shift register. This device was designed for the storage of 455 or 910 samples representing a line of a television picture. The device can accept clock inputs at up to 20 MHz; because of the rather demanding requirements on the clock signals (17 volts with about 10 ns rise and fall times for transfer, as short as 5 ns rise and fall for sample voltages) we purchased the complete Fairchild 321M module containing CCD and driver circuitry. A locally-designed circuit board was built for generation of the clock signals and the various required timing signals (see Fig. 2). This circuitry utilizes a 20 MHz crystal as its master clock and provides that frequency to the 321M as the fast clock signal. Dividers produce the slow clock signal which we chose as 100 kHz allowing for a division by two on the circuit board of the CCD transversal filter (in other words, the actual transfer frequency in the transversal filter is 50 kHz, or the time per transfer there is 20 microseconds). Thus about 500 signal samples could be processed between excitations of a typical NDE system operating at 1000 pulses per second.

The sampling/storing/readout-out cycle is illustrated in Fig. 3 with high frequency sawtooth waveforms at fundamental frequencies of 1, 2.5, and 5 MHz respectively (top to bottom). The samples read out at the low rate are clearly seen in the major part of the photograph; input sampling occurred during the first 7% of the trace, at the far left where the waveform is blurred. On the bottom trace of Fig. 3 one sees the loss of detail—loss of the higher frequency components—as the fundamental frequency is raised and the sampling theorem dictates increasingly poorer fidelity of the sampled representation of the waveform.

When we first operated the data acquisition system in the burst mode, we found unexpected signals appearing in the output. The signals are apparent in Fig. 4, an oscilloscope display of the output when a sawtooth waveform is input to the video delay line circuit. One notices, in addition to the samples' waveform (which appears smooth here because of the large number of samples per cycle of the sawtooth), eight samples which are displaced from the sawtooth and appear as isolated dots in the figure. Eventually, the following was learned about the origin and treatment of this affliction of the CCD video delay line: The voltage spikes are caused by the different structure of the CCD circuit on its silicon chip at the points where the charge-transfer path turns corners. The CCD321 is being redesigned by Fairchild engineers to correct this problem and a new device is expected to be available within a few months. The spikes do not appear if the clock rate is not changed, and so the phenomenon was not noticed early in development and distribution of the CCD321 because burst processor use was not examined. The amount of added charge producing the corner-turning spikes is roughly proportional to the amount the clocking frequency is changed. The spike amplitude can be reduced (from the 0.5 volt observed here) by carefully maintaining proper time relations between the newly initiated transfer clock and the sampling waveforms; an "enable" terminal and circuitry for synchronization exists on the
Even with the use of the enable synchronizing circuit the spikes are large enough to interfere with samples' waveforms, so the new CC0321 device will be welcomed. Further, use of the enable circuit prevents one from using multiplexed operation of the CCD321. When it can be used, multiplexed operation provides an effective doubling of the clock frequency for transfer in the video delay line; waveform samples are taken on each phase (+ and -) of the input clock, and alternate samples progress through two independent charge-transfer lines to be "interleaved" to form the output. (The multiplexed output is also relatively free of the large clock spikes which appear on the outputs of the two independent lines themselves.)

It is hoped that the redesign of the CCD321 itself and modification of its driver circuitry can permit burst operation in the multiplexed mode without the interfering spikes. In such a mode, operation with an effective clock frequency of 40 MHz and signal bandwidth approaching half that would be possible.

Experiments

The Analog Data Acquisition System is shown in Fig. 5. The device can be operated in a free-running mode or it can be operated in a triggered burst mode from either a remote or an internally-supplied local trigger signal. The real view of the instrument is included as it suggests some of the flexibility of the system. The A and B channels can be used independently or their inputs may be paralleled for multiplex ("mux") operation. Inputs are provided for A and B channels with signals no greater than one volt; otherwise the protected signal inputs (such as "a signal in") are used, though they are slightly less desirable because of a 4:1 signal amplitude decrease caused by the voltage divider in the protective circuitry.

The transversal filter having switches and adjustable resistors for tap weighting is shown in Fig. 6. The TAD32 is the large integrated circuit in the center of the circuit board. Most tests were made with this circuit.

Figure 7 shows a transversal filter circuit designed to use tap weighting supplied by resistors on small circuit boards (Fig. 8). The TAD32 is on one side of the 4 inch x 8 inch circuit board; weighting networks plug into a 40-pin zero-insertion-force socket on the opposite side of the board. Figure 9 shows a view of the entire setup.

The tap weights are related to the reference reflection waveform. For example, if one wanted to make a matched filter using the transversal filter, one would weight taps so that the transversal filter had an impulse response which was the time reverse of the reference waveform. Thus for the matched filter one might take sample values of the reference function (for example, using an oscilloscope display, or a digital voltmeter and a sample-and-hold circuit on the output of the data acquisition system), reverse the order of the sample values, and set tap weights proportional to those values. Figure 10 shows the reference waveform output from the data acquisition system and the output of a transversal filter, matched to this function, when the reference signal is fed into it.

To obtain the tap weights for an inverse filter (previously when using a SAW implementation we obtained the reference waveform), we took its frequency spectrum, inverted and weighted it with a windowing function, and then computed the impulse response of the filter to be fabricated. In a SAW filter there is a simple correspondence between the impulse response and the placement and length of each transducer electrode; hence it was relatively simple to design the SAW transversal filter from the impulse response.

With the CCD approach to transversal filtering, we at first employed different approaches--based on computer programs which yielded tap weights to achieve a given frequency response with a given optimized error. When we tested filters having tap weights adjusted to the computed values we found they did not yield improvement comparable to that seen with the SAW filter. We now believe this is either because phase information was necessarily lost in the process (owing to the nature of the programs used), or because the design responses were not closely enough approximated by the optimized responses. These suppositions can be checked with more computer experiments, but a more fruitful avenue appears to be to design the CCD transversal filter directly from the impulse response itself (rather than from the frequency response) as was done with the SAW filters.

The reasoning behind this statement is that any filter which has an impulse closely similar to the design impulse response must perform the deconvolution correctly and, hence, produce the desired improvement of spatial resolution. With the CCD taps we have full freedom in weighting, but no freedom in the placement of taps along the delay line; taps will be equally spaced along the line because the manufacturer put them there. We noticed earlier that the impulse response "called for" some unequal spacings in the SAW electrodes, and so we would expect to be able to approximate such an impulse response with the CCD only by "sampling" the impulse response somewhat densely with CCD taps (for example, with four taps per cycle of the waveform).

Remedies which should enable one to obtain a close approximation to the design impulse response are: (a) using two TAD32 devices in series (they are designed to operate in this fashion), and (b) "reconstituting" the slowed-down signal as it is clocked slowly out of the acquisition system by lowpass filter (eliminates the clock frequency components) and sample it at a suitable rate by the TAD32 circuits driven with a clock whose frequency can be varied this way a sufficient number of cycles of the impulse response could be sampled with CCD taps, whereas now at a given instant each tap of the TAD32 is responding to only a single sample of the ultrasonic return signal from the acquisition system sampler. Even though the constraints of the sampling theorem
are being observed with regard to the input signal sampling in the acquisition system, the sampling of the desired impulse response for tap weighting is too sparse for an adequate representation. However, there appear to be no fundamental limitations which will prevent the fabrication of a programmable filter which will provide improved spatial resolution in ultrasonic test signals and which will provide a way to help "normalize" ultrasonic test procedures.

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Figure 1. Burst processor system. (Top) Block diagram showing arrangement of analog data acquisition system which samples signal from NDE transducer using the fast clock from the variable rate clock generator. After acquisition, the clock generator frequency drops and lower frequency clock is supplied to the CCD video delay line, clocking out the stored samples slowly, and to the CCD transversal filter, whose output is slowed and filtered version of the signal input. (Bottom) Timing diagram for burst processor system.
Figure 2. Schematic diagram of the circuit board supplying clock signals to the video delay line and the transversal filter.

Figure 3. Display of sawtooth waveforms (fundamental frequencies 1, 2.5, and 5 MHz) sampled and then slowly clocked out of video delay line. (Horizontal scale 50 microseconds/major division.)

Figure 4. Output of the data acquisition system showing "corner-turning-spikes" which result when the clock rate is changed substantially (being corrected by the manufacturer).

Figure 5. Front and rear views of analog data acquisition system.
Figure 6. Transversal filter employing switches and variable resistors to adjust tap weights (built by Frederick Pack).

Figure 7. CCD transversal filter employing interchangeable weighting networks to change response. (a) 4 inch x 8 inch circuit board showing clock and signal inputs on left, TAD32 in center, output at right. (b) Rear of board showing zero-insertion-force socket which accepts plug-in weighting network board.

Figure 8. Top (right) and bottom (left) views of plug-in weighting network.

Figure 9. Photograph of burst processor system. From left to right are: power supply for transversal filter; transversal filter with switches and resistors; analog data acquisition system (with amplifier on top of it); pulse generators for adjusting triggering of ultrasonic system and oscilloscope; test block with its transducer; commercial (Panametrics) pulser/receiver/oscilloscope.

Figure 10. (Top) Output of analog data acquisition system when reference reflection waveform at around 5 MHz is input. (Bottom) Output of CCD transversal filter when taps are set for matched filter operation (filter matched to upper waveform) and reference function is input. (Horizontal scale 50 microseconds/major division.)