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A low voltage rail-to-rail operational amplifier with constant operation and improved process robustness

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A low voltage rail-to-rail operational amplifier with constant operation and improved process

robustness

by

Rien Beal

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ABSTRACT

An operational amplifier is one of the most basic components in analog, mixed-signal, RF, and other integrated circuit designs. Low voltage and low power operational amplifier design has become an increasingly interesting subject as many applications switch to portable battery powered operations. The need for design techniques to allow amplifiers to maintain an acceptable level of performance when the supply voltages are decreased is immense. One of the most important features in low voltage amplifier designs is ensuring that the amplifier maintains constant behavior in the presence of rail-to-rail input common-mode variations while providing a rail-to-rail output to maximize signal-to-noise ratio. In this work a new rail-to-rail low voltage operational amplifier is designed, simulated, and compared against state of the art amplifier designs. The amplifier architecture aims at achieving constant amplifier operation over a rail-to-rail common-mode input voltage range. The concept of constant operation refers to the ability to maintain constant specifications such as gain, gain-bandwidth product, phase margin, slew rate, and power consumption against large variations in input common-mode voltage. The amplifier is additionally designed to be robust with respect to variations in process parameters, supply voltages, and operating temperatures (PVT). A final evaluation of the performance of the proposed design versus that of the state of the art in the open literature is carried out. The intended capabilities and advantages of the new design are verified through extensive simulation.

CHAPTER 1. INTRODUCTION AND GENERAL LITERATURE REVIEW

1.1 Introduction

An operational amplifier is one of the most commonly used components in analog and digital circuit designs. It is found in applications such as communications transmitters and receivers, medical devices, and multimedia electronics. In each of these applications, the need for low voltage low power amplifiers has steadily increased as many devices shift toward portable and battery powered operations. It is the main goal in low power amplifier designs to maintain an acceptable level of performance as supply voltages continue to drop for these applications. In general, for CMOS VLSI technology, as the supply voltage and current decrease, the performance of the transistor degrades. This degradation necessitates research and exploration for low voltage and low power design techniques to compensate for the loss in performance due to reductions in supply voltages and currents.

As the supply voltage and current of an analog circuit decrease there are certain performance measures of the circuit which will suffer a loss in performance. For example, for lower supply voltages the signal to noise ratio of the circuit will decrease, as the maximum input and output signal for the circuit will be smaller. Also the achievable bandwidth will be reduced as the supply voltage and total current are reduced. Less headroom tends to be available when the supply voltages are reduced. A reduction in headroom removes the possibility of using cascoded or stacked devices to increase the output

impedance. In terms of the minimum usable supply voltage, it is required that the following expression is satisfied, $V_{DD} > V_{signal\_swing} + K*V_{Dsat}$, where V_{Dsat} is the minimum transistor saturation voltage, V_{signal_swing} is the signal swing of the circuit, and K represents the number of transistors stacked in series. Thus, as the supply voltage decreases, the largest possible value of K will also decrease, which implies cascoding may become difficult or impractical.

Each of the previous noted issues described will apply to all low voltage designs and should be considered at the design level; however there are more exclusive specifications which apply particularly to amplifier designs that will suffer as a result of reduced supply voltages. This includes such characteristics as DC gain, gain-bandwidth product, phase margin, and power consumption. In order to create a design in which these performance parameters do not degrade at low voltage, the cause of performance degradation must first be studied. The questions then become, what is the optimal amplifier implementation to compensate for the effects of low voltage and low power application? What are the main issues that trouble low voltage amplifier designs and how can they be overcome with minimal additional circuitry? Each of these questions serves as the motivation for this work and will be explored in more detail.

1.2 Amplifier Characterization

There are several performance measures used to characterize all amplifiers. Some of the most commonly observed characteristics include the DC gain (A_{VO}), gain-bandwidth product (GBW), phase-margin (PM), and power consumption. Other performance

specifications used to characterize amplifiers include slew-rate, common-mode rejection ratio (CMRR), power supply rejection ratio (PSRR), total harmonic distortion (THD), and the input noise voltage.

At low voltages each of these performance measures becomes more sensitive to the design of the amplifier and characteristics of the process. The theoretical limit of the minimum voltage that can be used to operate an amplifier is limited by the threshold voltages, which are characteristic of the process. Smaller feature size processes can be used (which have a lower threshold voltage) to achieve lower voltage operations. However, with smaller feature size processes, it becomes more difficult to optimize the performance measures mentioned above. In order to understand how an amplifier's performance measures are affected by low voltage implementation, it is important to first define each performance measure and explore which transistor parameters have the greatest affect on them.

The DC gain of an amplifier is one of the most commonly used performance measures. It is typically preferable for an operational amplifier to have a large DC gain, which will allow for better closed loop performance. The DC gain is the open loop gain from input to output of an amplifier at low frequencies. The DC gain of an amplifier mostly depends on the transconductance gain (g_m) of the input pair and the output conductance (g_o) of the amplifier. The transconductance gain expression is given by (1.1), where m is the mobility of the material, Cox is the gate oxide capacitance, W and L are the width and length of the transistor respectively, and I_{DQ} is the transistor quiescent current. Similarly, the output

conductance of a single transistor is given by (1.2), where l is the channel length modulation

factor, V_{GS} is the gate source voltage, and V_T is the threshold voltage. It is seen from (1.1)

and (1.2) that the DC gain of an amplifier will have several process dependent terms, namely

m, l, and Cox. This implies that there are physical limitations due to the process when

designing for a particular DC gain. Also it is observed that as these process variables vary

randomly, the DC gain will be affected as a result.

$$g_m = \sqrt{2 \cdot \mu C_{ox} \frac{W}{L} \cdot I_{DQ}} \qquad (1.1)$$

$$g_o = \lambda \left(\frac{1}{2} \mu C_{ox} (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS}) \right) \qquad (1.2)$$

The gain-bandwidth product is also an important performance measure for all

operational amplifiers. The GBW typically gives an indication of the relative speed of the

amplifier. The GBW is given by the product of the DC gain and the bandwidth of the

amplifier as the name suggest. The GBW often is compared to the unity gain frequency as

these two values are usually in the same range. It is also desired to have an amplifier with a

high GBW, which allows the amplifier to operate at higher speeds. The GBW is highly

dependent on the capacitive load (C_L) that is present at the output as well as the

transconductance gain of input stage. For multi-stage designs the GBW may also be limited

by the compensation capacitor, however the transconductance gain remains a factor for this

performance measure. As previously stated, g_m has several process dependent terms and hence the GBW can also be affected by variations in process terms.

The phase-margin is a parameter that is used to determine the stability of an amplifier in closed-loop applications. It is typically desired to have a phase margin greater than 45° at the open loop unity gain frequency, which implies that there is 45 degrees of phase above a -180° phase delay. The phase margin of an amplifier is mostly dependent on the separation of the dominate poles of the system. For a multistage design this is controlled by the use of a compensation capacitor. However the gain and the bandwidth of an amplifier will affect the phase margin significantly. For higher gains a large pole separation is necessary to achieve an acceptable phase margin. Also, the bandwidth gives an indication of what frequency the dominate pole lies and gives a hint about where the second dominate pole should be placed for the amplifier to be considered stable. Thus it is seen that as the gain and bandwidth of an amplifier change, the requirements for compensation to guarantee stability are also altered.

The power consumption of an amplifier is simply the amount of power the amplifier dissipates. The power consumption directly limits the maximum achievable GBW of the amplifier. Thus the GBW that will be observed is relative to the power which is consumed in the amplifier. When designing an amplifier, typically the power consumption is fixed and it is the goal of the design to maximize GBW based on this specification.

For the amplifier specifications mentioned it is important to understand how these specifications should be designed at low voltages. As stated previously, at low voltages the

signal to noise ratio of an amplifier is reduced as the maximum input signal is smaller. This

induces the need for rail-to-rail operations at low voltages. This implies that each of the

amplifier's performance measures are kept relatively constant for common-mode values

ranging from the negative supply (V_{ss}) to the positive supply (V_{dd}). This allows for the input

signal to be as large as possible, thus maximizing the signal to noise ratio. For low voltage

amplifiers it is also necessary to obtain rail-to-rail differential outputs to maximize the signal

to noise ratio.

In order to achieve a rail-to-rail operation, it is necessary to hold each of the

amplifier's performances measures constant across the entire common-mode range. If the

amplifier specifications are not held constant, the amplifier will exhibit an undesirable

variation in performance as the common-mode changes. For example if the DC gain of an

amplifier is different across the common-mode range, the phase margin of the amplifier will

also vary. This can cause the amplifier to either become undercompensated/unstable or

become overcompensated at a particular common-mode level. The same argument follows

for the GBW.

As previously mentioned, the DC gain as well as the GBW highly depends on the

input g_m and the output g_o of the amplifier. This implies that for low voltage amplifier

designs, it is of interest to keep g_m and g_o constant for the entire common-mode range in

order to obtain a constant DC gain and GBW. There has been much work in creating design

techniques to keep g_m as constant as possible [1-15]. Less work has been explored to keep g_o

constant, however it is an important topic when trying to design a rail-to-rail input/output

amplifier in terms of maintaining a more constant DC gain. Exploring methods for keeping g_o constant also gives way to implementing commonly used gain boosting techniques for low voltage designs.

1.3 General Literature Review

Research indicates that major performance measures such as DC gain, GBW, and PM of an amplifier are greatly influenced by the design of the input stage [1-15]. Because of this, there has been much focus on the optimal design of the input stage to keep these performance measures constant across the common-mode range. Most of the focus has shifted towards the argument of keeping g_m constant, but the overall intent is to obtain a constant operation for all amplifier specifications. Many designs use the same architecture, but make changes to the input stage to obtain a rail-to-rail input stage and constant operation.

A commonly used architecture for low voltage amplifier designs is a folded cascode amplifier. This architecture is used because it maximizes the ability to manipulate the input stage to achieve the rail-to-rail operation that is desired in low voltage design. A commonly used technique for the input stage is the implementation of a complementary input pair. This means that the input consists of an n-ch input pair as well as a p-ch input pair. Implementing this technique insures that at least one input pair is operating when the common-mode shifts near the supply rails. However, the use of complementary input pairs does not insure that there will be a constant operation across the common-mode range. Additional measures must be taken to insure constant operation, which will be explored in more detail in the following section.

To achieve a rail-to-rail output for a low voltage amplifier, it is typical to implement a class-AB output stage. A class-AB output stage allows for the transient output signal to swing relatively close to the supply rails as the transient current may be varied with the input signal. This technique is also often referred to as a push-pull stage because the class-AB output stage typically is made up of a set of p-ch and n-ch transistors where each transistor will conduct and amplify the signal for half of the waveform. This implementation is commonly used, however many different variation of class-AB output stages exist. In the following section a more detailed review of current low voltage amplifier design techniques used to obtain constant operations will be explored.

The structure of this thesis is organized as followed. Chapter 2 discusses previous work that has been presented pertaining to low voltage rail-to-rail amplifiers. Also a top level proposal of the design presented in this work is discussed in Chapter 2. Chapter 3 follows with a presentation of the new architecture. An analysis as well as the design procedures of the architecture is given. Chapter 4 presents the simulation results of the design and proves that the desired performance is indeed achieved. A comparison of the performance of this work's amplifier design and of others is also explored. Chapter 5 then gives a brief discussion of the overall design. This discussion includes design limitations and issues that arose during the design process.

In this thesis there is also a supplementary section found in Chapter 6 which includes additional research performed. However this material does not directly relate to the work seen in Chapters 1 – 5. Chapter 6 discusses a new DAC architecture which was attempted

and implemented unsuccessfully. The results and complications correlated with this design

are presented and analyzed.

CHAPTER 2. LITERARY REVIEW AND DESIGN PROPOSAL

2.1 Introduction

For low voltage amplifier design it is necessary to have rail-to-rail input/output operations to insure a maximum signal to noise ratio. There have been a number of works that have explored how to achieve a rail-to-rail behavior through proper input and output-stage designs. Rail-to-rail input techniques mainly revolve around the idea of maintaining a constant input g_m across the full common-mode range. To achieve rail-to-rail outputs, typically a class-AB output-stage is implemented. However, many different implementations exist for obtaining rail-to-rail input/outputs, each of which have their own advantages and disadvantages.

2.2 Amplifier Implementations

Specific techniques to maintain a nearly constant g_m over the entire V_{icm} have been reported in [1-15], most of which use an n-ch and p-ch complementary input differential pair. This implementation has some limitations because at the center of the V_{icm}, the total g_m will nearly double in value when the V_{icm} is closer to either of the supply rails as seen in Figure 2-1. This is due to the fact that there exists a large overlap region where both complementary pairs are active. The disadvantage of this overlapping regions is a variable DC gain, GBW, a non-constant slew rate, and non-optimal frequency compensation [2, 4, 9, 12-14] result.
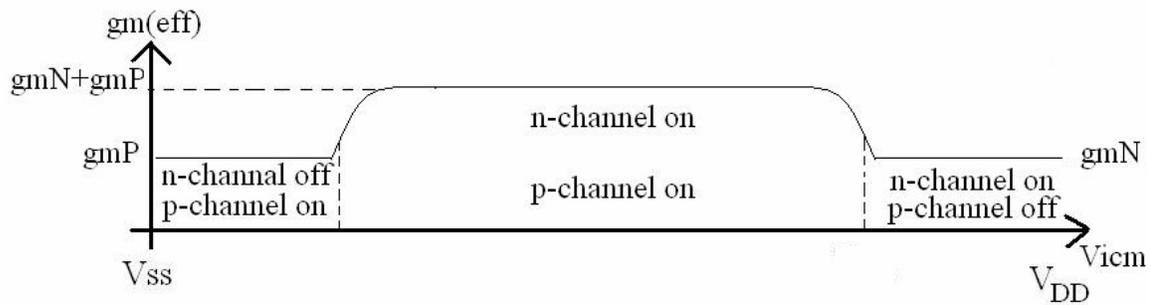
Figure 2-1 Complementary input gm variation

One method used to stabilize g_m across the entire V_{icm} when using an n-ch and p-ch complementary input pair is to employ current switches to increase and decrease the tail current. When V_{icm} is near either supply rail, the tail current is increased to 4 times the tail current compared to when V_{icm} is in the mid-range. This effectively gives a relatively constant g_m for the full V_{icm}. The reasoning for using 4 times the tail current to stabilize g_m becomes obvious after observing equation (1.1). In (1.1) it is seen that g_m is proportional to the square-root of the current I_{DQ}. Since at the center of the V_{icm}, g_m is doubled due to the two active pairs, in order to double g_m with a single active pair, 4 times the current is needed. Thus, for this method the tail current is increased to $4*I_{DQ}$ at V_{icm} near each of the supply rails (when a single input pair is active) and then decreased to I_{DQ} at the center of V_{icm} (when both pairs are active). This effectively creates a constant gm for the entire common-mode range which is depicted in Figure 2-2.
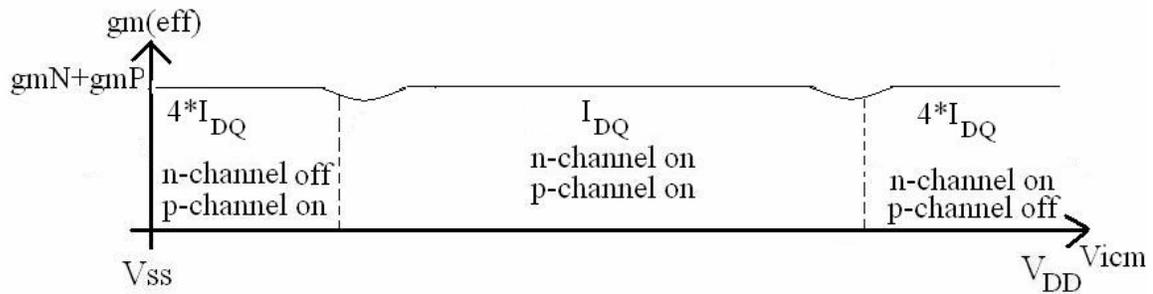
Figure 2-2. gm variation with switching tail current

Another method recently developed to stabilize g_m includes using level shifting [5]. Using this method, the transition region of the p-ch input pair is shifted up by DC level shifters to overlap with the n-ch pair. Two p-ch source followers were used as DC level shifters. Also, a less conventional approach to keep g_m constant has been explored using level shifters. In [9] instead of using a p-ch and n-ch complementary pair, a dual set of n-ch input transistors are used. The DC level shifter is attached to a single input pair to shift the common mode up such that the input pair remains active near the negative supply. A similar technique is explored in [13, 14].

It is stated in [12] that several guidelines should be followed for implementing a constant g_m circuits. First, the large-signal and small-signal performances should be kept constant irrespective of changes in the common-mode. Second, the accuracy of the techniques should not depend on a specific model or strict match requirements. This implies that the implementation is universal and robust. Third, the circuit should allow high frequency operations and consume minimal power. Last, the complexity should be sensible

[12]. A more in depth analysis of [5, 7, 9, 14, 15] will reveal how well these designs match up with these requirements and will identify possible limitations of the designs.

2.2.1 Complementary Input Pair Implementation

In [7] an implementation of a complementary n-ch and p-ch input pair to achieve a rail-to-rail input is presented. In order to maintain a constant g_m across the V_{icm} range, a g_m-control circuit is implemented. As indicated in [7], without a g_m-control circuit the input transconductance is a factor of two larger at the center of the common-mode. Therefore, the bandwidth also changes by a factor of two, changing the requirements for optimal compensation. It is first proposed that the g_m-control can be implemented by regulating the sum of the gate-source voltages of the two input pairs by using an electronic implementation of a zenor diode. However, it is suggested that this would require a complex feedback loop and for this reason is not discussed in more detail. A simpler g_m-control is presented which uses a feed-forward method of control by applying current switches. This is seen in Figure 2-3.

Figure 2-3. Complementary Input Stage with Current Switches (modified) [7]

In Figure 2-3 the bias current through $M_1 - M_4$ is controlled by $M_5 - M_8$. In the middle of the common-mode input voltage range, part of the bias current through the pMOS pair M_1, M_3 is removed by the current switches M_5, M_7 [7]. At the same time switches M_6, M_8 remove a portion of the current from the input pair M_2, M_4. When the common-mode input is high, the nMOS inputs will be turned on and the pMOS inputs will be turned off, while all of the bias current of the pMOS input pair will flow through M_5, M_7. Similarly, when the common-mode input is low, the pMOS input pair will be active and the nMOS input pair will be off, while the bias current of the nMOS input pair will flow through M_6, M_8. The main purpose of the current switches $M_5 - M_8$ is to limit the current through the input pair in the middle of the common-mode range. When the common-mode input voltage is equal to V_{B2}, the current through each input pair should be half of the value in comparison to when the common-mode is near the supply rails. This implies that three-fourths of the

current flows through the current switches, which is achieved by proper sizing. This

effectively reduces the total current in the input pair for the mid range common-mode input

voltages by a factor of four, and thus keeps the total g_m constant [7].

$$V_{AB} = V_{DD} - V_{SS} - V_{GSP} - V_{GSN} \tag{2.1}$$

The basic implementation of the class-AB output stage from [7] can be seen in Figure

2-4. The class-AB is in principle represented by the voltage source V_{AB}. To set the

quiescent current, the sum of the gate source voltages of the output pair can be controlled in

such a way that it is equal to the sum of the reference pMOS and nMOS gate source voltage

V_{GSP} and $V_{GSN;}$ respectively. This is obtained by setting V_{AB} as seen in (2.1) [7]. This allows

for rail-to-rail output swings making full use of the supply voltage.
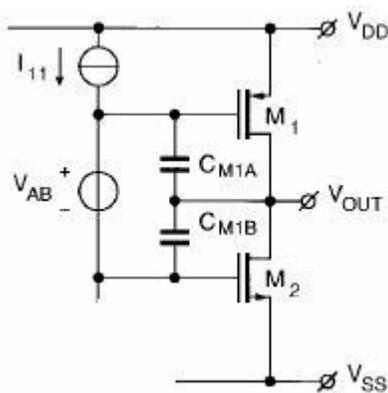
Figure 2-4. Class-AB Output Stage (modified) [7]

There were a few design limitation that were observed in [7]. As previously stated, for a good constant g_m circuit, it is desirable that the accuracy of the techniques should not depend on a specific model or strict match requirements. It is observed in [7] that this is not the case. The use of complementary input pairs suggest that there should be some level of matching between the n-ch input pair and the p-ch input pair. Also the use of the current switches implies that a specific model is assumed to keep g_m constant. As mentioned above, the tail current is varied by a factor of four to effectively keep the value of g_m constant across the common-mode range. This was derived from (1.1) which assumes the square-law model for the input pairs. This model may have some inaccuracies at the fabrication level, which is observed in the results of [7]. The g_m variation differs by 5% from simulation to fabrication. The likely cause of this difference may be due to the dependence of a particular model and matching to keep g_m constant.

It is also observed that the offset voltage of the final amplifier in [7] varies with the common-mode. This is due to the fact that a different input pair will be active at different common-mode levels. It is reported that there is an offset variation of approximately 8mV, which consequently increased the total harmonic distortion. These are the main limitations to this design, which mainly depend on the input stage. There have been many architectures developed since [7] was published, each of which try to improve on its limitations.

2.2.2 Complementary Input Pair with Dummy Input Implementation

A slightly different implementation for a rail-to-rail input stage was explored in [15]. The basic idea of using complementary n-ch and p-ch input pairs was implemented; however,

a different approach was taken to keep the input g_m constant across common-mode inputs. In this implementation the same basic idea of varying the tail current was implemented. In [15] instead of using current switches, a set of dummy input pairs was implemented. The input stage used in [15] can be seen in Figure 2-5.
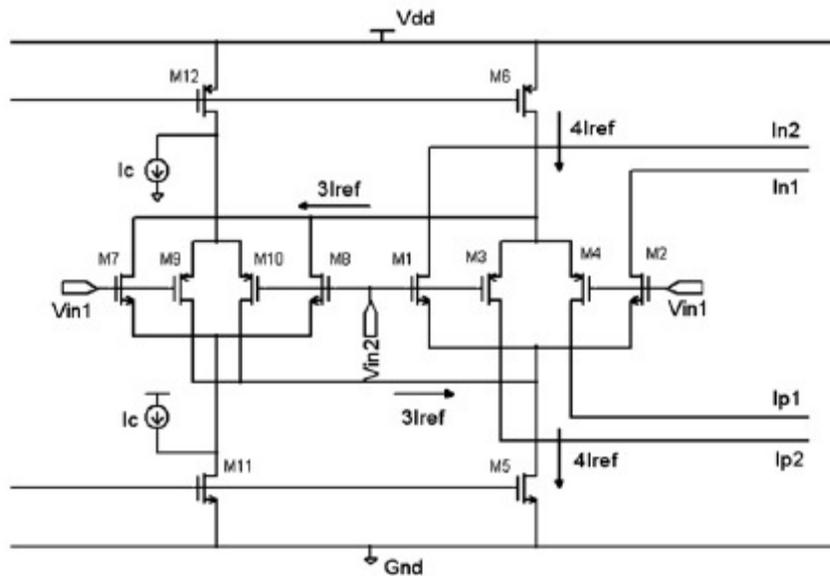
Figure 2-5. Complementary Input Stage with Dummy Pair [15]

In Figure 2-5 there is a complementary n-ch and p-ch pair as well as a dummy n-ch and p-ch pair. The dummy n-ch pair is connected to the tail current source of the p-ch input pair, and the dummy p-ch pair connects to the tail current source of the n-ch input pair. The dummy n-ch and p-ch pair serves the purpose of reducing the quiescent through the input pairs when the common-mode voltage is in the mid-range. The dummy pair will essentially have no effect when the common-mode is near the supply rails. The dummy pair consumes three-fourths of the current at the mid-range of the common-mode, just as the current

switches do in [7]. The current source I_c is used to keep M_{11} and M_{12} in the triode region when the dummy pair is turned off. This decreases the variation in g_m.

The results of [15] suggest that the variation of g_m proves to be better than that seen in [7]. However, it is observed that temperature has an impact on the constancy of g_m, which is caused by the complementary structure of the input stage. It was derived that in order to maintain a constant g_m for a complementary input pair, the sizing should follow (2.2) [15]. Any deviations from this ratio will result in variations in g_m. This limitation is observed in the results, as μ_p and μ_n will vary differently with temperature, thus offsetting the ratio seen in (2.2). The values μ_p and μ_n vary differently with temperature, due to fact that the mobility of electrons and holes responses differ with respect to temperature.

$$\frac{\mu_n}{\mu_p} = \frac{\left(\dfrac{W}{L}\right)_P}{\left(\dfrac{W}{L}\right)_N} \tag{2.2}$$

2.2.3 Complementary Input Pair with Overlapped Regions

In [5], an alternate implementation of complementary inputs to obtain a constant g_m was explored. Thus far, many papers that use complementary input pairs will vary the tail current source, to give a constant g_m. In [5] it is presented that if the transition regions of the complementary inputs are manipulated, it is no longer necessary to alter the tail current to achieve a constant g_m. As seen in Figure 2-6, the typical transition regions of a complementary input pair are usually disjoint, which employs the need to reduce the tail

current in the center of the common-mode range. As seen in Figure 2-6, there is region

where both input pairs are fully turned on. It is suggested in [5] that if the transition regions

are designed to overlap at the right point, there would be no need to compensate for the

region where both input pairs are active. This ideal overlapping region can be seen in Figure

2-7. For Figure 2-7 the p-transition region is shifted to overlap with the n-transition region.
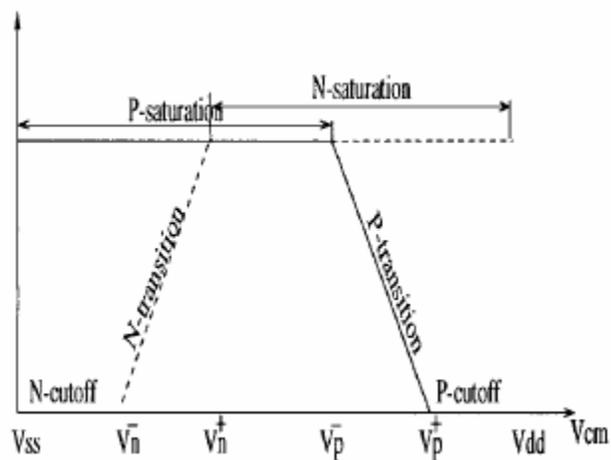
Figure 2-6. Typical Complementary Input Transition Region [5]

The proper level shift for the transition region is mathematically derived to obtain the

minimum deviation in g_m [5]. The implementation for the transition region level shift was

realized using a source follower circuit. Correct sizing and current flow through the source

follower allows for the optimal level shift of the design to be realized. A source follower was

used in this implementation because it has no effect on the slope of the transition region; it

only shifts the common-mode level so that the transition region is shifted. For the

implementation seen in [5], the transition shift is seen on the p-side; however the same

argument would also follow if this was conversely implemented on the n-side.
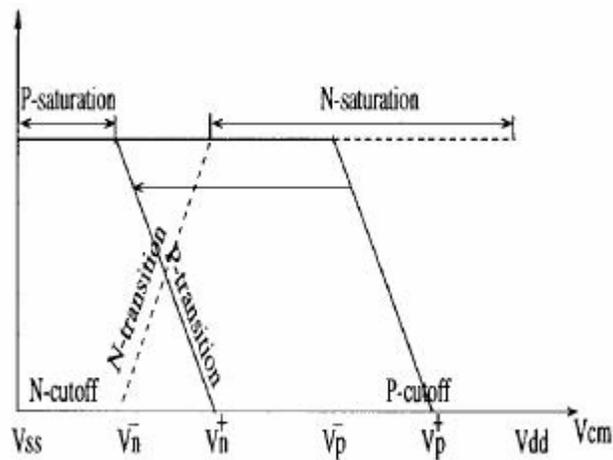
Figure 2-7. Shifted Complementary Input Transition Region [5]

The limitation that follows with this constant g_m implementation includes the error

involve when the optimal shift is not obtained. For example, if the transition regions do not

perfectly overlap after one region is shifted, this will cause variations in g_m. This problem is

an additional limitation to the ones faced by all complementary inputs. This implementation

also requires a strict matching of the n-ch and p-ch input pairs as given by (2.2). In fact, this

architecture is even more sensitive to mismatches in the input devices, as mismatches will

lead to different slopes in the transition regions. The idea of using level shifters to achieve a

rail-to-rail input was first explored in [5], however the idea has been improved upon in [9,

13, 14] to solve some of the problems seen in complementary pair input implementations.

2.2.4 Dual n-ch Input Implementation

It is presented in [9] that the use of level shifters can alleviate the need for

complementary inputs to achieve a constant g_m, for the entire V_{icm} range. It is reported that a

dual n-ch input pair can be used as opposed to a complementary input pair for rail-to-rail

inputs. This implies that the problems associated with complementary input pairs can be

overcome. As seen in [5, 7, 15] complementary inputs have the issue of strict matching

between n-ch and p-ch inputs as suggested by (2.2). Also, most implementations rely on the

square-law model to achieve a constant g_m. In [9] it is presented that these problems are no

longer troublesome with the implementation seen in Figure 2-8 because in this

implementation, the matching requirements now occur between two n-ch pairs, which can be

easily achieved. Since n-ch devices track one another as temperature and process varies, this

loosens the issues involved in matching the input devices which are seen in [5, 7, 15].
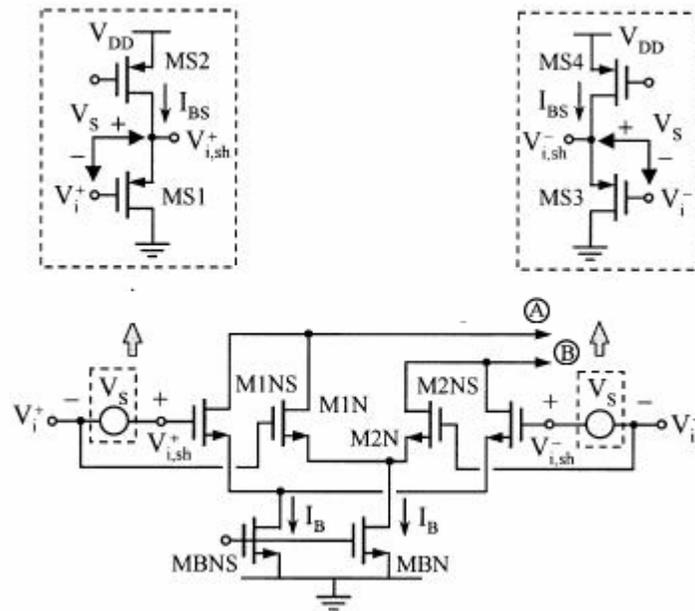
Figure 2-8. Dual n-ch Input Pair with Level Shift (modified) [9]

Figure 2-8 displays a two n-ch input pairs, one of which is attached to a level shifter.

The function of the level shifter is to shift the common-mode voltage seen at one of the input

pair to a higher voltage. This allows a single input pair to remain active as the common-mode moves near the negative supply voltage. As the common-mode shifts towards the positive supply, the level shifter will enter the triode region. When this occurs the input pair attached to the level shifter will no longer have the ability to differentially swing the signal. Thus only a single input pair will be active differentially. However, at the center of the common-mode both input pairs will be active and the differential g_m will be doubled. For this reason a canceling circuit is needed to keep the overall differential g_m constant.
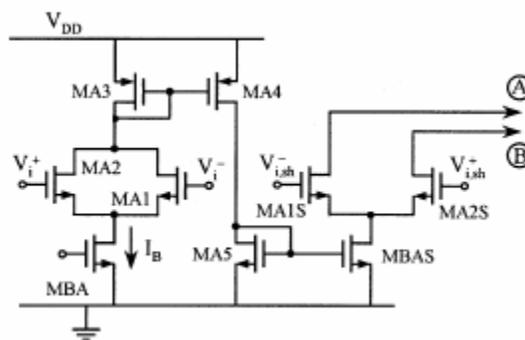
Figure 2-9. Cancellation Circuit (modified) **[9]**

Figure 2-9 displays the cancellation circuit that is used to keep the differential g_m constant. This circuit does not depend on a specific model, but uses a sensing pair to cancel the effects of the second input pair when both input pairs are active. As seen in Figure 2-9, terminals A and B are connected to the opposite terminals of that seen in Figure 2-8. This gives the differential cancelling effect needed to keep a constant differential g_m. It is noted that there is an emphasis on differential g_m in [9]. This is due to the fact that the common-mode g_m is not constant in the work. In [5, 7, 15], both the common-mode and the

differential g_m is kept constant; however, for an amplifier it is only important to ensure that the differential g_m is constant.

The design seen in [9] appears to alleviate many of the problems faced by complementary input pairs. An analysis of the design also proves that many of the requirements laid out for a good input stage in [12] are satisfied. A closer observation reveals that the large signal behavior of this architecture is not completely constant. The output g_o will vary tremendously as a result of the cancellation circuit which is used. The cancellation circuit will cause the current in the cascode stage to vary by a factor of three, which in turn changes the output g_o. Also, this use of current for cancellation purposes is seen as an inefficient use of current in the design.

2.2.5 Dual p-ch Input Pair Implementation

The same basic principle of implementing a dual input pair using a level shifter was explored in [14], but in this case a more current efficient and constant implementation is presented. In [14] a dual p-ch input pair is presented. The design implements level shifters on each input to regulate a constant voltage gain at the input. For this design there is no cancellation circuit used to keep g_m constant. Instead, a sensing circuit is used to alter the tail current through the input pairs, such that the total tail current is constant, irrespective of whether one or both pairs are active. This gives a constant g_m for the full common-mode range. The circuit that is used to achieve this constancy is seen in Figure 2-10.
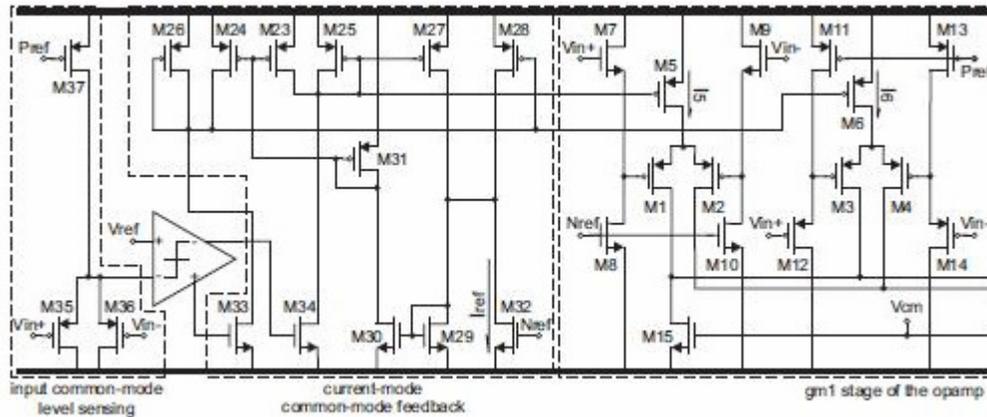
Figure 2-10. Dual p-ch Input Stage with Comparator Control [14]

In Figure 2-10, the sensing circuit is attached to a fully differential comparator. The sensing level is compared to a reference voltage V_{ref}, which will drive the gate of two control transistors. These control transistors will determine the amount of current in each of the input pairs. This is how the tail current is altered to maintain a constant g_m. In this implementation the voltage level of the takeover region is solely defined by V_{ref} [14]. Also the slope of the transition region is determined by the gain of the comparator, but in this case high gain is not compulsory.

The design seen in [14] has overcome the limitations of the architectures presented in [5, 7, 9, 15]. The input stage in [14] is capable of keeping a constant g_m with no strict matching requirements or no model assumption. The design maintains a constant total tail current which implies that there is a constant current in the cascode stage and a constant g_o. The current efficiency is better than that seen in [9], as there is no cancelling stage used. However the limitation of this design is its complexity. The complexity is much greater in

comparison to that seen in [5, 7, 9, 15]. The design in [14] need a reference voltage

generator, fully differential comparator, two level shifters, and common-mode feedback all as

a part of the input stage. This leads to the question of, can this sort of input stage with the

same functionality be implemented with lower complexity and possibly improve on the

constancies that have been achieved?

2.3 Proposed Design Implementation

The design proposed in this thesis attempts to implement a rail-to-rail input/output

operational amplifier with constant operation. The amplifier is designed for low voltage, low

power applications, which implies that the difference between the supply rails is comparable

to the value $V_{TN}+V_{TP} + 3*V_{Dsat}$ for the process. The main goal of the design is to present an

amplifier implementation that can achieve a constant operation, which is also robust to

process variations, similar to that seen in [9, 14]. The idea of constant operation in this work

is depicted as holding specifications such as gain, gain-bandwidth product, phase margin,

slew rate, and power consumption constant across the entire common mode range. This is

accomplished by designing an amplifier which keeps small signal and large signal parameters

constant over the common mode range. Achieving a constant operation which is robust to

process variations primarily lies in the design of the input stage and thus is the primary focus

of this work.

2.3.1 Input Stage

The input stage in this design will consist of a folded cascode stage with a dual n-ch input pair as seen in [9]. The dual n-ch input pair is capable of a rail-to-rail input common mode range. This is realized by using a level shifter at the input of one of the input pairs. The use of a level shifter allows the common mode voltage or the input gate bias voltage to be shifted a voltage Vs above the actual common mode. This ensures that one of the input pairs remains active when the common mode voltage approaches the negative supply. When the common mode approaches the positive supply, the current source attached to the level shifter will then enter a triode region, and the circuit will only allow for a single input pair to be active through the sensing circuit. The operation of this dual n-ch input pair implementation is much like that of the complementary p-ch, n-ch input pairs, which are traditionally used to achieve a rail-to-rail input common mode range as seen in [1-4, 7, 15]. The two implementations are similar in that at the center of the common mode range both input pairs are active; however, as the common mode approaches either of the supply rails, only a single input pair will be turned on.

The advantage to using a dual n-ch input pairs as opposed to the traditional complementary input pairs is its robustness to process variations. This implementation is naturally more robustness because of its uses of a common pair as the input pairs (i.e. two n-ch input pairs). Using this architecture, both input pairs can be well matched to one another with the use of common centroid layout techniques. The biasing current sources for these input pairs can also be laid out to have a common centroid. With a common centroid layout, both input pairs and current sources will have similar temperature and process sensitivities.

This sort of layout technique cannot be used with complementary input pairs. Thus it is immediately seen that an improvement in robustness is expected with this implementation.

The input stage that is presented in this work is a dual n-ch input pair. It is noted that the design can also be implemented with a dual p-ch input pair as seen in [14]. This work makes use of the robustness this implementation offers, and attempts to improve its ability to hold small signal and large signal parameters constant through sensing and control circuitry. The idea of keeping small signal and large signal parameters constant gives way to make the circuit more compatible for implementing gain boosting techniques such as regulation, positive feedback, etc. Constant small signal and large signal parameters also allow the compensation of the amplifier to be more efficient and can eliminate the need to overcompensate the amplifier at certain common mode levels. Much of this is achieved by the use of a new current sensing circuit, which is presented in the next chapter. The goal is to achieve each of these design merits with less complexity than that seen in [14]. As mentioned previously, much of this is achieved through the implementation of the first stage of the design.

2.3.2 Output Stage

The output stage of this design is a typical class-AB output. The design implements a class-AB output stage to achieve a rail-to-rail output as needed for low voltage applications. The design of the output stage is not as critical as that of the input stage, as many of the

design specification are dependent on the input stage. It is for this reason that there will be a

limited discussion on the output stage.

2.4 Target Design Specifications

The intended design specifications were made comparable to what is seen in [5, 7, 9,

14, 15], to prove the validity of the design and show that there is no degradation in

performance. The main specifications of interest include: the supply voltage, power

consumption, DC gain, gain bandwidth product, phase margin, and the capacitive load

driven. Other specification will be reported for the design; however, there will be no specific

design requirements. A summary of the design specification intended along with the

specifications achieved in [5, 7, 9, 14] is seen in Table1.

Table 1: Specifications Summary

Specifications	[9]	[5]	[14]	[7]	This Design
Input Stage	Duel n-ch pair	Complementary input pairs with overlapped transition regions	Duel p-ch pair	Complementary input pair	Duel n-ch pair
Supply Voltage (V)	3	3	1	3	2.2
Process (um)	0.8	1.2	0.065	1	0.5
Power Consumption (mW)	4.8	0.31	0.72	9	1mW
Gain A_v (dB)	95.1	113	100	85	110
Phase Margin (°)	60	>45	64	66	55
GBW (MHz)	17.5	5.5	40	2.6	15
Capacitive Load C_L (pF)	15	10	15	10	15

2.4.1 Supply Voltage

The supply voltage will be set at $V_{supply} = 1.37 * (V_{TN} + V_{TP})$. This gives a supply voltage of approximately 2.2V for the AMI 0.5um process. This classifies the amplifier as a low voltage design.

2.4.2 Power Consumption

The aim in most designs is to keep the power consumption to a minimum to allow devices to be suitable for portable or battery powered electronics. The aim of this work is to have a power consumption that is approximately 1mW.

2.4.3 DC Gain

The DC gain that is desired for this design is 110dB. The goal will be to design the amplifier to be compatible for allowing gain boosting techniques to optimize the gain. However, gain boosting will not be implemented in the presented design.

2.4.4 Gain Bandwidth

In this design, it is desirable to keep the gain bandwidth product and the unity-gain frequency constant across common mode inputs. This implies that the g_o value in the cascode stage of the design is kept constant. This is achieved by keeping the tail current at the input stage constant. The aimed design value for GBW is 15MHz, which is comparable to what is seen in [9] for the same capacitive load.

2.4.5 Phase Margin

The phase margin of the design will be set for 55 degrees. This is a typical specification that most amplifiers meet. At 55 degrees the amplifier is considered stable and gives minimum peaking in the step response.

2.4.6 Capacitive Load

The capacitive load used in the works discussed in this chapter use loads between the values of 10pF and 20pF. The design which this work will most resemble [9] uses a value of 15pF as its load. For this reason the capacitive load of this design is set to 15 pF.

CHAPTER 3. LOW VOLTAGE OPAMP DESIGN

3.1 Introduction

This chapter presents the design of a new low voltage rail-to-rail operational amplifier with constant operation. The idea of constant operation in this work implies that important small signal and large signal parameters are kept constant over the entire input common-mode range. Parameters such as g_m and g_o are kept constant to ensure that amplifier specifications such as DC gain, GBW, PM, and slew rate are constant. It is important to guarantee that these parameters are constant as variations can lead to instability or overcompensation in the amplifier [15]. Also at low voltage, it is desirable to have the same performance for the full V_{icm}, to allow the input signal to be as large as possible to maximize the SNR of the amplifier. This is to be done with a low complexity and increased process robustness implementation.

This chapter is organized as followed. The first section gives a brief mathematical analysis of the need for rail-to-rail operations at low voltages. The next section gives a general description of the new architecture, and also points out possible limitations. The section further describes the analysis of the new architecture and presents critical equations and expressions, which will ad in the design process of the amplifier. The third section explicitly discusses the design procedures of the new architecture and points out the trade-offs of the design. The final section presents the supplementary circuitry of the complete amplifier. This includes the bias generators needed to produce essential power supply independent reference voltages and currents.

3.2 Brief Rail-to-Rail Analysis

In the previous chapter it has been discussed that a rail-to-rail input common-mode range is needed when implementing low voltage structures, due to the need to maximize SNR at the input. As the supply voltage of an operational amplifier is decreased, the V_{icm} will also decrease. Depending on the amplifier architecture, the V_{icm} may reduce to a small percentage of the supply voltage. This can cause a small SNR at the input, as the noise level for a given circuit is fixed with the supply voltage. Thus, it becomes of interest to maximize the possible input signal in order to maximize SNR. To understand the limitation of V_{icm}, a quantitative review of V_{icm} for two amplifier architectures will be discussed. Also, a V_{icm} analysis of a commonly used input rail-to-rail architecture will be explored.

3.2.1 V_{icm} Limitations

A commonly used amplifier structure is seen in Figure 3-1. This is a differential input single ended output amplifier with a tail current bias. The positive supply is given by V_{DD}, and the negative supply is given by V_{SS}. By inspection, the V_{icm} range can be determined. The V_{icm} range is given by the minimum voltage needed at the gate of the input pair M1 and M2, to keep M5 in saturation, as well as the maximum voltage possible at the input that will allow M1 and M2 to remain in saturation. This range is given in (3.1), where V_{Dsat} is the minimum saturation voltage of a transistor, V_{TP} is the threshold voltage of a p-ch device, and V_{TN} is the threshold voltage of an n-ch device.

$$V_{SS} + V_{DSAT1} + V_{DSAT5} + |V_{TN}| \le V_{icm} \le V_{DD} - |V_{TP}| - V_{DSAT3} + |V_{TN}| \tag{3.1}$$
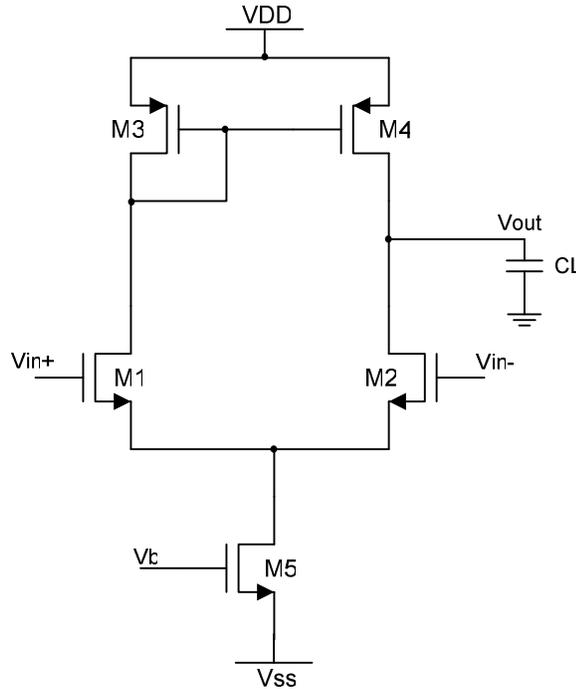
Figure 3-1. Commonly Used Amplifier Architecture

For the AMI 0.5um process the typical values of V_{TP}, V_{TN}, and V_{Dsat} are 0.9V, 0.7V, and 0.2V; respectively. Using these values, if the supply voltages in Figure 3-1 are set to $V_{DD} = 5V$ and $V_{SS} = 0V$, the V_{icm} range would be given by,

$$1.1V \le V_{icm} \le 4.6V .$$

This implies that the V_{icm} range is 3.7V, which is 70% of the supply voltage. Suppose that the supply voltage for the amplifier in Figure 3-1 is reduced to $V_{DD} = 2.2V$ and $V_{SS} = 0V$. The resulting V_{icm} range would be given by,

$$1.1V \le V_{icm} \le 1.8V .$$

The V_{icm} range in this case has reduced to 0.7V which is now 32% of the supply voltage. It is observed that as the supply voltage is reduced, the V_{icm} range will all decrease. As a result, the SNR is also decreasing since the noise level for a given circuit architecture is fixed. The analysis for Figure 3-1 was done using an n-ch input pair, however it is noted that a similar analysis follows for a p-ch input pair amplifier. The architecture seen in Figure 3-1 typically is not expected to have a large common-mode range, and hence is not commonly used in low voltage designs with large V_{icm} range requirements.

Figure 3-2 displays an amplifier architecture which has an increased V_{icm} in comparison to the circuit seen in Figure 3-1. Figure 3-2 displays a folded cascode amplifier with n-ch inputs. Since voltage biases are used to bias the gate of the cascode transistors as opposed to a current mirror like seen in Figure 3-1, the V_{icm} range is increased. The V_{icm} range is given by (3.2).

$$V_{SS} + V_{DSAT1} + V_{DSAT11} + \left| V_{TN} \right| \leq V_{icm} \leq V_{DD} - V_{DSAT3} + \left| V_{TN} \right| \tag{3.2}$$
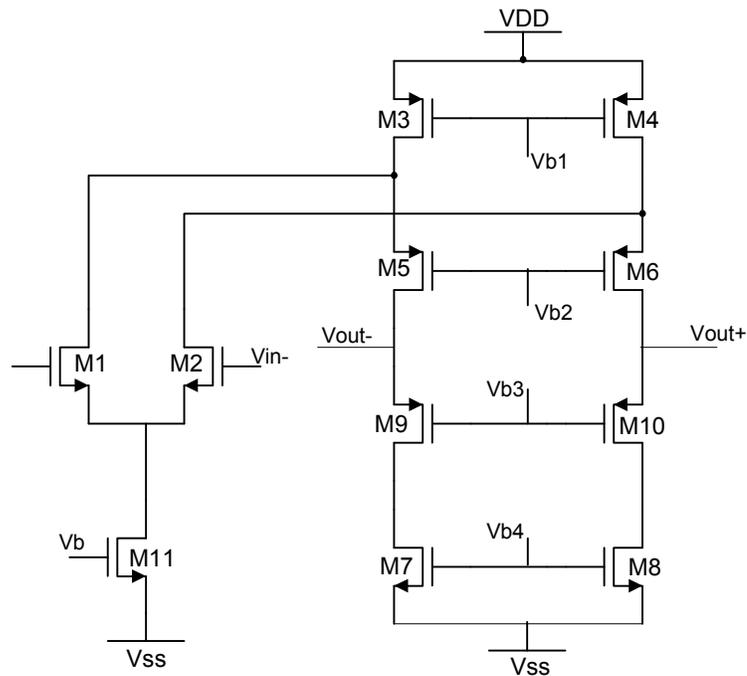
Figure 3-2. Folded Cascode n-ch Input Architecture

For the structure in Figure 3-2, if the supply voltages are set to $V_{DD} = 2.2V$ and $V_{SS} = 0V$, the V_{icm} range is given by:

$$1.1V \leq V_{icm} \leq 2.7V .$$

This structure has a V_{icm} range equal to 1.6V which is 73% of the supply voltage. It is seen that the positive V_{icm} limit is higher that V_{DD}. This implies that the common-mode can swing higher than the supply rail, and the circuit will continue to function properly. However, this circuit does not have a full common-mode input range. This means that the SNR for the circuit is not maximized. To achieve a rail-to-rail V_{icm}, a similar architecture to Figure 3-2 is implemented with an additional input pair.

3.2.2 Rail-to-Rail V_{icm}

A circuit that is capable of achieving a rail-to-rail V_{icm} is seen in Figure 3-3. This is similar to the architectures seen in [1-8]. Figure 3-3 displays an n-ch and p-ch complementary input folded cascode architecture. It can be shown that this circuit is capable of a rail-to-rail V_{icm}, by observing its V_{icm} range. To analyze the V_{icm} range for this particular circuit, the V_{icm} range of each input pair must be studied. First the V_{icm} range for the n-ch input pair is seen in (3.2). A similar analysis is performed to obtain the expression for the V_{icm} range for the p-ch input pair. The p-ch input pair is given by (3.3). The total V_{icm} range for Figure 3-3 is given by the addition of the ranges from (3.2) and (3.3). This gives a complete V_{icm} range which is seen in (3.4).

$$V_{SS} + V_{DSAT10} - \left| V_{TP} \right| \le V_{icm} \le V_{DD} - V_{DSAT4} - V_{DSAT14} - \left| V_{TP} \right| \qquad (3.3)$$

$$V_{SS} + V_{DSAT10} - \left| V_{TP} \right| \le V_{icm} \le V_{DD} - V_{DSAT5} + \left| V_{TN} \right| \qquad (3.4)$$
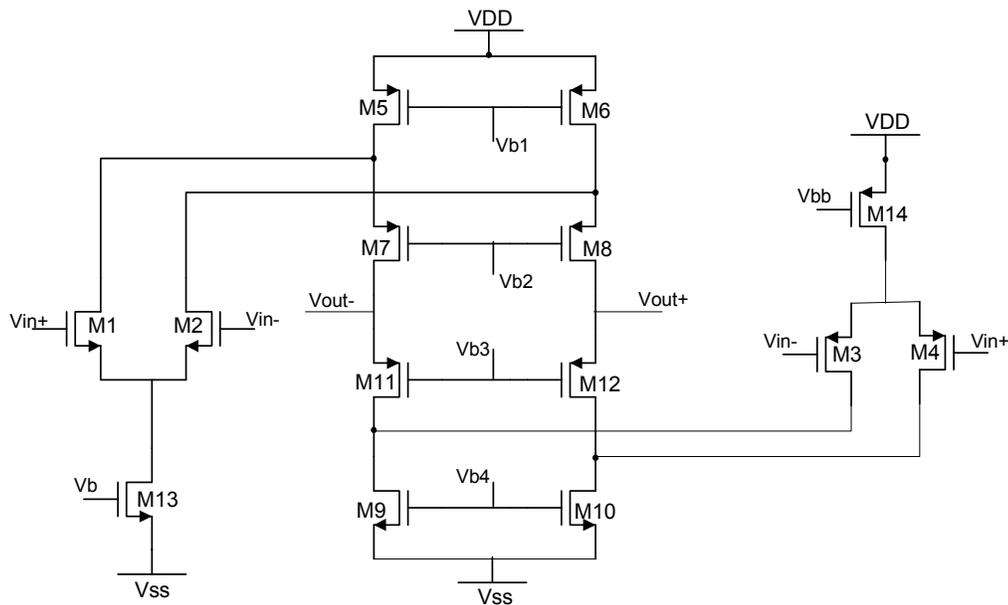
Figure 3-3. Folded Cascode Complementary Input Architecture

Suppose that the supply voltage is set to $V_{DD} = 2.2V$ and $V_{SS} = 0V$; the range of the V_{icm} for Figure 3-3 can be determined using (3.4). The range is given by,

$$-0.7V \leq V_{icm} \leq 2.7V .$$

As expected, the V_{icm} range is greater than the supply voltage. This implies that the input signal can be as large as the supply voltages, which will maximize the SNR of the circuit. Therefore, the circuit in Figure 3-3 theoretically solves the problem of achieving a rail-to-rail input. However the issues discussed in chapter 2 (e.g., obtaining a constant g_m, maintaining a constant current flow, etc.) still prove to be troublesome for this architecture. The architecture presented in this chapter will also achieve a rail-to-rail input in addition to keeping important amplifier parameters constant with low complexity.

3.3 Proposed Operational Amplifier Architecture

The operational amplifier architecture consists of a typical two stage amplifier. The first stage includes a rail-to-rail input stage implemented by a dual n-ch input pair. The complete first stage is a folded cascode architecture, where the total tail current is held constant by the input stage and sensing circuit. The second stage of the amplifier is a class-AB output stage, which is capable of rail-to-rail output swings. Between the amplifier stages, miller compensation techniques are utilized to achieve an acceptable phase margin to ensure stability. The amplifier is implemented in an AMI 0.5um process and is capable of operating at low voltages relative to the process.

3.3.1 First Stage

3.3.1.1 Input Stage

The first stage of the design is a folded cascode architecture. The most important portion of the first stage is found in the input stage. The input stage consists of dual n-ch input pairs, similar to that which is presented in [9]. The input stage of the design can be seen in Figure 3-4. It consists of two identical n-ch input pairs M1 – M4. M1 and M2 is a typical n-ch input pair. The input to the amplifier is attached directly to the gates of this input pair. This implies that as the common-mode approaches the negative rail and the V_{GS} of M1 and M2 falls below V_T, the input pair will enter a cut-off region. To guarantee that M1 and M2 and the tail current source operate in saturation, it is given that the common-mode level must be greater than $V_{SS} + 3*V_{Dsat} + V_T$. The value $3*V_{Dsat}$ comes from the implementation of the constant current source, which is realized by two cascoded n-ch

transistors. When the input common mode falls below $V_{SS} + 3*V_{Dsat} + V_T$, this input pair will be turned off. Thus it is observed that a single input pair is not sufficient to achieve rail-to-rail input operations. This induces the need for the second input pair.

The second input pair, M3 and M4 is attached to a level shifter. The purpose of the level shifter is to shift the common-mode level high enough to allow this n-ch input pair to remain active at low common mode voltages. That is, the level shifter should ensure that when the V_{icm} is equivalent to the negative supply rail V_{SS}, the voltage at the gate of M3 and M4 is above $V_{SS} + 3*V_{Dsat} + V_T$. This is so that this input pair and its tail current source will be operating in full saturation. If the level shifter were not present, as the common-mode voltage approaches the negative supply V_{SS}, the input pair would behave just like M1 and M2. However with the use of a level shifter, as the common-mode voltage approached the negative rail, the V_G of M3 and M4 will be a voltage Vs above the negative supply. The value Vs is designed to be greater than $V_{SS} + 3*V_{Dsat} + V_T$, thus the input pair M3 and M4 will remain active for low common-mode voltages.

Figure 3-4. Dual n-ch Input Stage

3.3.1.2 Level Shifter

The realization of the level shifter is implemented using a source follower circuit.

M5 and M7 serve as the source followers and M6 and M8 are the current bias transistors.

M6 and M8 are each attached to the bias point Vb1, which will induce a current flow through

M5 and M7. The sizing of M5 and M7 will determine the V_{GS} of the pair, where the V_{GS} is

the level shift Vs which is desired. As the common-mode voltage of the input approaches the

positive supply rail V_{DD}, the transistors M6 and M8 will enter a triode region that will cause

the gate voltage of M3 and M4 to pull-up to V_{DD}. This eliminates the capability of M3 and

M4 to differentially swing the output signal. Thus, when this takes place, the differential

swing of the signal is only dependent on M1 and M2.

The function of the dual n-ch input pairs is much like that of the complementary n-ch and p-ch input pairs. As described, when the common-mode is near the negative rail the pair M3 and M4 is active and has the capability to differentially swing the signal. At the center of the common-mode both pairs M1 – M4 will be active and each pair will be able to differentially swing the signal. Last, at high common-mode levels, the pair M3 and M4 will loose its differential swinging capability due to the level shifter, and only M1 and M2 will differentially swing the signal. However M3 and M4 will remain turned on for high common-mode voltages, which implies that both input pairs will be turned on for most of the common-mode range. This is a problem that is not experienced by complementary input pairs and will have to be compensated accordingly.

Just as seen in the operation of a complementary input pair, the g_m is not constant for the full V_{icm} since two input pairs will be active in the center of the common mode range. To compensate for this, the tail current is typically altered at certain common-mode levels to allow for a constant g_m [1-8]. The same approach is implemented for this design using a proper sensing circuit.

3.3.1.3 Constant gm Control

In Figure 3-4 it is depicted that the input pair M1 and M2 are biased by a constant tail current source. It is observed that as the V_{icm} nears the V_{SS}, the tail current will be pushed into triode and the input pair M1 and M2 will be turned off. When this occurs, the value of the tail current source attached to M1 and M2 will be near zero. As the common-mode rises,

the tail current source will also raise to the value I, as indicated in the Figure. Thus it is noted that the tail current source is not actually constant across the entire V_{icm}.

The tail current source attached to the input pair M3 and M4 is depicted as a variable tail current, which is one of the innovations of this design. The variable tail current source operates inversely to the constant tail current source attached to M1 and M2. As previously described, the tail current source attached to M1 and M2 will change with the common-mode. At low common-mode values the current source value will be near zero. As the common-mode rises, the input pair M1 and M2 turns on, and the current source will raise to the value I. The variable current source will do the opposite. When the common mode is low, the variable tail current source will hold the value I. As the common-mode rises and the constant tail current source approaches the value I, the variable current source will approach zero. This is done to keep the overall g_m of the input stage constant, as well as to hold the total tail current to the value I. The control of the variable tail current source is operated by a separate sensing circuit.

3.3.1.4 Sensing Circuit

The sensing circuit used to control the variable tail current source can be seen in Figure 3-5. As seen in the Figure, the sensing circuit has two pairs of n-ch sensing transistors, MS1 – MS4 that are used to sense the common-mode. MS1 and MS2 are attached to the shifted input Vins, which is the output of the level shifter in Figure 3-4. MS3 and MS4 are attached directly to the input of the amplifier. MS1 – MS4 are biased by a constant tail current source I, where the value of I is the same as that seen in Figure 3-4. The

bias point Vb2 and Vb3 are used to bias the variable tail current source seen in Figure 3-4, which is implemented with two cascode n-ch transistors.

As stated, the sensing of the common-mode is depended on MS1 – MS4. MS3 and MS4 will sense the regular common-mode voltage. When the common-mode voltage is low MS3 and MS4 will be turned off and the current flow through the pair will approach zero. As the common-mode goes high, the pair MS3 and MS4 will be turned on and the current through the pair will approach I. The pair MS1 and MS2 will sense the shifted common-mode voltage. This implies that this pair will always remain active and will flow the current I for all common-mode voltages.

Figure 3-5. Sensing Circuit

Both input pairs are attached to p-ch transistors which function as current mirrors. These current mirrors will steer the current through the pair MS1 and MS2 to either the right or left half of the circuit for different common-mode voltages. For low common-mode voltages, the pair MS3 and MS4 will be turned off which will cause the current through MS1 and MS2 to be mirrored to the left side of the circuit through MS8 and MS9. The current through MS8 and MS9 is then mirrored to the variable tail current source. As the common-mode begins to rise, the pair MS3 and MS4 will start to turn on and the current through MS1 and MS2 will be shifted to the right half of the circuit. This effectively decreases the current through MS8 and MS9 as the common-mode voltage rises. Decreasing the current through MS8 and MS9 implies that the current in the variable tail current source from Figure 3-4 is also decreasing. When the common-mode approaches the positive supply rail, the pair MS3 and MS4 will be fully active and will flow the current I. In this case, all the current from the pair MS1 and MS2 will be mirrored to the right half of the circuit, and the current through MS8 and MS9 will approach zero.

The sensing circuit effectively controls the variable tail current source with the common-mode. The use of MS3 and MS4 allows the sensing circuit to control the variable tail current source inversely to the fixed tail current source in Figure 3-4. The advantage of this circuit is that there is no specific model assumption used to control the variable tail current source as seen in other works [1-15]. This circuit can also be design to operate with great accuracy as matching between the input pair M1 and M2 in Figure 3-4 and MS3 and MS4 in Figure 3-5 will determine the accuracy. Using particular layout techniques seen in [16] to achieve a high level of matching will ensure the accuracy of the circuit.

3.3.1.5 First Stage Overview

The complete first stage of the operational amplifier of this design can be seen in

Figure 3-6. The first stage is designed using dual n-ch inputs. The input stage does not rely

on strict matching requirements between n-ch and p-ch devices. The dual n-ch input pair

also has the advantage of being robust to process variations as opposed to the complementary

n-ch and p-ch input pair implementation. Through the use of a sensing circuit the g_m of the

input stage is kept constant for the entire common-mode range. The method of keeping g_m

constant in this implementation has the advantage that it does not rely on a specific transistor

model to prove valid. As seen in other works [1-15] the methods used to keep g_m constant

typically rely on the square-law model of a transistor. However in this case, the

implementation only requires that the input pairs M1 – M4 and the sensing pairs MS1 – MS4
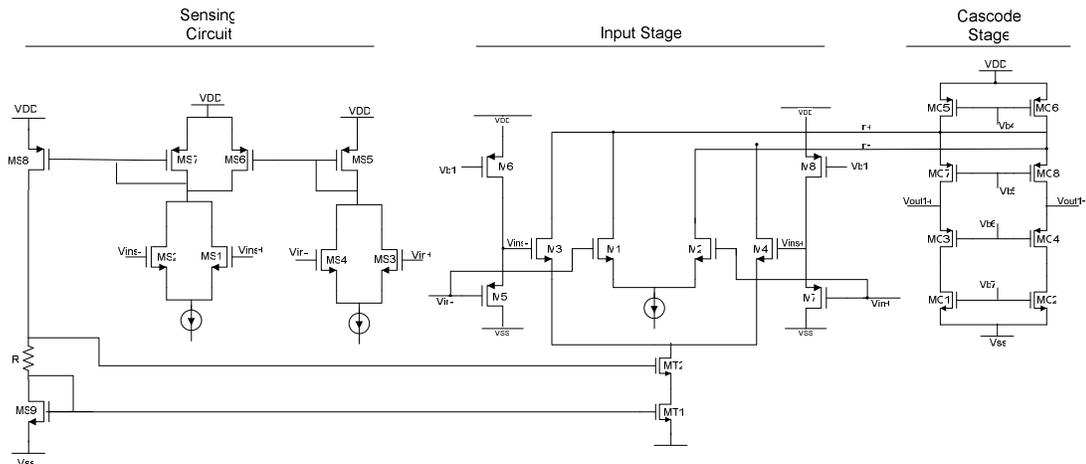
use the same model, which is a valid assumption.

Figure 3-6. First Stage Amplifier Design

The use of the sensing circuit also allows for the total tail current to remain constant for the full common-mode range. This is advantageous because it implies that the current through the cascode stage will also be kept constant. It is desirable for the cascode stage current to be constant, since the output g_o of the first stage is highly dependent on this current. Thus, if there are variations in the cascode stage current, there will be variation in the output g_o and as a result variations in the DC gain, gain bandwidth, etc. The architecture for this design essentially achieves the functionality of that seen in [14], however with the advantage of a design whose complexity is significantly reduced.

The cascode stage has four bias points, which are generated by a reference circuit. The output of the first stage is located at the center of cascode stage. The output of the first stage serves as the input to the second stage, which is also the output stage. The output stage as previously mentioned does not greatly effect the constant operation that is achieved in the first stage, but does influence the swing range of the output signal. For this reason very little emphasis is placed on the output stage design.

3.3.2 Output Stage

The output stage for the design is a class-AB output stage with rail-to-rail output swing. Rail-to-rail output swing is important at low voltages in order to maximize the SNR at the output. The implementation for the design can be seen in Figure 3-7. The implementation seen is Figure 3-7 represents one half of the output stage. The complete

amplifier is a fully differential structure, and the other half of the output stage would be a

replica of Figure 3-7 with reversed inputs. The implementation is a relatively basic

architecture, which does not require a detailed analysis as given for the first stage design.
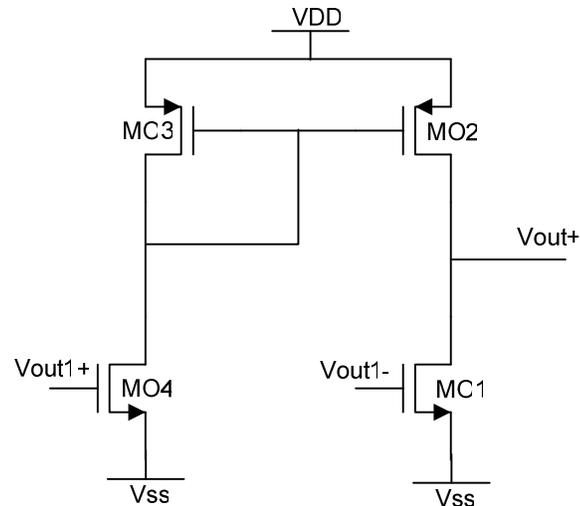

Figure 3-7. Output Stage Amplifier Design

The architecture seen in Figure 3-7 is a common source amplifier with a push-pull

operation which allows for a rail-to-rail output swing. The input to the common source

amplifier is feed from the output of the first stage. The common source amplifier MO1 is

biased from the DC voltage of the negative output of the first stage.   The current through

MO1 is set by the current flow through MO2. MO2 has a variable current flow, which can

vary with the transient signal. This is what forms the push-pull nature of the output stage.

The current in MO2 is determined by the current in MO4 and MO3. MO3 and MO2 form a

current mirror and will be proportional to on another. A large mirror gain from MO3 to MO2

is used, so that MO3 and MO4 do not consume much current and power. The current in

MO4 is determined by the positive output of the first stage. It is noted that the quiescent

current in MO1 and MO2 is set by the quiescent voltages Vout1+ and Vout1-. Thus, a

common mode feedback circuit is needed to stabilize Vout1+ and Vout1- in order to stabilize

the output stage. The push-pull operation is observed when the input signal swings

differentially and the positive output of the first stage goes high, which implies the negative

output of the first stage goes low. This causes the current in MO4 to increase. This will push

a larger current to the output through MO2. When the differential signal does the converse,

MO1 will pull increased current to the output. This is the basic idea of the push-pull

structure.

Since there is a push-pull operation present in the output stage, the output can swing

near the positive and negative rails. The complete output stage also includes a compensation

section which ensures stability for the two stage structure. As mentioned, Figure 3-7

represents one half of the output stage. A full schematic of the fully differential amplifier

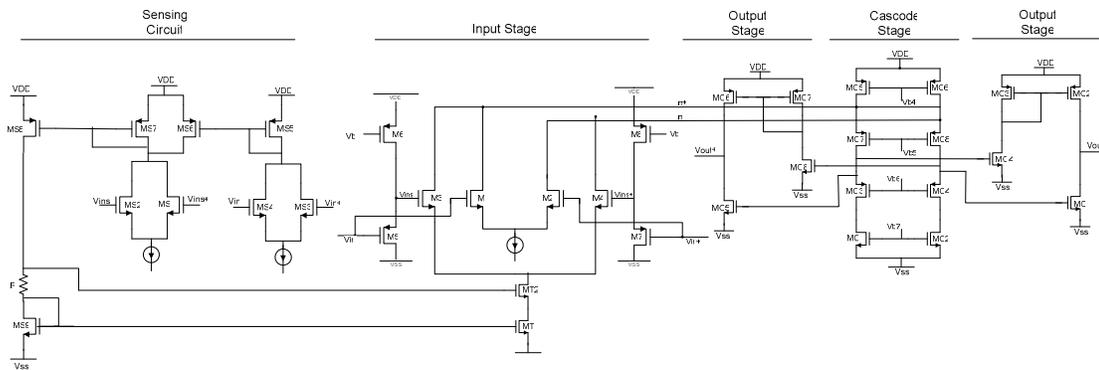excluding bias circuits and reference generators can be seen in Figure 3-8.

Figure 3-8. Fully Differential Amplifier Excluding Bias Circuits

3.4 Operational Amplifier Analysis

The theoretical analysis of the operational amplifier presented in the previous section is necessary to aid in the amplifier design process. It is important to theoretically demonstrate that the claims made in the previous section in fact hold true. Also it is imperative to understand the possible limitations of the architecture, to allow for a valid comparison of this design versus other amplifier architectures. In this section an analysis of the V_{icm} range for the amplifier of this work be presented, followed by an analysis of the level shifter and its limitations. Next the need for a constant g_m in low voltage circuits will be demonstrated. Last the robustness of g_m for the chosen dual n-ch input pair architecture will be explored.

3.4.1 V_{icm} Analysis

The V_{icm} range can be written by inspection of circuit given in Figure 3-6. It is noted that the constant tail current source should be replaced with two cascoded n-ch transistors to observe the common-mode range. As noted in section 3.2, to write an expression for the V_{icm} range, the range of each input pair must be summed together. The range of the pair M1 and M2, is nearly the same as that seen in (3.2). However, the range for M1 and M2 in Figure 3-6 slightly differs since the tail current source is cascoded in this case. The V_{icm} range for M1 and M2 in Figure 3-6 is given by (3.5). The use of cascoded tail current sources decreases the lower bound of the V_{icm} by V_{Dsat}.

$$V_{SS} + 3*V_{Dsat} + |V_{TN}| \leq V_{icm} \leq V_{DD} - V_{Dsat} + |V_{TN}| \qquad (3.5)$$

The V_{icm} range for the input pair M3 and M4 in Figure 3-6 is different than the V_{icm} of the input pair M1 and M2, due to the use of the level shifter. The level shifter shifts the common-mode voltage up by a value of Vs and thus changes the lower bound of the V_{icm} range by the value Vs. The V_{icm} range of the input pair M3 and M4 is given by (3.6).

$$V_{SS} + 3*V_{DSAT} + |V_{TN}| - V_S \leq V_{icm} \leq V_{DD} - V_{DSAT} - V_S \qquad (3.6)$$

As previously stated the value Vs is designed to be larger than $3*V_{Dsat} + V_{TN}$, which ensures that the lower bound for the V_{icm} is less than V_{SS}. If the supply rails are set to V_{DD} = 2.2V and V_{SS} = 0V, Vs is set to 1.3V, and all other parameters are as given in section 3.2, the V_{icm} range comes out to be,

$$0V \leq V_{icm} \leq 2.7V .$$

Thus, it is true that the V_{icm} of the dual n-ch input pair is rail-to-rail with the use of a level shifter. In order to identify any possible limitations, it is now important to analyze the level shifter, which allows for a rail-to-rail V_{icm}.

3.4.2 Level Shifter Analysis

The level shifter used in Figure 3-6 is implemented by a source follower circuit. Until this point, it has been assumed that the level shifter has no effect on the signal and acts as an ideal level shifter, but this is not necessarily true. In order to analyze the effects of the level shifter, a transfer function must be derived. For simplicity, the model seen in Figure

3-9 is used to derive a transfer function for the level shifter. In the model in Figure 3-9, the value of C_L consists of all the capacitors at the V_O node summed together. Similarly, the value R_L consists of all resistance values at the output node. The derivation for the level shifter transfer function is begun by writing the KCL at the node V_O. The derivation can be seen in (3.7) – (3.9).

$$-(V_i - V_o)g_m + (V_o - V_i)sC_{GS} + V_o sC_L + V_o \frac{1}{R_L} = 0 \qquad (3.7)$$

$$-V_i(g_m + sC_{GS}) = -V_o\left(g_m + \frac{1}{R_L} + s(C_{GS} + C_L)\right) \qquad (3.8)$$

$$\frac{V_o}{V_i} = \frac{(g_m + sC_{GS})}{\left(g_m + \frac{1}{R_L} + s(C_{GS} + C_L)\right)} \qquad (3.9)$$

An observation of equation (3.9) shows that there is some loss in the level shifter at low frequencies. There will not be an ideal level shift. However, it is observed that the loss can be minimized by maximizing R_L. This is a consideration that should be accounted for during the design phase. Also from equation (3.9), it is observed that the level shifter creates a pole and zero in the signal path. The pole is found at the frequency given in (3.10) and the zero is located at the frequency given in (3.11).

$$P = -\frac{g_m + \dfrac{1}{R_L}}{C_{GS} + C_L} \tag{3.10}$$

$$Z = -\frac{g_m}{C_{GS}} \tag{3.11}$$

The pole seen in (3.10) could be considered troublesome if it is near the unity gain frequency of the complete amplifier. If this is the case, there will be additional phase degradation when the input pair attached to the level shifter is active. For this reason, the pole of the level shifter must be pushed to a high frequency to avoid phase variations in the output due to the level shifter. In equation (3.10) it is seen that the pole can be pushed to a higher frequency by increasing the g_m of the level shifter or decreasing the load capacitor on the output node in Figure 3-9. These considerations are vital for an efficient design of the level shifter circuit in this amplifier structure. Another solution to avoid a phase degradation resulting from the level shifter is to shift the zero of the level shifter closer to its pole. The closer the pole and the zero of the level shifter, the less amount of phase delay at the output. Equations (3.10) and (3.11) give insight on how to reposition the pole and zero of the level shifter to be as close as possible for minimal phase degradation.
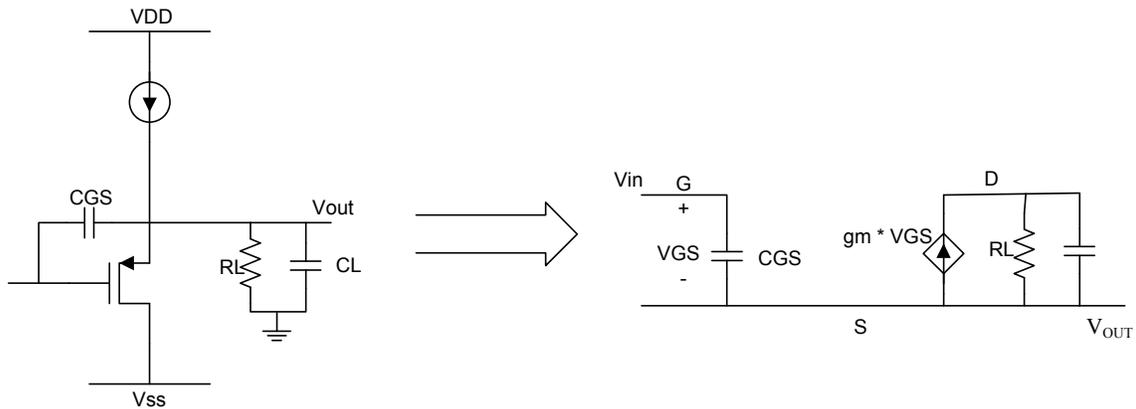
Figure 3-9. Level Shifter Small Signal Model

The analysis of the level shifter proves that there are some limitations associated with the use of the level shifter. The first limitation includes the non-ideal shift of the level shifter. It is seen that there is a loss associated with the level shifter which should be considered. The second limitation of the level shifter includes the pole created in the signal path. This can be troublesome and could possibly limit other design parameters of the amplifier when trying to compensate for this pole.

3.4.3 Constant gm Analysis

The need for constant g_m in the input pair has been discussed in [2, 4, 5, 7, 9, 10, 12-14]. However, it has not been shown how variations in g_m directly affect amplifier parameters. An analysis of a basic amplifier structure can give insight on how g_m relates to amplifier parameters. A basic amplifier structure is seen in Figure 3-1. In this figure, an input to output transfer function can be easily derived. A simplified transfer function for Figure 3-1 is seen in (3.12). From equation (3.12), the DC gain expression and the GBW expression can be written and are seen in (3.13) and (3.14) respectively.

$$A(s) = \frac{g_{m1}}{g_{O1} + g_{O3} + sC_L}$$ (3.12)

$$A_{VO} = \frac{g_{m1}}{g_{O1} + g_{O3}}$$ (3.13)

$$GBW = \frac{g_{m1}}{C_L}$$ (3.14)

From equations (3.12) – (3.14) it observed that g_m is directly proportional to the DC gain and GBW. This implies that any variations in g_m will be directly seen in the DC gain and GBW. For low voltage amplifiers, variations in the DC gain and GBW can greatly affect performance. Also, for a two stage structure like the one presented in this work, variations in DC gain and GBW will cause the amplifier to have large variations in the phase margin and possible become unstable. It is also seen in (3.13) that the DC gain can be affected by variations in g_o. However, in [2, 4, 5, 7, 9, 10, 12-14] this troublesome variation is neglected, yet it should be considered to create an amplifier with an increased constant operation as observed in (3.13).

A folded cascode structure such as that seen in Figure 3-2 can be analyzed in a similar fashion. An approximation of the DC gain and GBW can be seen in (3.15) and (3.16). For equations (3.15) and (3.16), the same g_m dependence is observed. This analysis can be extended to the first stage of the architecture presented in this work, Figure 3-6. The DC gain expression is similar to that seen in (3.15), but for this amplifier, there will be three

distinct regions because as the common–mode changes, there are three operation regions of this amplifier as discussed in previous sections. Thus the DC gain will be defined for each region. It is intended for each region to hold the same value; however, depending on the design there may be variations. The DC gain is given in (3.17). It is noted that for (3.17) the effects of the level shifter are neglected for this analysis.

$$A_{VO} = \frac{g_{m1}}{(g_{O1} + g_{O5})\dfrac{g_{O3}}{g_{m3}} + g_{O7}\dfrac{g_{O9}}{g_{m9}}} \qquad (3.15)$$

$$GBW = \frac{g_{m1}}{C_L} \qquad (3.16)$$

$$A_{VO} = \begin{cases} \dfrac{g_{m1}}{(g_{O1} + g_{OC5})\dfrac{g_{OC7}}{g_{mC7}} + g_{OC1}\dfrac{g_{OC3}}{g_{mC3}}}, & region1 \\[4ex] \dfrac{g_{m1} + g_{m3}}{(g_{O1} + g_{O3} + g_{O5})\dfrac{g_{O3}}{g_{m3}} + g_{O7}\dfrac{g_{O9}}{g_{m9}}}, & region2 \\[4ex] \dfrac{g_{m3}}{(g_{O3} + g_{OC5})\dfrac{g_{OC7}}{g_{mC7}} + g_{OC1}\dfrac{g_{OC3}}{g_{mC3}}}, & region3 \end{cases} \qquad (3.17)$$

The expression given in (3.17) is also similar to the expression for the DC gain of a complementary input pair folded cascoded amplifier. If the g_{m3} and g_{m4} values are replaced

with p-ch g_m values the expression for a complementary input pair amplifier could be obtained. This observation illustrates the need for the g_m values of the n-ch and p-ch input pairs in a complementary input circuit to be matched. If the g_m values are not matched each of the regions in (3.17) will hold different values. In the next section, the effects of process variation on g_m are observed. An analysis of how the dual n-ch input pair and complementary input pair behave to such variation will be explored, as it is shown in this section that variations in g_m directly affect major amplifier parameters.

3.4.4 Input Pair Analysis

It has been stated in [1-8, 12] that the g_m variation of a complementary input pair will suffer as process parameters change. This is due to the fact that n-ch and p-ch devices will vary differently as stresses are placed on the wafer. For example, as the temperature of the wafer changes, there will be variations in transistor parameters such as the threshold voltage and the mobility factor. Both the n-ch and p-ch devices have a threshold voltage and mobility factor that varies independent of one another with respect to temperature. This can give a large deviation with respect to the nominal design if a specific matching between n-ch and p-ch devices is required. It is also noted that these parameters are random variables of the process and will vary from chip to chip.

Treating transistor parameters as random variables, it can be shown theoretically how variations in process parameters will affect variations in the g_m. As mentioned in Chapter 2, a complementary input pair has three separate operating regions across common-mode inputs. There is a region where the p-ch input pair is active, a region where the n-ch input

pair is active, and a region where both input pairs are active. From this observation an expression for g_m for each operating region can be written (3.18), (3.19), and (3.20). These three expressions approximately represent how the g_m value of the input will vary with the common-mode input. The expression (3.18) corresponds to region 1 and represents when only the p-ch pair is active. Expression (3.19) represents region 2, which is when both the n-ch and p-ch input pairs are active. Expression (3.20) denotes region 3, where only the n-ch device is active.

$$\text{Region 1,} \qquad g_m = \sqrt{2 \cdot \mu Cox_p \cdot \left(\frac{W}{L}\right)_p \cdot 4I_{DQp}} \qquad (3.18)$$

$$\text{Region 2,} \qquad g_m = \sqrt{2 \cdot \mu Cox_p \cdot \left(\frac{W}{L}\right)_p \cdot I_{DQp}} + \sqrt{2 \cdot \mu Cox_n \cdot \left(\frac{W}{L}\right)_n \cdot I_{DQn}} \qquad (3.19)$$

$$\text{Region 3,} \qquad g_m = \sqrt{2 \cdot \mu Cox_n \cdot \left(\frac{W}{L}\right)_n \cdot 4I_{DQn}} \qquad (3.20)$$

Using equations (3.18) – (3.20) the effects of g_m versus process variations can be observed. By varying µCox and the widths of the p-ch and n-ch devices independently, a representation of the possible g_m effects can be observed. Figure 3-10 displays these effects for each operation region. In Figure 3-10 four separate variation tests are shown. The first includes when there are no variations in the process. Comparing all three regions, it is seen

that the variation from region to region is minimal. There is approximately a 0.1% variation

in g_m versus the common-mode input. The second test includes when there is a seven percent

variation in μCox for the n-ch and p-ch devices. In this case the deviation in g_m becomes

much larger. The variation is measured to be approximately 8.1%. The third assessment

varied the widths of the p-ch and n-ch devices by 2%. The deviation in g_m also proves to be

about 2%. The last variation test included varying both the width and the μCox of the

transistors. In this case the variation of g_m proved to be significant; with a 10.1% variation,
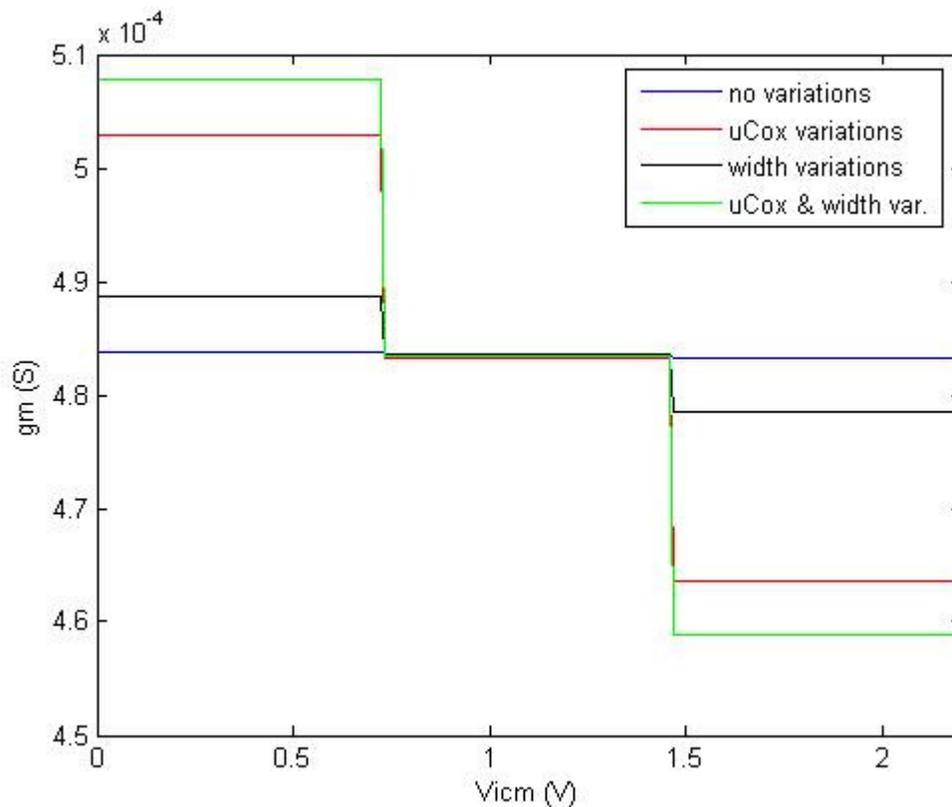
the g_m has strayed far from the nominal design.

Figure 3-10. Theoretical g_m variation for Complementary Input Pair

As seen in Figure 3-10, g_m is greatly affected by variation in the process. It is anticipated that simulation results will yield a similar outcome. Observations of equations (3.18) – (3.20) give insight to the reason why the variation becomes large as process parameters vary. In (3.18) and (3.20) it is seen that g_m is dependent on two different sets of parameters. If these parameters are varied differently as seen in Figure 3-10, the deviation in g_m becomes large. In order to create a robust input pair to these deviation effects, it is observed that each region of operation should depend on the same set of parameters which vary dependently. The solution to this problem is to use a dual n-ch or dual p-ch input pair. For this discussion a dual n-ch input pair will be considered, but it is noted that the same discussion follows for a dual p-ch input pair.

The implementation of a dual n-ch input pair also has three operating regions. There is a region where one n-ch input pair is active, a region where both n-ch pairs are active, and a region where the other n-ch input pair is active. Expressions for g_m in each region can be written and are seen in (3.21), (3.22), and (3.23). In equations (3.21) – (3.23), $I_1 + I_2 = I_{DQn}$. By performing a similar investigation to what was seen in Figure 3-10, the robustness of the dual n-ch input pair can be verified. Figure 3-11 displays the same variations test that was performed for the complementary input pair. It is seen in Figure 3-11 that the variation of g_m is unchanged. The g_m variation remains at 0.1%, just as in the no variations case. The level of g_m only shifts with the process variations.

$$\text{Region 1,} \qquad g_m = \sqrt{2 \cdot \mu Cox_n \cdot \left(\frac{W}{L}\right)_n \cdot I_{DQn}} \qquad\qquad (3.21)$$

Region 2, $\qquad g_m = \sqrt{2 \cdot \mu Cox_n \cdot \left(\dfrac{W}{L}\right)_n \cdot I_1} + \sqrt{2 \cdot \mu Cox_n \cdot \left(\dfrac{W}{L}\right)_n \cdot I_2}$ \hfill (3.22)

Region 3, $\qquad\qquad g_m = \sqrt{2 \cdot \mu Cox_n \cdot \left(\dfrac{W}{L}\right)_n \cdot I_{DQn}}$ \hfill (3.23)
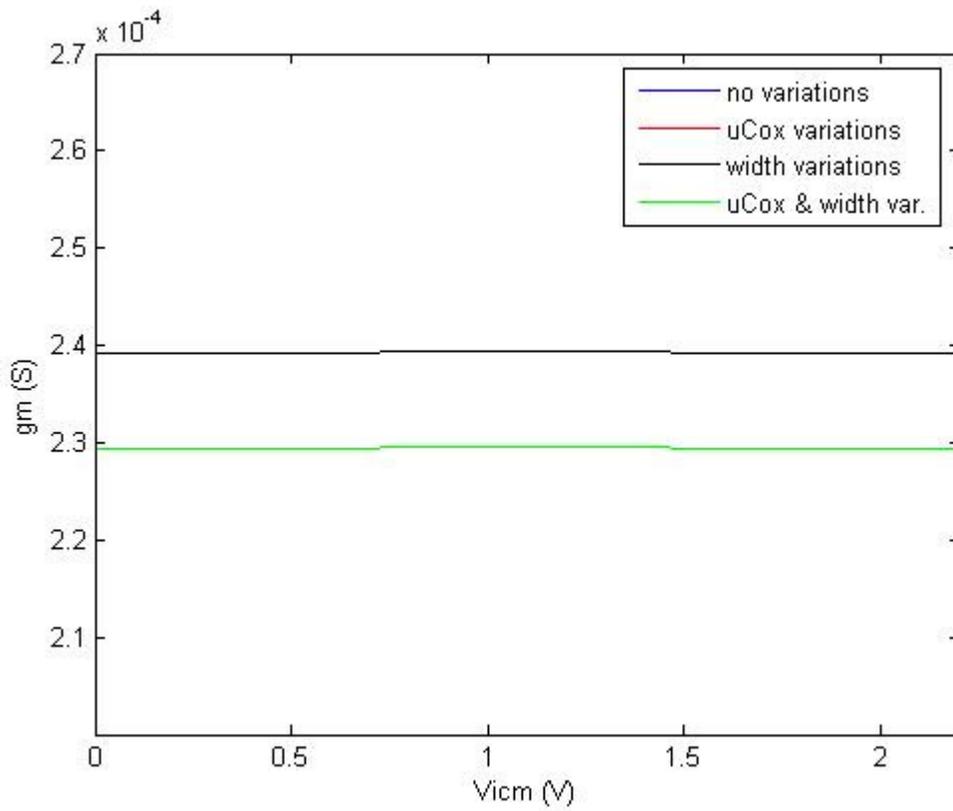

Figure 3-11. Theoretical g_m variation for Dual n-ch Input Pair

Through the observations seen in Figures 10 and 11, it has been verified theoretically that a dual n-ch input pair is more robust to process variations as expected. The model that was used for this analysis is a simple square-law transistor model, which gives an approximation of the behavior that will occur. However, the model must be verified through simulation using a higher level transistor model to confirm this behavior with better accuracy. This will be explored in the next chapter along with a comparison to the theoretical approximation.

3.5 Design Procedures

The design procedure for the operational amplifier of this work was derived from the analysis performed in the previous section. In the previous section particular limitations that the circuit architecture holds were identified and must be considered in the design of the amplifier. Transistor sizing and current allocation can be derived using analysis equations to achieve a certain performance. The design process begins with the current allocation of the amplifier stages. Next the design of the level shifter and input stage is performed. The sensing circuit was then designed. Additional design was performed for the amplifier, however in this section it is the goal to specifically present the design procedures for the innovative portions of the amplifier.

3.5.1 Current Allocation

The total design current was rationed between the first and the second stages of the design. The amount of current that was placed in the second stage was allocated to ensure

that the GBW is not limited by this stage. Since the second stage is a class-AB output, the current requirement to attain maximum GBW is reduced with respect to the size of the load capacitor. This is because for class-AB output stages the transient current can swing higher than that of the quiescent current. The current percentage in the second stage and the first stage was set to 55% and 35% respectively. This leaves 10% of the total current for biasing and common-mode feedback circuitry.

The GBW limitation of the second stage is given by g_{ms}/C_L, where g_{ms} represents the transconductance gain of the second stage, and C_L represents the load capacitor. The GBW limitation for the first stage is given by g_{mf}/C_c, where g_{mf} represents the transconductance gain of the first stage, and C_c represents the compensation capacitor. To ensure that GBW is maximized the current is allocated between the first and second stages such that $g_{mf}/C_c = 4*g_{ms}/C_L$, where it is assumed that $C_L \approx 5*C_c$. It is also assumed that the class-AB transient current can swing approximately four times the quiescent current. Hence, to achieve the equality $g_{mf}/C_c = 4*g_{ms}/C_L$ the current in the second stage should be slightly larger. The ratio of current in the first and second stages which was given was chosen to satisfy this equality.

3.5.2 Level Shifter Design

As seen in section 3.4, there are some limitations on the level shifter which must be considered during its design. The main limitation that was considered was the appearance of an additional pole in the signal path. This pole can create undesirable variations in the phase margin as well as the GBW when the input pair attached to the level shifter is active. So it is

important to design the level shifter such that this additional pole does not have a negative

effect on the amplifier performance.

In equation (3.10), the relative location of the additional pole created by the level

shifter is given. In order for the pole to have minimal effect on the circuit's performances, it

is important to design this pole to be at a frequency about 20-30 times the GBW of the

amplifier. This is to guarantee that the effective phase delay from the additional pole is not

seen at the operating frequency of the amplifier. To increase the pole frequency of the level

shifter, (3.10) suggests that the g_m can be increased, or that the C_L and C_{GS} should be

decreased. Assuming that C_L is fixed and $C_L \gg C_{GS}$, to increase the frequency of the pole,

g_m must be increased. To increase g_m, the current in the level shifter and/or the size of the

level shifter can be increased.

Now assuming that the g_m of the level shifter has been maximized, where it still holds

true that $C_L \gg C_{GS}$, the C_L of the level shifter should be minimized. The dominate

contributor to C_L of the level shifter is the C_{GS} of the input pair. This implies that the input

pair sizing must also be considered in the design of the level shifter. The C_{GS} of a transistor

is given by (3.24). In (3.24) it is seen that the C_{GS} of the input pair is directly related to the

area of the transistors. Thus to minimize C_L the input pair sizing should be limited.

$$C_{GS} = \frac{2}{3}WLC_{ox} + WL_{OV}C_{ox} \qquad (3.24)$$

For the complete design of the level shifter there are three considerations that should be made. The first includes determining what the GBW of the complete circuit will be. This gives insight about where the pole of the level shifter must lie. The second consideration for the level shifter design includes finding an optimal current allocation and sizing to maximize g_m and maintain $C_L >> C_{GS}$, where C_{GS} represents the C_{GS} of the level shifter. This is done for some initial sizing for the input pair. Last, the C_{GS} of the input pair should be minimized. This will decrease the C_L on the level shifter. However, the sizing of the input pair has a lower bound as the gain of the amplifier depends on the input pair size. An optimal solution can be found from these three design considerations for the level shifter.

3.5.3 Sensing Circuit

The design of the sensing circuit also corresponds with the design of the level shifter. This is because a portion of the sensing circuit is also attached to the level shifter and will increase the value of C_L. For this reason the sensing circuit input pair is sized to be a fraction of the regular input pair. The sensing circuit input pair should be sized to be approximately 1/8 – 1/10 the size of the amplifier input pair. This ensures that the C_{GS} of the sensing circuit has a small contribution to the C_L of the level shifter.

It is also important that the design sensing circuit input pair be a ratio of the input pair. The sensing circuit should also have the same ratio of current flowing through it. This is done to maintain a consistent common-mode sensing. If the sensing circuit input pair is a ratio of the amplifier input pair, with the same ratio of current, the manner in which the common-mode affects the sensing input pair should be the same as that of the amplifier input

pair. This allows for an accurate control of the variable tail current source on the shifted

input pair.

CHAPTER 4. RESULTS AND MEASUREMENT

4.1 Introduction

A discussion of the amplifiers simulated results is given in this chapter. It will be shown that the amplifier specifications that were the goal of the design were obtained. This chapter will first present the simulated results including the level shifter response, constant parameters versus V_{icm}, and other typical amplifier specifications. The discussion will then move on to the evaluation and comparison of this design versus other rail-to-rail constant operation designs. The comparison will include how well this design holds amplifier parameters constant with respect to published designs. The last portion of this chapter includes a process robustness comparison, which evaluates the robustness of the dual n-ch input pair to the complementary input pair. This simulation is then matched up against the analytical results presented in Chapter 3.

4.2 Simulation Results

4.2.1 Level Shifter Response

The location of the level shifter's dominant pole is extremely important to the amplifier's performance. As discussed in Chapter 3, if the pole is not placed at a sufficiently high frequency, the phase delay of the level shifter will affect the output of the amplifier. Figure 4-1 displays the simulated gain and phase results of the level shifter. The figure

shows that the bandwidth of the level shifter, which is approximately the location of the

dominate pole, is found at 509MHz. In the figure the phase delay of the level shifter at the

amplifier's GBW is also labeled. At the amplifier's GBW the phase delay of the level shifter

is seen to be 1.43 degrees. This implies that the phase delay of the level shifter will have

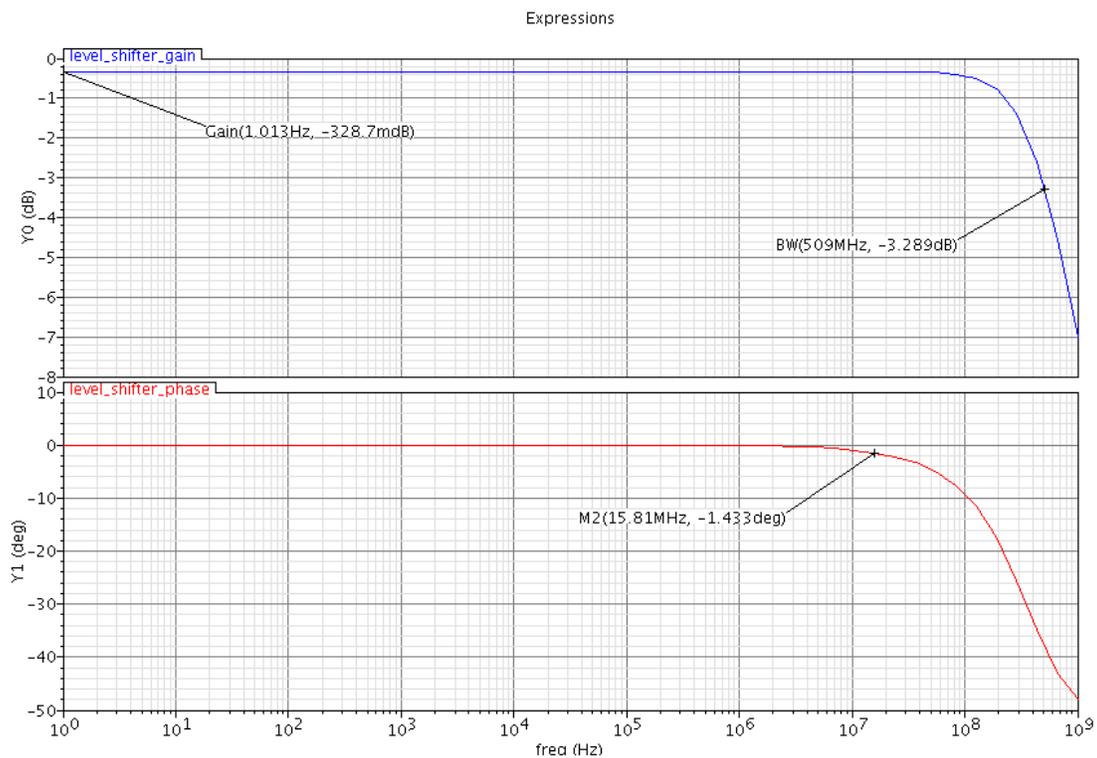minimal affect on the amplifier's constant performance when it is in operation.

Figure 4-1. Level Shifter Gain and Phase Response

4.2.2 Constant Parameters versus V_{icm}

The argument of obtaining constant g_m has been one of the main foci of this design,

as constant g_m allows for other amplifier parameters to be kept constant. Figure 4-2 displays

a plot of g_m versus the common-mode voltage. It is seen that there is minimal deviation in

g_m, with a deviation of about 6%. The figure proves that a dual n-ch input pair can be used to obtain a constant g_m comparable to that of other implementations.
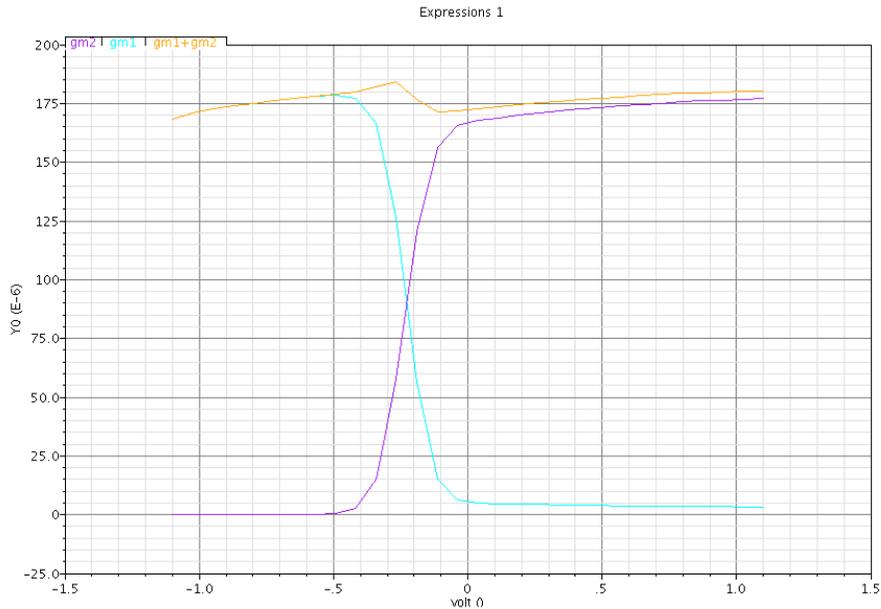

Figure 4-2. g_m versus V_{icm}

In Figure 4-3 a display of several amplifier parameters versus V_{icm} is given. Figure 4-3 displays the DC gain, cascode stage current (Ic), GBW, and PM. In the figure, Ic, the cascode stage current corresponds to the output g_o of the first stage, which affects the first stage gain as discussed in Chapter 3. Recall that this current is kept constant by the sensing circuit and variable tail current source. It is seen that each of the parameters in Figure 4-3 has minimal variation. A summary of the parameters in Figure 4-3 with their corresponding variations can be seen in Table 2.
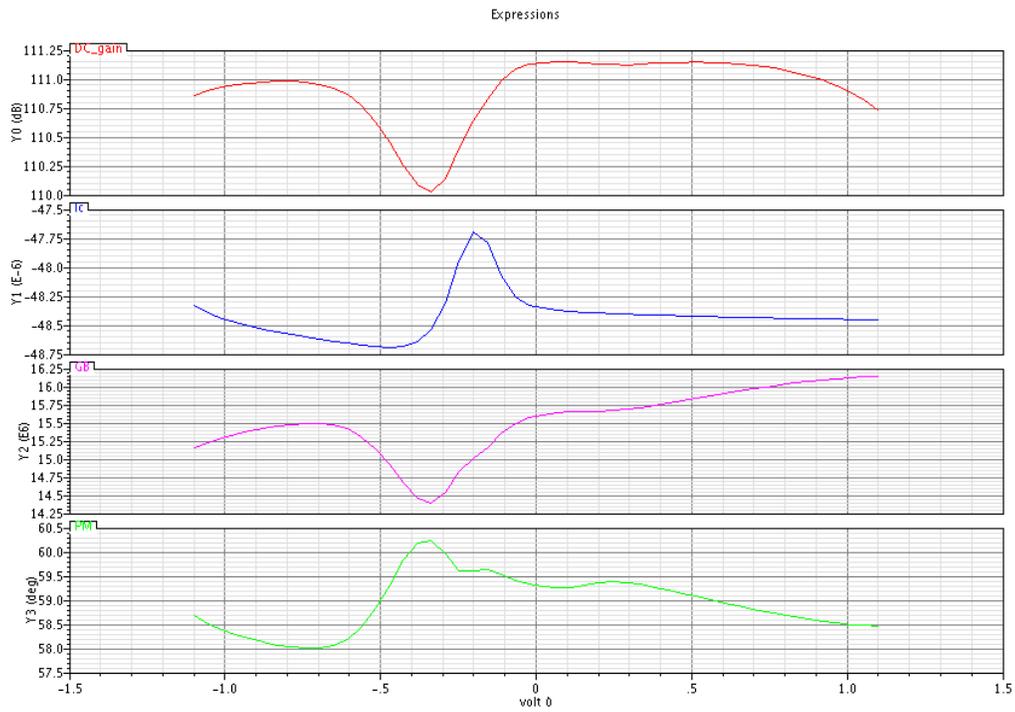
Figure 4-3. Amplifier Parameters versus V$_{icm}$

Table 2. Amplifier Parameters and Variations versus V$_{icm}$

Specification	Value	Percent Variation
g$_m$	177 uS	6%
DC gain	111 dB	1%
GBW	15.6 MHz	9.3%
PM	59.2°	3.3%
Cascode Stage Current	48.3 mA	1.7%

4.2.3 Amplifier Frequency and Transient Response

An extension of the information seen in Figure 4-3 is displayed in Figure 4-4. Figure

4-4 gives the frequency magnitude and phase response of the amplifier for three different

common-mode levels. This test was performed in open-loop configuration. It is seen that

the response has minimal variation in the operating region of the amplifier (below GBW).

The cause of variations past GBW are due to the level shifter, as the dominant pole of the

level shifter becomes troublesome at these frequencies. Figure 4-4 gives the approximate DC
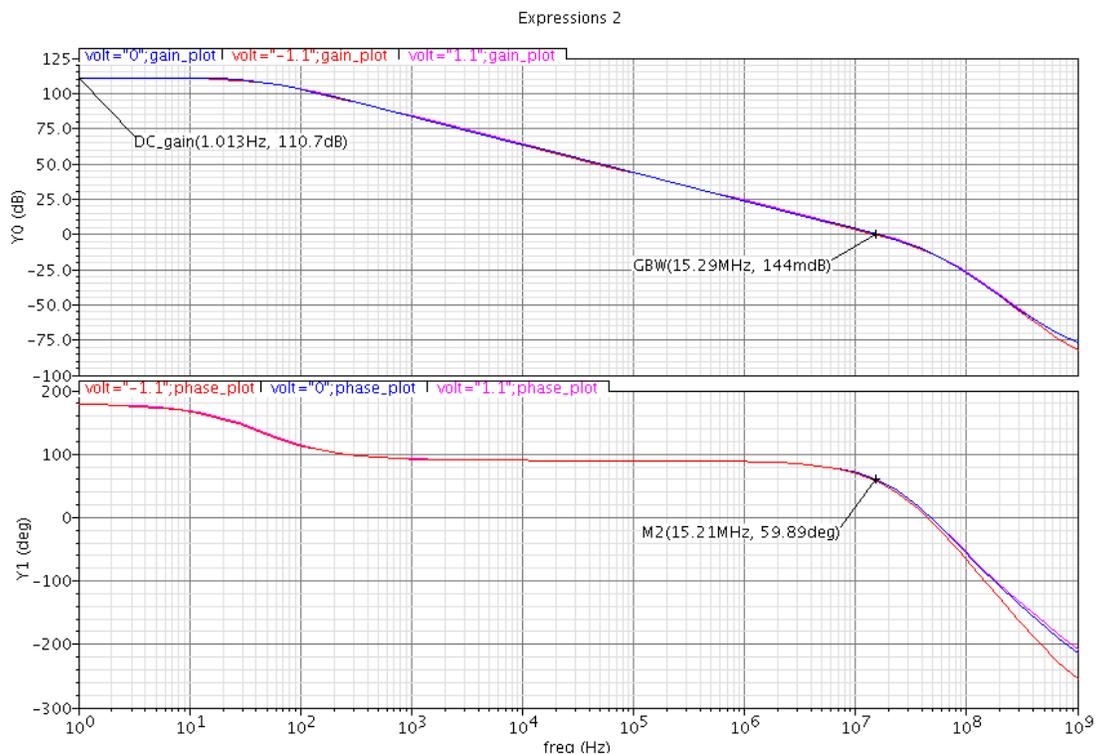
gain, GBW and PM of the amplifier.

Figure 4-4. Amplifier Magnitude and Phase Response vs. Frequency

A closed loop transient response of the amplifier is seen in Figure 4-5. The amplifier

was placed in a unity gain, negative feedback configuration. Different input signal levels

were fed to the amplifier and the resulting output is what is seen in Figure 4-5. The purpose

of Figure 4-5 is to display that the amplifier has a rail-to-rail output swing capability. It is

seen in Figure 4-5 that the amplifier saturates about 50mV from the supply rails, which
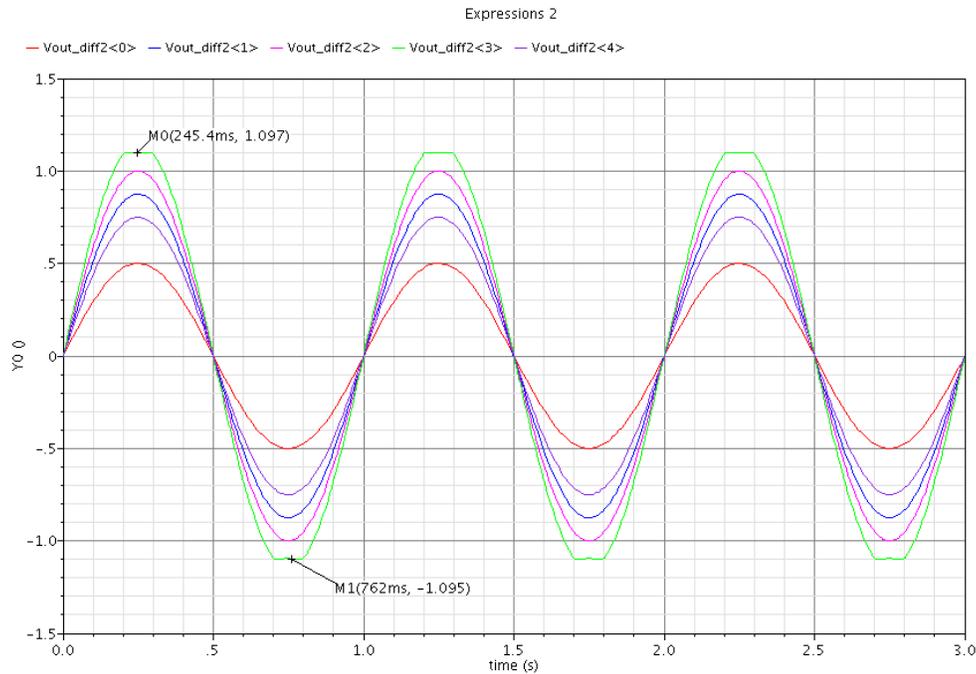
implies a near rail-to-rail output.

Figure 4-5. Closed-Loop Transient Response

4.2.4 Amplifier Parameters vs. Temperature

A summary of the amplifier's parameters is given in Table 3. The table displays

typical specifications used to characterize amplifiers. These specifications are given at three

different temperatures. The specifications given in Table 3 were tested using typical test

circuits found in the literature.

Table 3. Amplifier Specifications versus Temperature

Specifications	-25C	50C	100C
DC gain (dB)	113	110	106
GBW (MHz)	22.23	13.9	10.83
PM (degrees)	59.46	57.62	53.87
Power Consumption (mW)	0.669	0.605	0.578

4.3 Evaluation and Comparison

In this section a comparison of this work's amplifier performance to other

implementations is given. For the first section of comparisons, other input stage

implementations were designed in the AMI 05 process and were then substituted as the input

stage for the amplifier of this work. Using this comparison strategy an evaluation of how

well constant parameters are kept due to the input stage is explored. The last section of

comparison gives a comparison of the complete amplifier versus amplifiers in the literature.

Typical specification are compared and evaluated.

4.3.1 Constant Parameters

Figure 4-6 and Figure 4-7 give a comparison of the Vin versus Vout DC sweep for

two different input pairs. Figure 4-6 shows a Vin versus Vout sweep for four different

common-mode levels for a dual n-ch input pair. Figure 4-7 displays the same information,

however for a complementary input pair. In Figure 4-6, it is seen that for each of the

common-mode levels, the change in the curve is small. This implies that there is a constant

gain for this implementation, as the slope of the curve corresponds to the gain of the

amplifier. However, in Figure 4-7 the gain has greater deviation. Thus the complementary

pair does not have an operation that is as constant as that of the dual n-ch input pair.
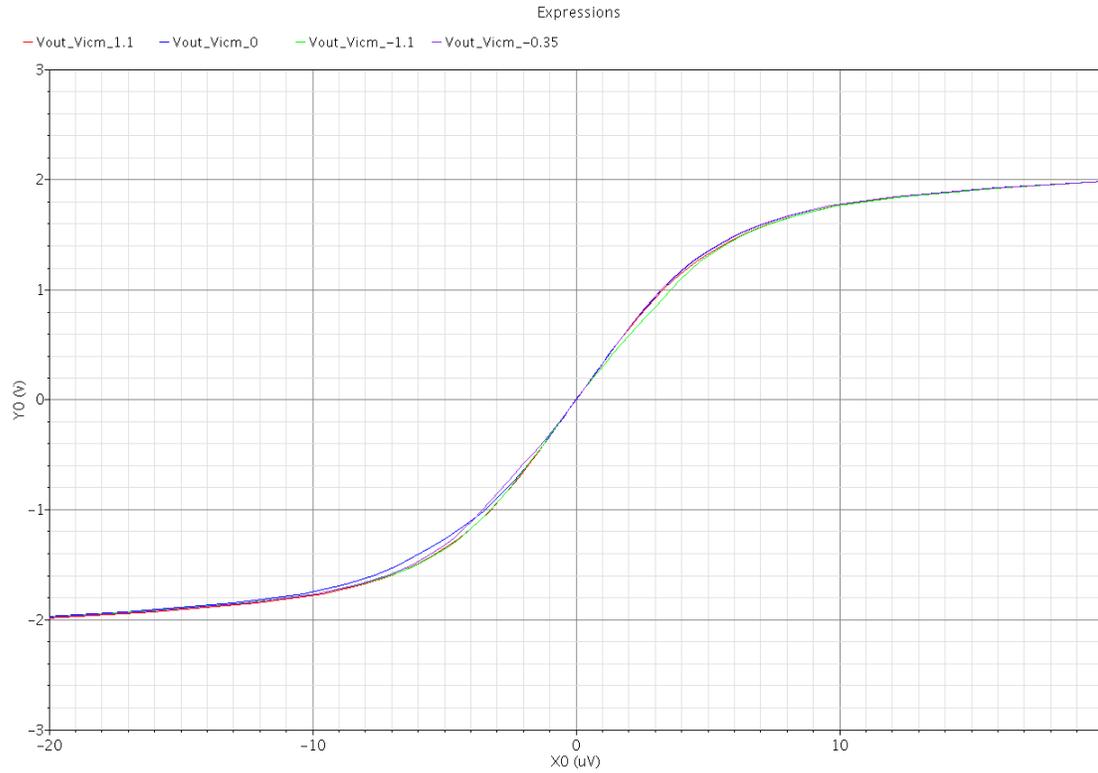

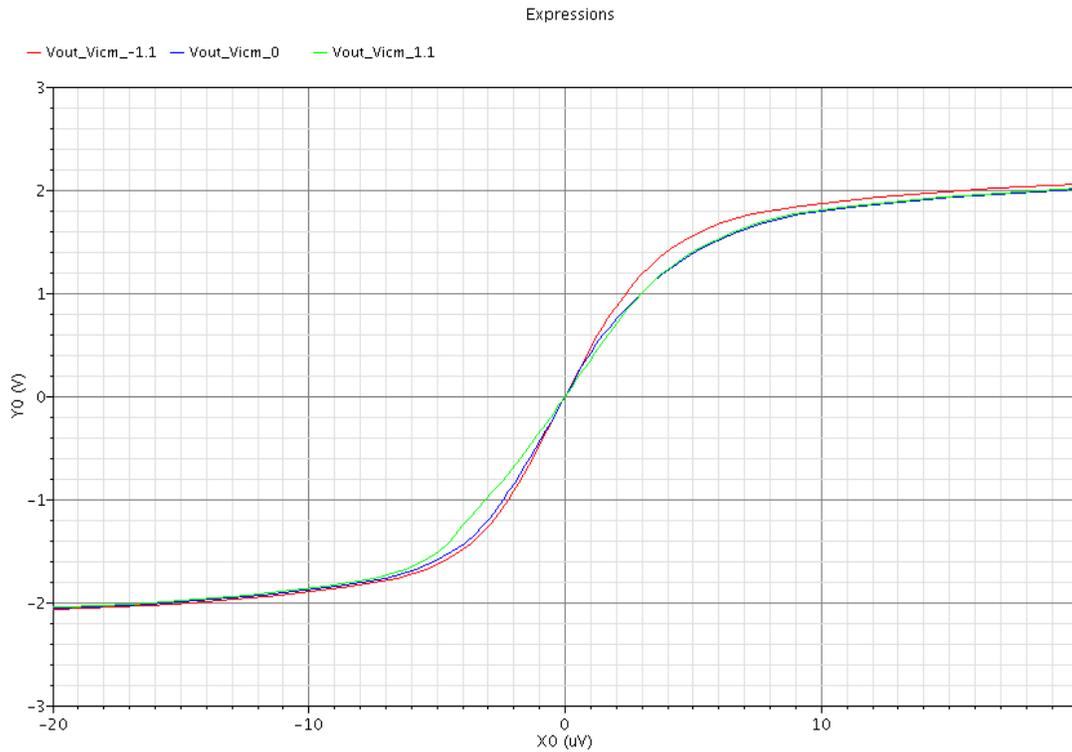**Figure 4-6. Vin versus Vout Sweep of Dual n-ch Input Pair**

Figure 4-7. Vin versus Vout Sweep of Complementary Input Pair

4.3.2 Amplifier Specifications

A comparison of the simulated results of this amplifier to others in the literature is

seen in Table 4. The findings in Table 4 are similar to results displayed in Table 2 .

However, in Table 4 the actual results of the amplifier are given, whereas the specs in Table

2 were goals of the design. It is observed that the majority of the goals of the design were

achieved and the performance of the amplifier of this work is comparable to those in the

literature. The conclusion of the results seen in Table 4 implies that there are no negative

effects due to the input stage of the amplifier implemented with respect to typical amplifier

specifications.

Table 4. Amplifier Specification Comparison

Specification	[9]	[5]	[14]	[7]	This Design
Input Stage	Duel n-ch pair	Complementary input pairs with overlapped transition regions	Duel p-ch pair	Complementary input pair	Duel n-ch pair
Supply Voltage (V)	3	3	1	3	2.2
Process (um)	0.8	1.2	0.065	1	0.5
Power Consumption (mW)	4.8	0.31	0.72	9	0.6
Gain A_v (dB)	95.1	113	100	85	111
Phase Margin (°)	60	>45	64	66	59
GBW (MHz)	17.5	5.5	40	2.6	15.6
Capacitive Load C_L (pF)	15	10	15	10	15
Figure of Merit (GBW*C_L / P)	54.68	177.419	833.33	2.89	390

4.4 Process Robustness Comparison

In Chapter 3, a theoretical analysis of the performance for a complementary input pair and a dual n-ch input pair versus process variations was given. In this section, the simulated analysis is presented. Recall that Chapter 3 displayed large variations for the complementary

input pair versus process variations and that the dual n-ch input pair displayed no variation. It is seen that similar results are given from simulations as observed in Figure 4-8 Figure 4-9.

Figure 4-8 displays the variation of g_m versus V_{icm} for a dual n-ch input pair at different process corners. Similar to the results seen in Chapter 3 the variation has minimal change at each process corner. The level of the g_m curve is the only part of the graph that is changed. A summary of the g_m variation due to each process corner is seen in Table 5. It is seen that the g_m variation for the typical process parameters is 7%, and for the worst case the variation becomes 11.4%. This implies that the variation of g_m should fall within 3% of the nominal design.
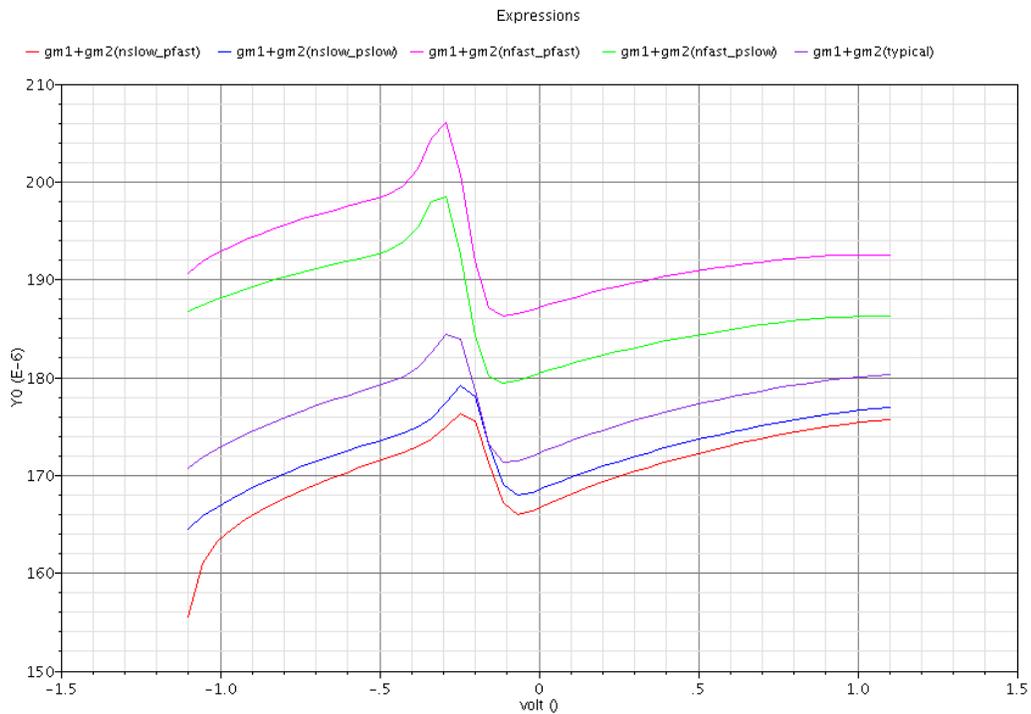

Figure 4-8. Dual n-ch Input Pair, g_m versus V_{icm} at Process Corners

Table 5. Dual n-ch g_m Variation

Corner	g_m Value	Variation
Typical	176 uS	7%
nslow_pfast	170 uS	11.4%
nslow_pslow	172 uS	8.4%
nfast_pfast	186 uS	9.7%
nfast_pslow	194 uS	9%

In Figure 4-9 the variation of g_m versus V_{icm} for a complementary input pair at different process corners is seen. Just as seen in Chapter 3, the robustness of this input pair implementation is poor. It is seen in Figure 4-9 that the shape of the curve changes at different process corners. The variation increase at different corners as summarized in Table 6. For the typical case the variation of g_m is 10%, but for the worst process corner, the variation of g_m is 18%. This implies that the variation of g_m should fall within 8% of the nominal design.
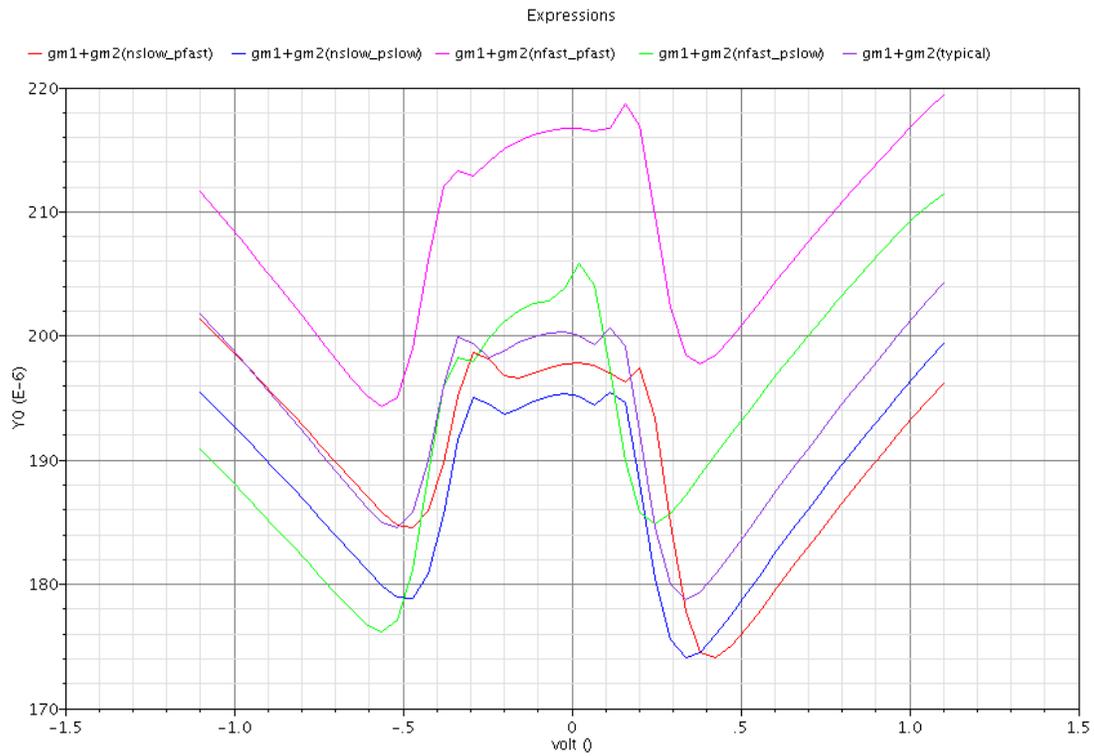
Figure 4-9. Complementary Input Pair g$_m$ versus V$_{icm}$ at Process Corners

Table 6. Complementary Input g$_m$ Variation

Corner	g$_m$ Value	Variation
typical	195 uS	10%
nslow_pfast	189 uS	13.9%
nslow_pslow	185 uS	12.6%
nfast_pfast	207 uS	11.8%
nfast_pslow	194 uS	18%

The observations of Figure 4-8 Figure 4-9 as well as Table 5Table 6 prove that a dual n-ch input is more robust to process variations compared to a complementary input pair. It is seen that for the worst case the variation of g_m can be 3% different from the nominal design for the dual n-ch input pair. For the complementary pair it is seen that the g_m variation can be different by nearly three times that of the dual n-ch input for the worst case. These results echo what was seen in Chapter 3 and thus the analysis that was performed is viewed as accurate.

CHAPTER 5. SUMMARY AND DISCUSSION

5.1 Introduction

The final conclusions and design discussions of the implementation present in this work is reviewed in this chapter. A further discussion of the implementation issues not covered in previous chapters will be given as well as limitations of the design that result. The issues that are discussed point towards further research that could be explored to improve the design presented. The remainder of the chapter identifies successful innovative techniques that were presented and draws conclusions for the overall design.

5.2 Implementation Issues/Performance Limitations

During the design process there were a few implementation issues that arose unexpectedly which exposed the limitation of the design. The main issues were discussed in Chapter 3 and possible design procedures were given to overcome these problems. However, the design procedures given may not be the optimal solution to compensate for these issues as this was not the main focus of this work. In this section some implementation issues will be revisited and alternate schemes will be given to overcome these problems.

5.2.1 Level Shifter

The dominant pole of the level shifter is one problem that was discussed in Chapter 3. It was described that if there is no sort of compensation for the effects of this pole, there will be phase degradation in the amplifier as a result. Chapter 3 mentioned two possible methods to eliminate the effects of the level shifter pole. The first was to push the pole to a

sufficiently high frequency. The design procedure was also given for this method. The second was to move the pole and zero of the level shifter closer together to minimize phase delay. Each of these methods serves the purpose of minimizing the effects of the level shifter; however each of the methods has costly limitations that have not yet been overcome.

Pushing the pole to a sufficiently high frequency was the technique presented in Chapter 3. The design procedure given will yield the minimization of this problem; however this technique may become power inefficient. In Chapter 3 it was noted that in order to push the level shifter pole to a high frequency, the value of C_L should be decreased and the value of g_m of the level shifter should be increased. For C_L to be decreased, the size of the input pair should be decreased. There is a limitation on how much the input pair can be decreased because the gain of the amplifier will decrease as a result.

To increase the value of g_m for the level shifter, the width and length ratio can be increased or the current in the level shifter can be increased. It was observed that there is also a limit on how large the level shifter can be, because as the size of the level shifter increases, the drain-to-source capacitance (C_{DS}) will also increase. This is not desirable because it will cause the value C_L to increase. Thus the sizing for the level shifter is limited and must satisfy that C_{DS} of the level shifter is much less than C_{GS} of the input pair. This leaves increasing the current in the level shifter as the last pole frequency maximization technique. During the design process it was seen that the amount of current needed to increase the level shifter pole to a sufficiently high frequency was not an efficient use of power. Nearly twice the current in the first stage needed to be used in the level shifter. This

implies that this method may not be the most efficient technique and leaves the possibility for more research for a more suitable level shifter implementation.

The other technique mentioned in Chapter 3 that was explored was the method of moving the level shifters pole and zero closer to one another. This is achieved by increasing the C_{GS} of the level shifter. The most efficient way to implement this technique is to add a capacitor across the gate and source of the level shifter. This will cause the phase of the level shifter to have minimal variation across the frequency range of interest. A display of the gain and phase of a level shifter with an increased C_{GS} is seen in Figure 5-1. The phase degradation is seen to be less than 1 degree.
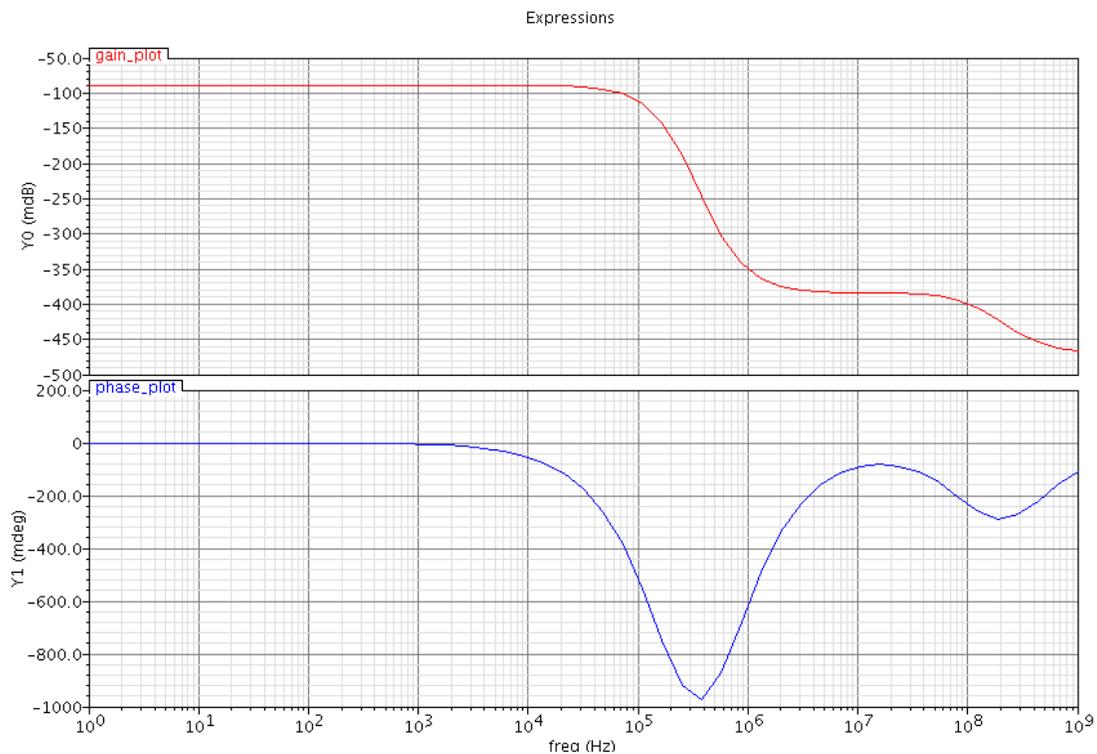

Figure 5-1. Level Shifter Output with Increased C_{GS}

The limitation of this technique is the capacitor size needed to produce such results. For this design the capacitor used to produce the results seen in Figure 5-1 is a 2pF capacitor. This will cause the input capacitances of the amplifier to also be large. Thus, an optimal solution for the issues related to the level shifter has not been found. This allows for opportunities for further research to improve the efficiency of the amplifier present in this work.

5.2.2 Tail Current Variation

Another issue that was observed during the implementation of this design was the need for cascoded tail current sources. It was seen that as the common-mode of the input was varied, the V_{DS} of the tail current would also change significantly. This caused the current of the tail current source to change as a result. When there are variations in the tail current source with the common-mode input, this causes variations in the performance of the amplifier as well. To resolve this problem cascoded tail current sources had to be added. This allows for the value of the current to be less dependent on the V_{DS} across the tail current source. A better variation performance was observed as a result.

The latter implementation issue is mentioned because it is noted that as the voltage of the amplifier is decreased, using a cascoded tail current source may not be practical. Thus for lower voltage designs, the variation that was achieved through this design may not be possible with the use of the same process. Future work can explore how to ensure that there are minimum variations in the tail current source without cascoding. This will allow the

amplifier given in this work to be designed at lower voltages without the use of a lower feature size process.

5.3 Conclusions

In this work a presentation of a low voltage, constant operation, rail-to-rail operational amplifier was given. The idea of constant operation in this work is depicted as holding specifications such as gain, gain-bandwidth product, phase margin, slew rate, and power consumption constant across the entire common-mode range. To hold these parameters constant, previous work typically focused on keeping g_m constant. However, in this work, in addition to holding g_m constant, the output conductance g_o of the first stage is also held constant. This allows for a more constant operation as needed for lower voltage applications.

The idea of keeping g_o constant also opens the possibility of implementing gain boosting techniques in the amplifier design. This can prove to be useful when the amplifier design is implemented in lower feature size processes, where higher gains become more difficult to achieve. Also, as the voltage is decreased the amount of tolerable variation in amplifier parameters is also decreased. The implementation of this work gives an acceptable variation performance for lower voltage usage. The design presented in this work has the additional advantage of its process robustness compared to other implementations. This work has proved to be an innovative design that will allow for further optimization in low voltage operation amplifier designs.

CHAPTER 6. SUPPLEMENTARY MATERIAL H-BRIDGE DAC DESIGN

6.1 H-Bridge Functionality

The basic H-Bridge structure (seen in Figure 6-1) is comprised of 4 switches which regulate the current flow through a given load. The structure is configured in such a way to allow the current driven through the load to be steered in both directions, which is achieved by only closing two diagonal switches at a time. This allows for the voltage across the load to hold both positive and negative polarities. The primary use of the H-Bridge seen in the literature is in power driving applications. This is seen in [17-20].
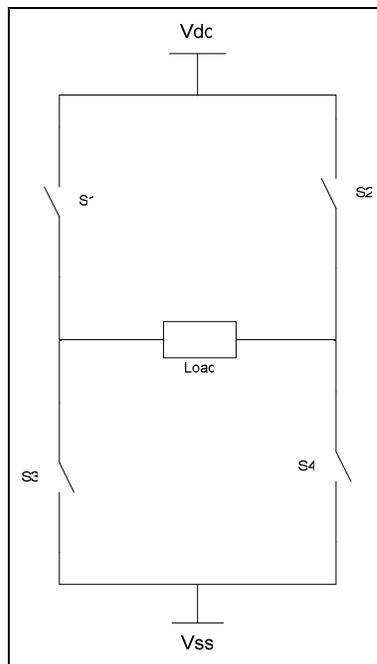

Figure 6-1. Basic H-Bridge Structure

In [19] an active voltage source rectifier which incorporates an H-Bridge configuration is presented. This structure serves the purpose of limiting negative influences on the line power-quality of the system. In the paper an optimal control algorithm for a cascaded H-Bridge structure to achieve maximum power-quality is given. Similarly, [18] presents a set of equations for determining an optimal voltage ratio of DC voltages for H-Bridge cells to give maximum power-quality. This paper also explores cascading H-Bridge cells with an optimal power-quality and a minimum number of DC levels.

6.2 H-Bridge Structure as a DAC

A less common explored application of the H-Bridge structure includes its uses as a digital-to-analog converter (DAC). If the structure is examined, it can be seen that if additional branches are added, the output can take on many different signal levels. For example in Figure 6-2, the H-Bridge structure is implemented with two additional branches on each end of the basic structure. Each branch is attached to a voltage source of a different magnitude which allows the output across the load to take on several different voltage levels. The implementation seen in Figure 6-2 has a total of 8 different output levels which is equivalent to a 3-bit DAC. It is observed that as devices are added to the structure, along with different voltage sources, the number of levels will increase as given by (6.1), where D is the number of devices and L is the number of levels. The relationship between the number of devices and the resolution n for the H-Bridge is given by (6.2). A summary of the number of devices in relationship with the possible number of levels and resolution achievable can be seen in Table 7.

$$L = \frac{D^2}{2^3} \qquad\qquad (6.1)$$

$$D = 2^{\frac{n+3}{2}} \qquad\qquad (6.2)$$

In Table 7 it is seen that with an increase in the number of levels the structure becomes considerably more expensive as the number of devices and voltage sources needed increases considerably. It is less desirable to have the number of devices in a DAC structure increase exponentially as a function of the resolution. For example, in an R-String or thermometer coded current steering DAC, the amount of devices needed increases as a function of 2^n with the resolution. The H-Bridge structure implemented as a DAC will have a device count which increases much less than that of the R-String or thermometer coded current steering DAC with respect to the resolution as seen in (6.2). At first inspection this seems to be an attractive feature. However, because of the need for independent voltage sources for each device added, a higher resolution H-Bridge DAC seems less practical. This implies that for the use of digital-to-analog converter applications, the H-Bridge structure likely should be used as a lower resolution part.

Table 7. H-Bridge Device to Resolution Relationship

Devices (D)	Levels (L)	Resolution (n)
4	2	1 bit
8	8	3 bit

16	32	5 bit
32	128	7 bit
64	512	9 bit
128	2048	11 bit

To increase the effective resolution of the H-Bridge DAC, some sort of modulation would be necessary in a previous stage. For example, if the H-Bridge structure was driven from a $\Sigma\Delta$ modulator or a pulse width modulator, the effective resolution would be increased. This however is a topic left for discussion after the feasibility of the H-Bridge structure as a DAC is verified.

As seen in references [17, 20] the H-Bridge commonly is used in high voltage applications. If the structure is to be used as a DAC, using high voltages would not be feasible and thus the H-Bridge structure must be explored to meet the requirements for lower voltage operations. Particular design techniques and architectures are not applicable to both high voltage and low voltage designs [21]. For this reason the H-Bridge structure was explored for its feasibility in lower voltage application.
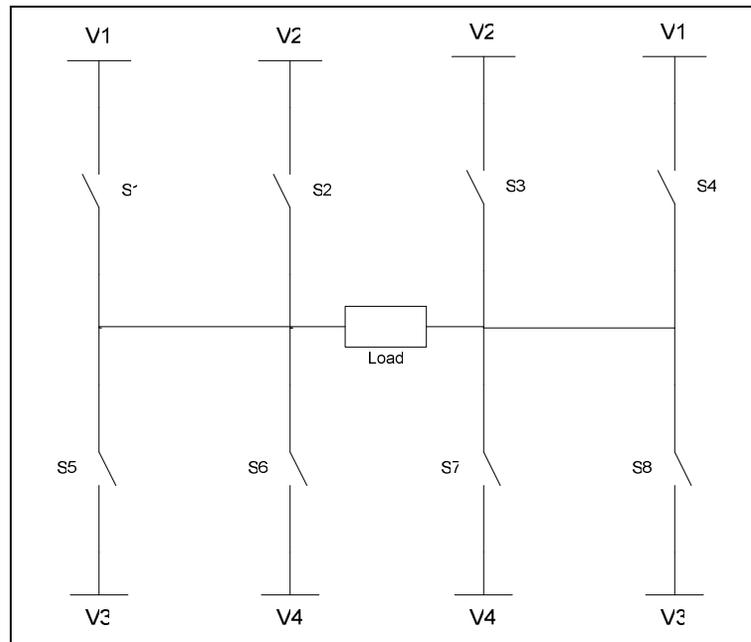
Figure 6-2. Ideal 3 bit H-Bridge DAC

When examining the H-Bridge structure in lower voltage applications, the first and most obvious potential problem is the issue of not having ideal switches in the implementation. The switches are usually implemented with metal oxide semiconductor (MOS) transistors which will have a particular resistance based on its gate drive, drain-source voltage and current, dimensions, etc. The non-ideal switch impedances associated with the H-Bridge structure are only troublesome at lower voltages. At high voltage operation the voltage drop that will occur as a result of the switch impedance can be neglected. But for lower voltage applications; if this problem is not compensated, the H-Bridge DAC implementation will experience poor linearity, which is due to the different voltage levels to which the switches are attached. An alternate switch may need to be explored to overcome this limitation.

6.3 Low Voltage Complications

6.3.1 Switch Impedances

The switch impedances were seen as a non-linear variation in the architecture. These will be troublesome in the final design, and will limit characteristics such as total harmonic distortions (THD) and spurious free dynamic range (SFDR). The use of a single MOS transistor was the current implementation for the switches in the structure. Due to the operation of the architecture, this type of switch implementation will always have a non-linear variation with the output voltage level if a constant gate drive is applied. This is due to the different current values flowing through each branch of the DAC and the variation of the drain to source voltage with each output level. To compensate for this non-linear variation, the gate drive of each switch would have to be tuned in addition to sizing each switch with a high level of precision. The issue about compensating for varying switch impedances has been explored in the literature for DAC design. However, a technique that was applicable to this architecture was not found, and for that reason a new switch implementation was considered.

6.3.2 New Switch Implementation

The desired specifications for a new switch implementation include a low on resistances as well as a constant voltage drop regardless of the current. The first switch implementation considered was a super source follower seen in Figure 6-3. This circuit is usually used a buffer in other applications, but seemed to have the potential to act as a

switch. The small signal analysis of this circuit suggests that this part would have a low on

resistance which could be controlled dominantly by the size of M1. Also, this circuit should

give a constant Vgs drop from the input to the output of the switch. The intended operation

for this switch is seen in Figure 6-4. The switch ideally should have a constant Vgs drop

with little output resistance.

The output resistance for the super source follower was derived and is seen in

equation (6.3). This equation uses the small signal parameters of the device to characterize

the output impedance, and as it appears, it should operate as an improved switch needed for

the design. However, upon further investigation it was seen that the small signal parameters

do not characterize the super source follower's behavior as a switch well. This was also

verified through Cadence simulations. The main issues that were observed with this switch

included its load driving capabilities and current limits. In the DAC design the switches will

need to drive a small resistive load as well as large currents. This implementation proved not

to be capable of this task and thus was not further researched.

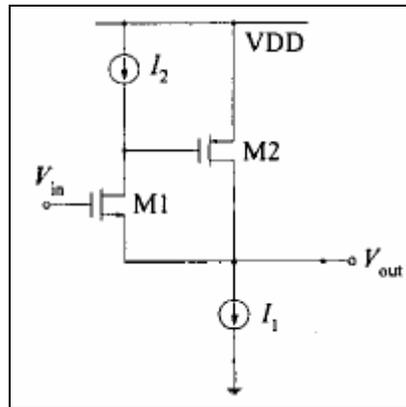$$r_{out} = \frac{1}{g_{m1}\left(r_{o1}g_{m2}+1\right)} \tag{6.3}$$
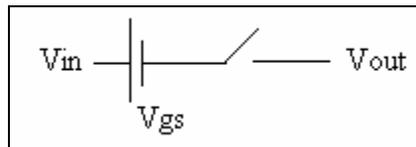
Figure 6-3. Super Source Follower

Figure 6-4. Source Follower Implementation

The second switch implementation was a flipped source follower seen in Figure 6-5. Similarly to the super source follower, this circuit is often used as a buffer circuit. A similar analysis was performed to analyze the output resistance of this switch. Upon inspection, this switch implementation also seemed to have a low tunable output resistance. The switch was again analyzed in Cadence to verify that the analysis would hold true. This implementation experienced a better switch performance then that of the super source follower; however, there were other issues that arose that made this switch impractical.

The first problematic issue experienced with the flipped source follower was turning the switch completely off. The ideal operation of the switch allows for the switch to be

controlled from the gate terminals V+ and V-. The control transistors are designed to steer

the current through one branch of the circuit (the circuit is symmetric, other half not drawn).

However, upon testing the switch, this was not the case. The switch would not completely

turn off when the current was steered to the complementary branch. This was due to the

control of the top p-ch transistor; because this transistor is not completely turned off the

switch will still output a current. A revision of this implementation was considered, however

the results of this revision are still under investigation. The final investigation of this switch
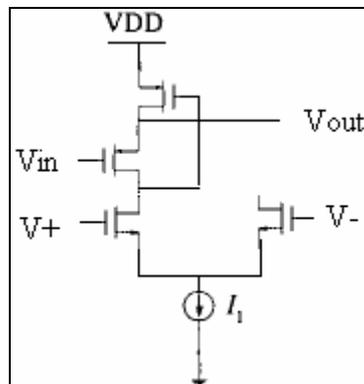
is left for further research.

Figure 6-5. Flipped Source Follower

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