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Dual-frequency dual-inductor multiple-outputs (DF-DIMO) buck converter topologies with fully-integrated output filters

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Dual-frequency dual-inductor multiple-outputs (DF-DIMO) buck converter topologies

with fully-integrated output filters

by

Yongjie Jiang

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Ames, Iowa

2016

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<tr>
<td>DSP</td>
<td>Digital Signal Processor</td>
</tr>
<tr>
<td>SIMO</td>
<td>Single-Inductor Multi-Output Power Converter</td>
</tr>
<tr>
<td>DIMO</td>
<td>Dual-Inductor Multi-Output Power Converter</td>
</tr>
<tr>
<td>DF-SIMO</td>
<td>Dual-Frequency SIMO</td>
</tr>
<tr>
<td>DF-DIMO</td>
<td>Dual-Frequency DIMO</td>
</tr>
<tr>
<td>LDO</td>
<td>Low Drop-Out Power Converter</td>
</tr>
<tr>
<td>SC</td>
<td>Switched Capacitor Power Converter</td>
</tr>
<tr>
<td>DVS</td>
<td>Dynamic Voltage Scaling</td>
</tr>
<tr>
<td>MEC</td>
<td>Multiple inductor Energizing/de-energizing Cycle</td>
</tr>
<tr>
<td>SEC</td>
<td>Single inductor Energizing/de-energizing Cycle</td>
</tr>
<tr>
<td>DCM</td>
<td>Discontinuous Conduction Mode</td>
</tr>
<tr>
<td>CCM</td>
<td>Continuous Conduction Mode</td>
</tr>
<tr>
<td>PCCM</td>
<td>Pseudo Continuous Conduction Mode</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>DCR</td>
<td>Direct Current Resistance</td>
</tr>
<tr>
<td>ACR</td>
<td>Alternating Current Resistance</td>
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ABSTRACT

In multi-core DSPs, there is a need for multiple independent power supplies to power the digital cores. Each power supply needs to have fast dynamic response and must support a wide range of output voltage with up to hundreds of mA load current. In this dissertation, the key performance metrics in power converter design are introduced, the advantages and disadvantages of the conventional power converter topology are analyzed and a new Dual-Frequency Dual-Inductor Multiple-Output (DF-DIMO) buck converter topology is presented to improve the limitations of the conventional topologies. The proposed topology employs a dual-phase 20-MHz current-mode-controlled input stage to reduce the inductance required per phase to only 200 nH, and a 4-output 100-MHz comparator-controlled fully-integrated output stage to reduce the capacitance required per output to 10 nF. To enable each output to handle up to 250-mA load with less than 40-mV voltage ripple, a 3rd-order bond-wire-based notch filter is employed at each output for voltage ripple suppression. Additionally, the proposed design employs dynamic output re-ordering to enhance dynamic and cross-regulation performance, interleaved pulse-skipping to enhance light-load efficiency, and high-gain local output feedback to enhance DC load Regulation. Targeting multi-core DSPs, the proposed design is implemented in standard 65-nm CMOS technology with 1.8-V input, and outputs in the range of 0.6–1.2 V with a total load of 1 A. It achieves a peak efficiency of 74%, less than 40-mV output voltage ripple, 0.5-V/70-ns Dynamic Voltage Scaling (DVS), and settling time of less than 85 ns for 125-mA all with no cross regulations.
CHAPTER 1

INTRODUCTION

In order to reduce the power consumption of multi-core DSPs, each core needs to operate from its own independent power supply that is dynamically optimized based on the real-time workload of each core [1-4]. Therefore, such DSPs requires multiple power supplies that can generate a wide range of low-voltage outputs (0.6–1.2 V), support load currents of up to 250 mA for each digital core, and feature fast dynamic response. The most common approach used to realize these power supplies is shown in Figure 1.1, where secondary power converters is employed to convert power from the DSP’s primary power supply (i.e. 1.8 V) to the digital cores.

![Diagram of Multi-Core Digital Signal Processor]

**Figure 1.1** A block diagram showing a typical multi-core DSP system with secondary power converters used to generate multiple independent power supplies from the DSP’s primary power supply
There are several options to implement these secondary power converters [29]. One option is fully-integrated linear regulators as shown in Figure 1.2(a) [33], which are attractive due to their low cost, but offer limited efficiency (33% at 0.6-V output). A second option is fully-integrated, high-frequency Switch-Capacitor step-down converters as shown in Figure 1.2(b), which offer better efficiency than fully-integrated linear regulators at the expense of larger silicon area. However, they provide optimized efficiency only at fixed conversion ratios, unless reconfigured as a function of the output voltage, which results in poor Dynamic Voltage Scaling (DVS) response [5-8, 26-27]. A third option is conventional buck converters as shown in Figure 1.2(d), which offer high efficiency across a wide range of conversion

**Figure 1.2** Various options for implementing the secondary power converters to power the digital core of the DSP chip.
ratios, but require large and costly off-chip passives and suffer from limited dynamic performance. A fourth option is a conventional Single-Inductor Multiple-Output (SIMO) buck converter as shown in Figure 1.2(e), which offers high efficiency with reduced cost by requiring only a single off-chip inductor. However, in addition to their limited dynamic performance, they suffer from poor cross-regulation and still require multiple off-chip capacitors [9-18]. A fifth option is the recently-proposed Dual-Frequency SIMO (DF-SIMO) buck converter as shown in Figure 1.2(f). This topology is similar to a conventional SIMO, except that the output switching frequency is much higher than the input switching frequency. The DF-SIMO topology is attractive as it reduces the output capacitors to levels at which they can be integrated on-chip, and enables significantly faster output dynamic response and much improved cross-regulation [19-20]. However, the implementation in [19-20] has poor DC load regulation and can only support up to 50-mA load per output to maintain 80-mV voltage ripple. Thus, it is more suitable for low-power microcontrollers rather than multi-core DSPs. Moreover, due to the low input switching frequency (2 MHz), a large 15-µH inductor is required, and the input stage continues to have slow dynamic response. Additionally, the fixed output order employed by the implementation limits the improvement in cross-regulation.

This dissertation tackles the limitations of DF-SIMO by proposing a Dual-Frequency Dual-Inductor Multiple-Output (DF-DIMO) buck converter with a 20-MHz, dual-phase input stage that reduces the required inductance to only two 200-nH inductors, which can be co-packaged with the DSP as shown in Figure 2(e). Furthermore, a 100-MHz output stage with 3rd-order bond-wire-based notch output filters is proposed to allow up to 250-mA load per output with less than 40-mV voltage ripple. Moreover, dynamic output re-ordering and interleaved pulse-skipping are proposed to improve cross-regulation and light-load efficiency.
Finally, a high-gain error amplifier in the output control loop is introduced to improve DC load regulation. The DF-DIMO converter is implemented in 65-nm CMOS and provides 4 outputs at 0.6–1.2 V. It achieves peak efficiency of 74%, DVS response of 0.5-V/70-ns, and settling time of 85 ns for 125-mA load steps.

The dissertation is organized as follows: Chapter 2 discusses the key metrics in the power converters that used in the DSP system. Chapter 3 discusses the advantages and limitations of the state of the art topologies. Chapter 4 analyzes the control techniques for the SIMO converter, where the analysis will also apply to the recent proposed DF-SIMO converter and the proposed DF-DIMO converter. Chapter 5 introduces the design considerations and tradeoffs of the DF-SIMO converters. Chapter 6 presents the top level and circuit level design of the various components of the proposed DF-DIMO converter along with the measurement results and comparison to the state of the art topologies. Chapter 7 concludes the dissertation and discusses the future work.
2.1 Efficiency

The power conversion efficiency of the power converter can be expressed by Equation 2.1:

\[
Eff = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{P_{\text{in}} - P_{\text{loss}}}{P_{\text{in}}}
\]  

(2.1)

where \(P_{\text{in}}, P_{\text{out}}\) and \(P_{\text{loss}}\) are the input power, output power and power loss, respectively. The power loss in the power converter can be classified as conduction loss, gate drive switching loss and transitional loss. Figure 2.1 shows a typical diagram of a buck power converter and the conduction loss \(P_{\text{cond}}\) and gate drive switching loss \(P_{\text{sw}}\) of this converter can be expressed by Equation 2.2 and Equation 2.3:

\[
P_{\text{cond}} \approx \frac{1}{T_{\text{sw}}} \int_{0}^{T_{\text{sw}}} \frac{I_{\text{HS}}(t)^2 dt}{\beta_{\text{HS}} \frac{W_{\text{HS}}}{L_{\text{HS}}} (V_{\text{in}} - V_{\text{thHS}})} + \frac{I_{\text{LS}}(t)^2 dt}{\beta_{\text{LS}} \frac{W_{\text{LS}}}{L_{\text{LS}}} (V_{\text{in}} - V_{\text{thLS}})}
\]

(2.2)

\[
P_{\text{sw}} \approx V_{\text{in}}^2 C_{\text{oHS}} W_{\text{HS}} L_{\text{HS}} + V_{\text{in}}^2 C_{\text{oLS}} W_{\text{LS}} L_{\text{LS}}
\]

(2.3)

where \(T_{\text{sw}}, W_{\text{HS}}, W_{\text{LS}}, L_{\text{HS}}, L_{\text{LS}}, C_{\text{oHS}}, C_{\text{oLS}}, \beta_{\text{HS}}, \) and \(\beta_{\text{LS}}\) is the switching period of the converter, channel width of the high-side device, channel width of the low-side device, channel length of the high-side device, channel length of the low-side device, unit gate capacitance of the high-side device, unit gate capacitance of the low-side device, technology parameter of the high-side device, and technology parameter of the low-side device, respectively. From Equation 2.2 and Equation 2.3, the device channel length must be minimized in order to reduce the conduction loss and the switching loss. However, the
channel length is limited by the input voltage of the power converter. For instance, the short channel device (<130nm) can only tolerate very low voltage (<1.2V) and cannot be directly used to interface with the primary supply voltage of the DSP chip (1.8 V).

The transition loss describes the loss during the period that the high-side power FET is partially turned on. The operation waveforms in this period (the gate-drive voltage $P_{dr}$, drain-source voltage $V_{ds,HS}$ and drain to source current $I_{HS}$ of the high-side FETs) are plotted in Figure 2.2. As shown, since the inductor current is simultaneously supplied by the high-side device and the body diode of the low-side device during this transition, $V_{ds,HS}$ is kept at input voltage level, which results in large losses. The transitional loss of the high-side FET can be expressed by Equation 2.4:

$$P_{cond} \approx \frac{1}{T_{sw}} \int_{0}^{\Delta tr} V_{ds,HS} \cdot I_{HS} \cdot dt$$ (2.4)
where $\Delta tr$ is the transition time of the high-side current described in Figure 2.2. From the equation, the transitional loss can be either reduced by decreasing the transition time of the gate drive signal or the switching frequency of the power converter. However, shorter transition time $\Delta tr$ results in larger voltage ringing at the chip input due to rapid change of the current through the package inductor, which degrades the reliability of the on-chip power device, and a lower switching frequency degrades the dynamic performance of the power converter and requires large passive devices to maintain the same output voltage ripple. An on-chip ringing suppression filter can be employed and optimized to improve device reliability without increasing the transition time and with a reasonable increased loss.

2.2 Dynamic Response

There are two categories dynamic response associated with the power regulators: 1) responding to a load current change (load-step response) and 2) responding to a reference voltage change (DVS).
Figure 2.3 shows a typical waveform of the power converter responding to a load current change, where the output voltage of the power converter (supply voltage of the load system) $V_{out}$ suddenly deviates from its original voltage level when load current is inserted or released. The control loop of the power converter detects the deviations of the output voltage and controls the power devices to bring it back to the desired value. In modern power converters, the recovery time (or settling time shown in Figure 2.3) and the magnitude of the deviation (spike/overshoot/undershoot) must be minimized to maximize the digital core performance. The voltage waveforms $V_{out}$ as shown in Figure 2.3 that respond to the load step typically have three regions. The first region (voltage spike region) “(a)” is the response to the fast transition current through the parasitic inductance $L_{par}$ associated with the off-
chip capacitor or DSP package, and the magnitude of the voltage spike can be approximated by $L_{par} \frac{di}{dt}$, where $\frac{di}{dt}$ is the slope of the load step. Since the slope of the load step is determined by the DSP system and cannot be reduced through power converter design, the routing parasitic inductance must be minimized to reduce the voltage spikes. The best way to improve the routing impedance is to integrating all the output capacitor on-chip, which is the focus in this dissertation. The second region “(b)” of the load transient response ends when the power converter can provide at least the same amount of current as the load current. The magnitude of the overshoot/undershoot of the load step response can be expressed by Equation 2.5:

$$V_{os/us} \approx \left| \int_{t_0}^{t_1} \frac{I_{Load} - I_{PWR}(t)}{C_{Load}} \cdot dt \right|$$

where $t_0$ is the time that the load step inserted or released, and $t_1$ is the time that the output current of the power converter “$I_{PWR}$” equals to the load current “$I_{Load}$”, and $C_{Load}$ is the load capacitor of the power converter. In buck converters (shown in Fig. 3), the slew rate of the power converter output current is limited by the error amplifier bandwidth and regulator switching frequency, inductance employed by the converter and the voltage across the inductor. Shunt linear regulator can be employed to improve the current slewing limitation but at the expense of the efficiency [34]. The third region “(c)” is that the output voltage of the power converter being returned to its original DC level, where the output current of the converter is higher than the load current. The output current approaches to the load current with the output voltage approaching to the final value. It is worth noting that the final DC value of the output voltage after the load step might be slight different from that before the
load step due to finite loop gain of the power converter and finite resistance on the conduction path, and this difference is referred as DC offsets of the load regulation.

In order to reduce the power consumption of multi-core DSPs, the digital core needs to operate from its own independent power supply, which is dynamically scaled based on the real-time workload of each core as shown in Figure 2.4(a), where the digital core ideally

Figure 2.4 (a) The digital core operated from its own independent power supply that is scaled based on the real-time workload of each core and (b) power converter with slow transient response degrades the effectiveness of the DVS algorithm
operates from high supply voltage and at high frequency when the workload is heavy and from low voltage and at low frequency when the workload is light. However, as shown in Figure 2.5(b), due to finite response time, the transition time of the supply voltage can be significant relative to the work load updating period. Therefore, the effectiveness of this DVS scheme can be significant degraded in reality. Similar to load step response, the DVS performance is also limited by bandwidth of the error amplifier, switching frequency, inductance employed in the regulator. However, unlike the load step response, a larger output capacitor will limit the effectiveness of the DVS performance of the power converter.

2.3 Cross Regulation

Figure 2.5 shows typical waveforms of cross regulation transient, where a load step is applied to one output of the secondary power converter(s) for the digital cores (i.e. $I_{out1}$) shown in Figure 1.1 and it not only causes disturbance on $V_{out1}$, but also causes disturbances on the other outputs of the secondary power converters (i.e. $V_{out2}$, $V_{out3}$, $V_{out4}$). The cross regulation transient is typically caused by the converter(s) that sharing the same passive components to generate multiple outputs. (i.e. input capacitor, primary inductors). The brute force way to improve cross-regulation performance is to increase the load capacitance of each supply or use independent components to build the power supplies at the expense of the area, costs and slow dynamic response. In addition, fast output switching frequency and reserved freewheeling current can also improve the cross regulation performance, which will be discussed in this dissertation.

2.4 Area and Cost

One feasible option to reduce the total size and weight of the circuit board that used in the portable devices (i.e. cell phones, media players and laptop computers) is to minimize the
number and size of the discrete passive components of the power converters which occupies more than half of the area of the system. The output capacitors of the power converters are desire to be fully integrated on-chip to minimize the routing impedances and maximize the performance of the load system, while the inductors that are employed by the power converters are preferable to be reduced to less than 200 nH, so that they can be co-packaged with the DSP core to reduce the area and fully integrated with the digital cores in future technologies.

**Figure 2.5** Typical waveforms of the cross regulation transient
CHAPTER III

POWER CONVERSION SCHEMES

3.1 Linear Regulators

Figure 3.1 is the block diagram of a linear regulator, which consists of an error amplifier and a PMOS FET. The output voltage is regulated to the reference voltage by adjusting the on resistance of the PMOS FET through the error amplifier. The output capacitor can be integrated on-chip to reduce the routing inductance and the area of the circuit board. The maximum efficiency of the LDO can be represented as:

$$Eff = \frac{P_{out}}{P_{in}} = \frac{V_{out} \times I_{out}}{V_{in} \times I_{in}} = \frac{V_{out}}{V_{in}}$$  \hspace{1cm} (3.1)
From the equation, if the linear regulators are used as the secondary power converters to interface with 1.8-V shared supply voltage, the maximum efficiency will be 33% if the output voltage is 0.6 V.

3.2 Switched Capacitor Converters

Figure 3.2 (a) show the block diagram of the switched capacitor power converter with

3:1 conversion ratios, where the SC converter has two phases and the charge transfer capacitors $C_{tf}$ are in series configuration in phase 1 and in parallel configuration in phase 2. From charge conservation shown in the figure, the efficiency of the power converter with 3:1 conversion ratio can be written as:

**Figure 3.2** Block diagram of the switched capacitor power converter: (a) with 3:1 voltage conversion ratio and (b) with 3:2 voltage conversion ratio
where \( Q_{out,ph1} \), \( Q_{out,ph2} \), \( Q_{in,ph1} \) and \( Q_{in,ph2} \) are the total charges delivered to the load in phase 1, delivered to the load in phase 2, delivered from the input in phase 1 and delivered from the input in phase 2, respectively. From the equation, this configuration allows the power converter to achieve near 100\% power conversion efficiency if the output voltage is 0.6 V and converted from the 1.8 V-input, but it also limits the maximum output voltage to 0.6V, which is undesirable. To achieve 1.2-V output voltage, a 3:2 conversion ratio configuration, as shown in Figure 3.2 (b) can be used, where the efficiency can be expressed as:

\[
Eff = \frac{P_{out}}{P_{in}} = \frac{V_{out} \times (Q_{out,ph1} + Q_{out,ph2})}{V_{in} \times (Q_{in,ph1} + Q_{in,ph2})} = \frac{3}{2} \times \frac{V_{out}}{V_{in}} \quad (3.3)
\]

From Equation 3.3, if the input voltage is 1.8 V, the 3:2 switched capacitor filter provides 100\% power conversion efficiency at 1.2-V output voltage, but only 50\% efficiency at 0.6-V output voltage.

Therefore, the switched capacitor power converters provide optimized efficiency only at fixed conversion ratios, unless reconfigured as a function of the output voltage, which results in poor DVS response.

### 3.3 Single Output Buck Converters

A conventional single-output buck converter, shown in Figure 2.1, ideally achieves near 100\% power conversion efficiency for any conversion ratios. However, since the switching frequency of a conventional single-output buck converter is typically limited to
several mega-Hertz (i.e. 2 MHz), the inductor or the capacitor employed must be in the several micro-Henrys or several micro-Farads level, which is difficult to be integrated on-chip or co-packaged with the DSP chip.

In some recently published power converters [24, 28, 30], the switching frequency of the buck converter can be designed to hundreds of Mega-Hertz in order to integrate the inductor and capacitor on-chip. However, the short-channel devices (<130 nm) must be used to achieve reasonable switching loss, where the rating voltage of these devices is at 1.2-V and cannot directly interface with the 1.8-V supply voltage of the DSP core.

### 3.4 Single-Frequency SIMO Converters

![Figure 3.3](image-url) The block diagram of a typical SIMO buck converter with two stage topology
As shown in Figure 3.3, the Single Inductor Multiple Output (SIMO) buck converter typically has two stages. The input stage is similar to the power stage of the single-output buck converter, which consists of a high-side and a low-side power FET (i.e. $S_N, S_P$), while the output stage has one power distribution FET for each output (i.e. $S_{o(i)}$). The output voltage of each output is compared to the reference voltages to determine the duty cycle of input stage and the on-time of the output power distribution FETs, which ensures that the outputs are regulated to their target value and the average voltage of the input switching node $V_{swi}$ is equal to the average voltage of output switching node $V_{swo}$. The SIMO converter achieves nearly 100% power conversion efficiency for any conversion ratios without reconfiguration and requires only one inductor which is shared by all the outputs.

However, conventional SIMO converter suffers from poor cross regulation, and the current ripple through the output capacitor of the SIMO converter is even larger than that of the single-output buck converter due to its discontinuous current distribution. Therefore, larger off-chip output capacitors, which are expensive and limit the dynamic performance of the converter, must be employed in order to achieve small output voltage ripple.

### 3.5 Dual-Frequency SIMO Converters

The schematic diagram of Dual-Frequency Multiple Output buck converter (DF-SIMO) is similar to conventional SIMO converter as show in Figure 3.4. However, unlike conventional SIMO converters, the input stage of the DF-SIMO converter employs high voltage devices (0.18-μm CMOS) and switches at lower frequency (i.e. 2MHz) in order to interface with high input voltage, while the output stage employs low-voltage devices (65-nm CMOS) and switches at much higher frequency (i.e. 100MHz) in order to improve the cross
regulation performance and dynamic performance without suffering from a significant efficiency drop due to switching loss. In addition, higher switching frequency reduces the size of the output capacitor, so that the output capacitors can be fully integrated on-chip to further improve the dynamic performance of the converter and reduce the system area and cost.

With comparator-based controller implemented in [20], only the peak of the output voltage is regulated as shown in Figure 3.5, and the voltage ripple is a function of the load current [20]. Therefore, the implementation in [20] has poor DC load regulation and only supports up to 110-mA load per output to maintain an 80-mV voltage ripple with 13 nF capacitors and

Figure 3.4 The block diagram of DF-SIMO buck converter showing its dual-frequency operation.
120 MHz switching frequency. Thus, it is more suitable for low-power microcontrollers rather than multi-core DSPs. Moreover, due to the low input switching frequency (2 MHz), a large 15-μH inductor is required, and the input stage continues to have slow dynamic response. Additionally, the fixed output order employed by the implementation limits the improvement in cross-regulation.

**Figure 3.5** The operation waveforms of the DF-SIMO converter showing the average output voltage, output voltage ripple and the reference voltage for the $i^{th}$ output.
CHAPTER 4

SIMO CONVERTER CONTROL TECHNIQUES

Conventional SIMO buck converter control techniques can be classified as two categories: 1) Multiple inductor Energizing/de-energizing Cycle (MEC) in one output switching period [15-16] and 2) Single inductor Energizing/de-energizing Cycle (SEC) in one output switching period [8-14], where the inductor energizing and de-energizing is accomplished by controlling ON and OFF of the high-side and low-side power FET of the input stage.

4.1 MEC Control

Figure 4.1 and Figure 4.2 show a block diagram of a 2-output SIMO converter with MEC control and its operation waveforms, where the controller dedicates one inductor energizing and de-energizing cycle for each of the outputs, and the duty cycle of each cycle within the time slot of each output is determined by the individual feedback loop of each output. Ideally, the on-time of the input stage power FETs can be related to the input and output voltages by:

\[
\frac{V_{o(1)}}{V_{in}} \approx \frac{t_{on\_hs(1)}}{t_{on\_ls(1)} + t_{on\_hs(1)}} \tag{4.1}
\]

\[
\frac{V_{o(2)}}{V_{in}} \approx \frac{t_{on\_hs(2)}}{t_{on\_ls(2)} + t_{on\_hs(2)}} \tag{4.2}
\]

where \(t_{on\_hs(1)}\), \(t_{on\_hs(2)}\), \(t_{on\_ls(1)}\) and \(t_{on\_ls(2)}\) are all defined in Figure 4.2. SIMO converter with MEC control is very similar to the single-output buck converter that operating in the DCM (Discontinuous Conduction Mode), but with additional multiplexers to select the proper feedback and reference signals in their allocated slots. Therefore, if one of the output
voltages is less than its reference, the controller can either requests a longer on-time for its high-side power FET or a higher inductor current that delivered to its load within its own time slots. However, since all the outputs must operate in DCM mode, this controller limits the maximum current that the converter can delivered to the load. To tackle this limitation, an optional freewheeling switch is employed, so that the converter can operate in Pseudo Continuous Conduction Mode (PCCM) by setting a minimum on-time for the freewheeling switch as shown in Figure 4.3. However, this control mechanism have serious regulation problem if some of the outputs operate in heavy load while some outputs operate in light

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**Figure 4.1** The block diagram of the SIMO buck converter with MEC control
load. In addition, the switching and conduction loss associated with the freewheeling switch degrades the efficiency especially in aforementioned heavy-light load condition. Moreover, since high voltage device must be employed at the input stage to tolerate high input voltage and the input stage power switches must switch multiple times (one time for each output) to energize and de-energize the inductor in one power converter switching period as shown in Figure 4.3, the total switching loss will be further increased.
A 3-output SIMO converter with SEC control and its operational waveforms are shown in Figure 4.4 and Figure 4.5, where the inductor current is distributed to all the outputs in one inductor energizing and de-energizing cycle. The duty cycle of the input stage and the on-time of the output switches are determined by the feedback information from all the outputs rather than the independent feedback loop for each output in its dedicated time slots. Similar to MEC control, the duty cycle of the input and output stage in SEC control can
be related to the input and output voltage by the following equation:

\[ V_{in} \cdot D_{in} \approx \sum_{i=1}^{n} V_{o(i)} \cdot D_{o(i)} \]  \hspace{1cm} (4.3)

\[ D_{o(i)} \approx \frac{I_{o\_avg(i)}}{I_{ind}} \]  \hspace{1cm} (4.4)

where \( D_{in} \) is the duty cycle of the input stage, \( D_{o(i)} \) is the duty cycle of the \( i^{th} \) output at the output stage, \( I_{o\_avg(i)} \) is the average load current of the \( i^{th} \) output and \( I_{ind} \) is the instantaneous inductor current which can be approximated as average inductor current if the current ripple is small. Since the duty cycle is a function of both the load currents and output
voltages, it is difficult for the voltage mode controller to respond correctly in this control technique without knowing the load current condition for all the outputs. For example, for a three-output SIMO converter with the input voltage of 1.8V, the output voltages are regulated to 0.6V, 0.9V and 1.2V initially. If the output voltage of the 0.9-V output is lower than its reference, the converter requires a higher input stage duty cycle ($D_{in}$) in order to recover the output voltages when the load current of the 0.6-V output is much higher than the load current of the 1.2-V output and a lower $D_{in}$ when the load current of the 1.2-V output is lower than the load current of the 0.6-V output.

If the inductor current sensing is available, a current-mode controller can be employed to assist the system to respond correctly. For instance, if one of the output voltages

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**Figure 4.5** The timing diagram and operation waveforms of the SIMO buck converter with SEC control
is lower than their references and the other output voltages are well-regulated, the current-mode controller can regulate the inductor current to a much higher level, and the duty cycle of the input stage can be adapted automatically to recover its output voltage to the reference.

However, if some of the output voltages are lower than their reference voltages while the others are higher than the reference voltages, the current mode controller still cannot respond to the error information correctly. To address this, the ordered power distributive control mechanism [11] can be used at the output stage, where the inductor current is distributed to the outputs sequentially (from the first output to the last output) and the error is accumulated at the last output. The current mode controller then determine the duty cycle of the input stage based only on the error information from the last output as shown in Figure 4.4.

In addition, to prevent the last output from being an error accumulating victim and suffering excessive overshoots and undershoots during the transient, a freewheeling switch can be employed and the controller can reserve a dedicated time slot for the freewheeling switching being turned on after all the outputs are served. The current mode controller again can determine the duty cycle of the input stage and the inductor current based on the actual on-time of the freewheeling switch as shown in Figure 4.6 and Figure 4.7. Since all the errors are accumulated to the average current through the freewheeling switch, transient performance at the last output is significantly improved.

Unlike MEC control, the inductor energizing and de-energizing cycle in SEC control is shared by all the outputs, and thus the effective switching frequency at the input stage is much lower, where the device needs to interface with high voltage. Therefore, the SEC control can significantly improve the efficiency without increasing the voltage ripple or
employing a larger off-chip capacitor. In addition, the scenario that some of the outputs are in high-load condition and some of the outputs are in light load condition no longer increases the control complexity and can be easily handled by pulse skipping control (which is discussed in detail in Chapter 7 of this dissertation).

**Figure 4.6** The block diagram of the SIMO buck converter with SEC control and an additional freewheeling switch
There are two options to determine the duty cycle of each of the outputs in SEC control. The first option (comparator-based control as shown in Figure 4.8) is to use one comparator for each of the outputs to compare the output voltage to a reference, where each output is severed sequentially and on-time of each output is determined by the output of the comparator which compares the output voltage to a reference. The comparator-based control allows the output voltage to be charged to its reference in less than one switching period. Therefore, the power converter enjoys a good transient performance. However, since the
output voltage can be noisy due to the rapid change of the load current, false triggering of the comparator can occur, which results poor regulation of the output voltage.

The second option (charge-based control) is to use one additional amplifier at each of the outputs. If the average output voltage is less than the reference voltage, the controller increases the on-time and requests more charge for this particular output as shown in Figure 4.9. Since the duty cycle of the output of the charge-based control is based on the information of the average output voltage, the output voltage regulation is improved at the expense of the transient performance.

**Figure 4.8** The schematic diagram of the comparator-based control that used in the output stage to regulate the output voltage to its reference

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The schematic diagram of the comparator-based control that used in the output stage to regulate the output voltage to its reference.
Figure 4.9 The schematic diagram of the charge-based control that used in the output stage to regulate the output voltage to its reference.
CHAPTER 5

DESIGN CONSIDERATIONS AND TRADEOFFS OF THE DF-SIMO POWER CONVERTER TOPOLOGIES

For DF-SIMO converter, the input stage employs high voltage devices and switches at lower frequency in order to interface with high input voltage, while the output stage employs low-voltage devices and switches at much higher frequency in order to improve the cross regulation performance, dynamic performance and fully integrating the output capacitors without suffering from significant efficiency drop due to switching loss. Therefore, the DF-SIMO converter employs single energizing and de-energizing cycle for multiple outputs’ switching periods instead of for one. Similar to single-frequency SIMO with SEC control, the DF-SIMO converter employs current mode controller for the input stage, while comparator-based control or charge-based controller can be employed at the output stage. Thanks to the control schemes used in the output stage, the low frequency components of the current that delivering to the 1st output to the n – 1th outputs are minimized, while the high frequency components of the current is filtered by the small size of the on-chip integrated capacitor. However, the low frequency inductor current ripple is accumulated at the last output and cannot be filtered out by the on-chip capacitors, and thus a large voltage ripple can be observed at the last output if only on-chip capacitor is used. If a single off-chip capacitor is used as the filter at the last output, a large voltage spike will be produced at the last output due to rapid transition of the current through the package bond-wire and parasitic inductance of the off-chip, which is also unacceptable.

There are two options to mitigate the voltage ripple and spikes at the last output. The first option is to employ a composite filter to absorb the low frequency current ripple as well
as the high frequency spikes. The block diagram of the DF-SIMO converter with this composite filter is shown in Figure 5.1. As discussed, since the comparator-based control is employed at the output stage from the 1st to the \( n-1 \)th output, the duty cycle of these outputs increases with the decrease of the inductor current and the charges that are distributed to one of these outputs are approximately the same for all the output switching cycles. Therefore, low frequency \((f_{swl})\) components of the inductor current that distributed to these outputs can be ignored and only the high-frequency \((f_{swo})\) current ripple needs be taken into consideration, which can be suppressed by the on-chip output capacitors (i.e. \( C_1 \) to \( C_{(n-1)} \)).

The rest of the inductor current which not only contains high-frequency but also low-
Figure 5.2 The current path (in red) at the output stage of the DF-SIMO converter shown in Figure 5.1 for (a) second output is ON and (b) the last output is ON.
frequency current ripple is distributed to the last output and need to be suppressed by the composite filter. Figure 5.2 shows the current path at the output stage of the DF-SIMO converter for the scenarios that the second output is ON (a) and the last output is ON (b). As shown, the inductor current that distributed to the first output to the $n - 1^{th}$ output is...
routed to the negative port of the composite filter, while the current distributed to the last output is routed to the positive port of the composite filter. The composite filter along with its input stimulus thus can be modelled in Figure 5.3 and the impedances of the composite filter are plotted in Figure 5.4 and Figure 5.5. Since the input stimulus of the output filter contains both input and output switching frequency components, the resonance peak of the output filter must be designed to be between these frequencies to minimize the output voltage ripple. From the figure, the input switching frequency can be designed to 3MHz, while the output switching frequency can be designed to 100MHz.

The second option is to add a dedicated freewheeling switching slot at the end of each output cycle as in single-frequency SIMO. However, the average current through this switch must be regulated to be larger than half of the inductor current ripple, so that the low frequency inductor current ripple can be absorbed by the freewheeling switch and small voltage ripple can be achieved with only on-chip capacitors [20]. Therefore, the input and output frequency is no longer limited by the composite filter resonant frequency but the overall efficiency can be degraded due to additional freewheeling current loss.
CHAPTER 6
A 1A, DUAL-FREQUENCY DUAL-INDUCTOR 4-OUTPUTS BUCK CONVERTER WITH FULLY-INTEGRATED OUTPUT FILTER FOR DIGITAL SIGNAL PROCESSORS

6.1 Top Level Design of the Proposed DF-DIMO Topology

The block diagram of the proposed DF-DIMO buck converter is shown in Figure 6.1, where 4 outputs are generated from a 1.8-V input source [21]. The design is fully integrated
on-chip except for the two 200-nH inductors. Similar to the 2-MHz single-phase input stage in the DF-SIMO in [19-20], the power switches are implemented using single 1.8V-rated devices to interface directly with the input, which mitigates the reliability concerns and

$$\text{Figure 6.2 Timing diagram showing the steady-state waveforms of the inductor current in the 20-MHz dual-phase input stage and the sequential distribution of the current to the outputs and the freewheeling switch at 100-MHz rate}$$

eliminates the need for the complicated gate-drive circuits and intermediate power supplies associated with using cascodes of low-voltage devices [30, 31]. However, due to the 20-MHz input stage in the proposed DF-DIMO, on-chip ringing suppression filters must be employed to reduce ringing at the input rails in order to protect the power switches from excessive voltage stress. The output stage is switching at 100 MHz with the power switches implemented using single 1.2V-rated devices to minimize losses. Unlike conventional 1st-order single-capacitor output filters typically employed in SIMO and DF-SIMO topologies
the proposed DF-DIMO employs 3rd-order notch output filters implemented using bond-wire inductors and on-chip capacitors to further suppress the output voltage ripple so that higher levels of loads can be supported [21]. The steady-state operation of the DF-DIMO converter is illustrated in Figure 6.2. In normal operation, the current from the two inductors is distributed sequentially to the outputs so that each output is served once every output switching cycle, and five times each input switching cycle. The period of time each output is served within an output switching cycle is determined by a peak-voltage comparator-based controller to ensure output regulation. After all outputs have been served, any remaining current in the inductors is routed to a freewheeling switch for the rest of the output cycle. Moreover, the average current in the freewheeling switch (i.e. the freewheeling current) is regulated by the input stage to at least half the total inductors’ ripple current to ensure proper operation and create a reserve current in the inductors at all times. This mechanism of controlling the freewheeling switch and its reserve current ensures that the outputs dynamic response and cross-regulation performance is limited only by the output stage’s high switching frequency and the reserve freewheeling current instead of the lower switching frequency of the input stage [21].

6.2 Input Stage Design of the DF-DIMO Topology

For 4, 250-mA outputs, the total inductor current in the DF-DIMO converter exceeds 1 A, which degrades efficiency due to conduction losses at the input stage. Thus, a dual-phase input stage is adopted to reduce these losses. Moreover, to reduce the inductance to 400 nH (to be co-packaged with the DSP), a 20-MHz input switching frequency is selected. This 20-MHz dual-phase design also results in much faster input stage response compared to the DF-SIMO scheme in [19-20], which improves output dynamic response and cross-
regulation in cases where the freewheeling current is insufficient to handle large steps in the output voltage or current. Moreover, it allows for quickly adapting the freewheeling current in cases where output voltage or current changes are known in advance (common in DSPs) to achieve better dynamic response without reducing efficiency. This would not be possible with a slow input stage as it can’t adapt the freewheeling current for frequently toggling loads, and thus, it must always be set to high levels, which degrades efficiency.

However, a 20-MHz input switching frequency introduces large switching and transitional losses across the input power switches. To minimize transitional losses, it is necessary to reduce the rise and fall times of the gate-drive signals of the high-side power switches (“$S_{P<1-2>}$” in Figure 6.1), but faster gate-drive transitions produce large ringing at the on-chip input and ground rails due to the rapid current transition through the parasitic inductors of the package pins used for these rails. This ringing causes excessive voltage stresses across the power switches and degrades their reliability. On-chip input ringing suppression filter must be employed to tackle this issue.

6.2.1 Input Filter Design

6.2.1.1 Using a Capacitor-Only Ringing Suppression Filter

One method to suppress the on-chip input and ground ringing is to introduce an additional on-chip decoupling capacitor $C_f$ (capacitor-only ringing suppression filter) as shown in Figure 6.3(a). To study the on-chip input and ground ringing, the converter can be modelled by the lumped impedance network shown in Figure 6.3(b), where $L_{P,\text{in}}$, $C_{P,\text{in}}$, and $R_{P,\text{in}}$ are the effective parasitic inductance, capacitance, and resistance of the package pins used for the input voltage. This lumped network is stimulated by a current source $I_{in,\text{int}}$
oscillating between zero and $I_L$ to produce the voltage $V_{in\_int}$. From Figure 6.3(b), the transfer function $Z_f$ between $V_{in\_int}$ and the stimulating current source $I_{in\_int}$ can be derived as:

$$Z_f \approx \frac{(L_{P_{in}} \cdot s + R_{P_{in}})}{L_{P_{in}}(C_{P_{in}} + C_f)s^2 + R_{P_{in}}(C_{P_{in}} + C_f)s + 1} \tag{6.1}$$

Figure 6.3 (a) Capacitor-only ringing suppression filter employed at the on-chip input to suppress the voltage ringing (b) Combined circuit model of the schematic diagram shown in (a) along with its input stimulus $I_{in\_int}$

From Equation 6.1, it can be shown that the peak magnitude of $Z_f$ and the resonance frequency $f_p$ of that peak are:
\[ |Z_f| = \frac{L_{\text{pin}}}{R_{\text{pin}}(C_{\text{pin}} + C_f)} \]  

\[ f_p = \frac{1}{2\pi\sqrt{L_{\text{pin}}(C_{\text{pin}} + C_f)}} \]

Figure 6.4 shows \( |Z_f| \) for \( L_{\text{pin}} = 1 \text{nH} \) and \( R_{\text{pin}} = 50 \text{m\Omega} \) and various values \( C_f \) between 0–10 \( \text{nF} \). Moreover, the Fourier Series of the stimulating current source \( I_{\text{in,int}} \) can be written as:

\[ I_{\text{in,int}} = \sum_{n=1}^{\infty} a_n \cdot \cos(2n\pi f_{\text{swi}}) \]

where \( f_{\text{swi}} \) is the switching frequency of the input stage, and \( a_n \) are the Fourier Series Coefficients, which are plotted in Figure 6.5 for various values of \( \Delta tr \) assuming \( f_{\text{swi}} = 40 \text{ MHz} \). By observing the spectral behavior of \( |Z_f| \) and \( I_{\text{in,int}} \), it can be seen that increasing
the on-chip decoupling reduces the peak of $|Z_f|$, which should reduce the ringing. However, since the resonance frequency also drops with larger on-chip decoupling, this peaking occurs at frequencies where the spectral components of $I_{in \_int}$ are larger as shown in Figure 6.5, which limits the effectiveness of ringing suppression. As a result, the resonance frequency of $|Z_f|$ must be moved to a much lower frequency than the switching frequency of the converter in order to get significant suppression of all the spectral components of $I_{in \_int}$, which requires a very large on-chip input decoupling capacitor (>20nF), and thus large area.

To suppress ringing without significantly increasing silicon area, instead of pushing the resonance frequency of the impedance network to a much lower frequency than the

\[
\begin{align*}
\Delta t_r &= 4 \text{ns}, \ d = 0.6, \ I_L = 1 \text{A}, \ f_{swi} = 40 \text{MHz} \\
\Delta t_r &= 0.1 \text{ns}, \ d = 0.6, \ I_L = 1 \text{A}, \ f_{swi} = 40 \text{MHz}
\end{align*}
\]

**Figure 6.5** Spectral components of the stimulating current source of Fig. 6.4 for two values of the rise and fall time of the current step.
switching frequency of the converter by making $C_f$ quite large, $C_f$ can be made just large enough to place this resonance frequency between the switching frequency of the converter and its first harmonic as shown in Figure 6.6 [22].

![Figure 6.6](image)

**Figure 6.6** The transfer function of the impedance network showing placing its peak frequency between the switching frequency and its first harmonic.

### 6.2.1.2 Using an RC snubber ringing suppression filter

An on-chip input decoupling capacitor can be used to help reduce this ringing. However, this either requires a fairly large capacitor, or a smaller one but with precise knowledge of the value of the parasitic inductors [22]. Instead, an RC-based on-chip input ringing suppression filter is introduced. Figure 6.7 shows the combined circuit model of the package pins and the input capacitance of the power switch in each input phase, along with
the RC-based ringing suppression filter. The filter, commonly referred to as RC snubber [23], is formed by the series combination of the resistor “\(R_f\)” and the capacitor “\(C_f\)”. The ringing at the on-chip input rail “\(V_{\text{in,int}}\)” due to the converter’s input current “\(I_{\text{in,int}}\)” can be studied through the impedance “\(Z_f\)” shown in Figure 6.7, which can be written as:

\[
Z_f \approx \frac{(R_fC_f \cdot s + 1)(L_{\text{p, in}} \cdot s + R_{\text{p, in}})}{R_fC_fL_{\text{p, in}}C_{\text{p, in}}s^3 + (R_fC_fR_{\text{p, in}}C_{\text{p, in}} + L_{\text{p, in}}C_f + L_{\text{p, in}}C_{\text{p, in}})s^2 + (R_{\text{p, in}}C_{\text{p, in}} + R_{\text{p, in}}C_f + R_fC_f)s + 1} \tag{6.5}
\]

From Equation 6.5, if \(R_f = 0\) and \(C_f = 0\) (no ringing suppression filter), the poles of \(Z_f\) will be high-Q complex poles, which results in frequency peaking in \(Z_f\) as shown in Figure 6.7(b) and a corresponding time-domain ringing in excess of 2.3V (i.e. 3.2 V) as shown in Figure 6.7(c), which can damage the high-side power switch. If \(R_f = 0\) (capacitor-only filter), the poles of \(Z_f\) continue to be high-Q complex poles, with the frequency peaking in \(Z_f\) dropping in magnitude and location at higher values of \(C_f\). It can be shown that \(C_f\) must be significantly larger than 23 nF to ensure that if the parasitic inductance is less than expected, the peaking frequency of \(Z_f\) will continue to be lower than the switching frequency of the input stage and that the corresponding time-domain ringing will be lower than 2.3 V as shown in Figure 6.7(c), which takes large silicon area. To reduce the time-domain ringing and its sensitivity to the precise value of the parasitic inductance without a large \(C_f, R_f\) can be used to ensure that the poles of \(Z_f\) are always real in order to eliminate the inductance-dependent frequency peaking in \(Z_f\) altogether. From Equation 6.5, this is accomplished by ensuring that \(R_f\) is larger than \(\left(2 \times \sqrt{\frac{L_{\text{p, in}}}{C_f}}\right)\). In this case, the maximum magnitude of \(Z_f\) can be approximated by \((R_f)\), which is also insensitive to the precise value of the parasitic inductance. However, since the magnitude of \(Z_f\) is still a function of \(R_f\), it is not desired to
increase $R_f$ much beyond $\left(2 \times \sqrt{\frac{L_{P,\text{in}}}{C_f}}\right)$ to avoid excessive ringing. For the characterized values of the parasitics associated with the input pins and the power switch, $R_f = 1.8 \ \Omega$ and $C_f = 2 \ \text{nF}$ ensure that the time-domain ringing peak is less than 2.3 V as shown in Figure 6.7(c). The required on-chip capacitance is significantly reduced.

![Parasitics Model](image)

**Figure 6.7** (a) RC snubber ringing suppression filter employed at the on-chip input to suppress the voltage ringing (b) Frequency response of “$Z_f$”, and (c) Time-domain peak of the on-chip ringing with no ringing suppression filter, a capacitor-only filter, and RC snubber circuit

### 6.2.2 Input Controller Design

The input stage uses the peak-current-mode controller shown in Figure 6.8 to regulate the average freewheeling current “$I_{avg,\text{fw}}$” to at least half the total inductor’s ripple current
as described. This is accomplished by integrating the difference between the estimated freewheeling current \( I_{est.fw} \) and the reference level \( I_{ref.fw} \) to obtain the error signal \( V_{err} \) using the simple circuit shown in Figure 6.8, where \( I_{est.fw} \) is obtained by gating the sensed average inductors’ current \( I_{avg.ind} \) by the high-frequency control signal \( S_{fw} \) of the freewheeling switch obtained from the output controller. This eliminates the need to directly sense the freewheeling current, which greatly simplifies the design.

The current imbalance problem in multi-phase converters results from using a voltage-mode controller that compares the output voltage to the same ramp and produces the same duty-cycle for all the phases. Therefore, if there is any mismatch between the phases (i.e. inductor value, switch resistance, etc..), current imbalance will occur. However, in our design, we are using a peak-current-mode controller, where the peak inductor current of each individual phase is sensed and compared to the same “shared” error voltage for all the phases.

Figure 6.8 Schematic diagram of the current-mode controller of the input stage of the proposed DF-DIMO converter showing the freewheeling current estimator
Therefore, regardless of any mismatch between the phases, the peak current will be the same in all the phases due to the action of the controller and the “shared” error voltage (i.e. the duty-cycle for each phase is adjusted to maintain the same peak current). As a result, the current imbalance problem is eliminated.

The input stage control loop in Figure 6.8 is a first-order inherently-stable loop as demonstrated in [20], with the integrating capacitor “\( C_c \)” and the sense resistors “\( R_{sen} \)” determining its unity gain frequency (around 2 MHz in this design). Since the output filters are outside of this control loop, they do not affect its transfer function or its stability. The transfer function of the input stage control loop can be described as:

\[
H(s) \approx \frac{2}{R_{sen}C_c s}
\]  
(6.6)

The inductor current in each input phase is sensed by the conventional current sensors shown in Figure 6.9. However, at the beginning of the ON-time and OFF-time of the power switches, where a rapid transition in the current occurs, and due to the limited bandwidth of the sense amplifiers, the sensed current profile produced by the conventional current sensors will be inaccurate until the sense amplifiers settle. This is not a problem at low switching frequencies as this settling time is much shorter than the switching period, and thus, the average inductor current can be accurately estimated by directly summing the sensed high-side and low-side currents. However, with high switching frequency, the settling time becomes significant relative to the switching period, leading to large errors in the estimated average inductor current. To mitigate this issue without increasing the quiescent current of the amplifiers, additional sample and hold circuits are proposed to sample only the peak and valley levels (“\( I_{sh.peak<i>\)” and “\( I_{sh.valley<i>\)” of the sensed high-side and low-side currents, and
summing these values to generate the accurate estimation of the average inductor current that can be used by the input controller in Figure 6.8.

**Figure 6.9** Schematic diagram of the high-side and low-side current sensors including the proposed peak and valley sample and hold circuits used to mitigate the impact of the settling errors of conventional current sensors.

### 6.3 Output Stage Design of the DF-DIMO Topology

#### 6.3.1 Output Filter Design

In the DF-SIMO topology, a 1st-order filter implemented using a single on-chip capacitor is employed at each output to suppress the output voltage ripple [19-20]. With this strategy, the steady-state output voltage ripple “$\Delta V_{o(i)}$” of any given output can be approximated by:
\[
\Delta V_{o(i)} \approx \frac{I_{o(i)}}{C_{o(i)}} \times f_{swo} \left( 1 - \frac{I_{o(i)}}{I_{ind}} \right)
\] (6.7)

where \(I_{o(i)}\) and \(C_{o(i)}\) are the \(i^{th}\) output’s load current and output capacitance respectively, \(I_{ind}\) is the inductor current, and \(f_{swo}\) is the output switching frequency. From Equation 6.7 it can be seen that higher load current results in larger voltage ripple. For instance, in DF-SIMO assuming 4 identical outputs with the average freewheeling current set to zero, the average inductor current would be 4-times the individual load current. Thus, with 100-MHz output switching frequency and 10-nF capacitance per output, maintaining 40-mV of voltage ripple requires limiting the load current to 50 mA per output. To allow for higher loads without increasing the voltage ripple, either the output switching frequency or the on-chip capacitance must be increased at the expense of efficiency or silicon area. Moreover, traditional ripple reduction techniques used in buck and switched-C topologies, such as

**Figure 6.10** Options for implementing higher order output filters using bond-wire inductors to suppress voltage ripple at the output switching frequency: A 3\textsuperscript{rd}-order low-pass filter
active ripple cancellation [25] and interleaved input stages [27-28], will not be effective in the comparator-controlled DF-DIMO topology since the output voltage ripple is dominated by the load rather than the inductor ripple current. Therefore, and to avoid increasing the output switching frequency [32] or increasing the output on-chip capacitance in the DF-DIMO topology, we propose leveraging package bond-wires to replace the 1st-order single-capacitor filter used at each output with a higher order filter to allow up to 250-mA of load per output with less than 40-mV of ripple. Due to the fact that current is routed to the outputs in the form of discontinuous pulses, the trans-impedance of the output filter should be as small as possible at the output switching frequency. One option to implement such output

**Figure 6.11** Options for implementing higher order output filters using bond-wire inductors to suppress voltage ripple at the output switching frequency: A 3rd-order notch filter.
filter using bond-wires is shown in Figure 6.10, where the output on-chip capacitor $C_o$ is split equally between the load side and the output power switch side in order to keep the total on-chip capacitance the same as in the single-capacitor filter case. The load side is bonded to a dedicated package pin using a single bonding pad, while the output power switch side is bonded to the same pin using a separate pad. This configuration realizes a 3$^{rd}$-order trans-impedance function as shown in Figure 6.12, which provides better attenuation to the current pulses compared to a traditional single-capacitor filter. However, further attenuation to the current pulses can be achieved by adding another on-chip capacitor “$C_p$” between the two
bonding pads as shown in Figure 6.11. The trans-impedance function of this filter can be written as:

$$\frac{V_o}{I_{o-prefilter}} = \frac{L_sC_ps^2 + R_sC_ps + 1}{s(L_s(C_1C_2+(C_1+C_2)C_p)s^2 + R_s((C_1+C_2)C_p + C_1C_2)s + (C_1+C_2))}$$

(6.8)
where $L_s$ and $R_s$ are the series inductance and resistance of the 2 bond-wire inductors (for this design, $R_s$ is about 50 mΩ per 1-nH inductance), and $C_1$ and $C_2$ are defined as shown in Figure 6.10 to maintain the same total on-chip capacitance as in Figure 6.11. The transfer function has a pole at DC, two poles at \( \frac{1}{2\pi \sqrt{L_s(C_1+C_2+C_p)/c_1+c_2}} \), and two zeros at \( \frac{1}{2\pi \sqrt{L_sC_p}} \), which realizes a 3rd-order notch filter. By properly sizing $C_1$, $C_2$, and $C_p$, the notch frequency of the filter can be designed to further suppress the 100-MHz component of the output voltage ripple as shown in Figure 6.12. However, since $L_s$ is expected to vary, it is important to characterize how the voltage ripple changes with such variations to select the optimum value of $C_p$. For that purpose, transient simulations are performed for various values of $L_s$ and $C_p$ while keeping the total on-chip capacitance $C_o = C_1 + C_2 + C_p$ constant at 10nF. The resulting output voltage ripple magnitude is plotted in Figure 6.13. From these simulations, sizing $C_p$ in the range of 0.5–0.8 nF will result in the output voltage ripple being 40 mV or less across a wide range of bond-wire inductance values (2.5–8 nH).

### 6.3.2 Output Stage Control

In the basic peak-voltage comparator-based control scheme with a single-capacitor output filter shown in Figure 6.14(a) [19-20], the $i^{th}$ output starts receiving charge from the inductor at the rising edge of the signal “$S_{set(i)}$”, which causes the signal “$S_{set(i+1)}$” to move to logic “low” and turns ON the output power switch. Once the $i^{th}$ output rises to the reference level “$V_{ref(i)}$”, the control comparator “cmp” causes the signal $S_{set(i+1)}$ to move to logic “high”, which turns OFF the output power switch and also triggers the $(i + 1)^{th}$ output to start receiving the inductor charge. Since only the peak of the output voltage rather than its average is regulated, and since the voltage ripple is a function of the load, this scheme suffers
from poor DC regulation as shown in Figure 6.14(a). Moreover, any noise at the output can easily falsely trigger the control comparator.

Since the DF-DIMO topology proposed in this paper employs a more complicated output filter, a modified version of the basic peak-voltage comparator-based control must be used as shown in Figure 6.14(b). In this scheme, the pre-filter voltage “\( V_{\text{pf}}(i) \)” rather than the final output voltage is compared to the peak voltage “\( V_{\text{peak}(i)} \)” to determine the state of the power switch, where \( V_{\text{peak}(i)} \) is generated by the high-gain error amplifier “\( EA \)”.

**Figure 6.14** (a) Basic peak-voltage comparator-based control with a single-capacitor output filter showing poor DC load regulation, and (b) The proposed modified comparator-based control with interleaved pulse-skipping, 3rd-order notch output filter, and error amplifier showing improved DC load regulation.
the pre-filter voltage is done to ensure the stability of the control loop since the final output voltage is phase-shifted by more than 180° from the gated inductor current “$I_{o\text{-prefilter}(i)}$” due to the 3rd-order notch filter. This also has the additional benefit of isolating the control comparator from any output noise. Moreover, the error amplifier “$EA$” introduced in the output feedback loop improves the output’s DC load regulation by ensuring that its average voltage is regulated rather than its peak voltage as shown in Figure 6.14(b). Since the pre-filter voltage $V_{o\text{-prefilter}(i)}$ is compared to the $V_{peak(i)}$ to determine the duty-cycle of the output stage, the input of the filter can be considered connected to a voltage-controlled voltage source with an input voltage of $V_{peak(i)}$ and a gain of 1 and the output stage control
loop can be modelled as Figure 6.15. The control comparators are implemented with multi-stage continuous-time comparators, and the transfer function of the local, comparator-based output feedback loop including the error amplifier can be derived as:

\[ H(s) = F(s) \times G(s) = F(s) \times \left[ \frac{A_0}{1 + s/p_1} \right] \]  

(6.9)

where \( F(s) \) is the transfer function of the 3rd-order filter, and \( A_0 \) and \( p_1 \) are the DC gain and dominant pole of the error amplifier. The unity gain frequency of the amplifier (i.e. \( A_0 \times p_1 \)) is designed to be around 10 MHz, which is lower than the poles and zeros of the filter (>30MHz). Therefore, \( F(s) \) has very small impact on the phase margin, and the loop behaves as a first-order loop that is naturally stable.

In single-output buck converters, a load step \( \Delta I \) will result in an undershoot \( \Delta V_{us} \) if the load step is positive, and an overshoot \( \Delta V_{os} \) if the load step is negative. The overshoot and undershoot can be approximated using standard equations in the literature [35] by:

\[ \Delta V_{us} = \frac{L \times \Delta I^2}{2 \times C_{out} \times (V_{in} - V_o)} \text{ if } \Delta I \text{ is a positive step} \]  

(6.10)

\[ \Delta V_{os} = \frac{L \times \Delta I^2}{2 \times C_{out} \times V_o} \text{ if } \Delta I \text{ is a negative step} \]  

(6.11)

where \( C_{out} \) is the output capacitance, \( L \) is the inductor, and \( V_{in} \) and \( V_o \) are the input and output voltages respectively. This equation essentially describes the droop in the output voltage until the inductor current catches up with the new load value.

In the DF-DIMO design with EA, similar equations can be developed. For positive load steps, if the step size is smaller than the freewheeling current “\( I_{avg,fw} \)” (the level at
which the freewheeling current is regulated), the reserve current in the inductor is sufficient to handle the step without waiting for the input stage to accumulate additional current in the inductor. In this case, the undershoot voltage “$\Delta V_{us}$” is determined only by the on-chip output capacitance, the output switching frequency “$f_{sw o}$”, and the load step size “$\Delta I_l$”, and can be approximated by:

$$\Delta V_{us} \approx \frac{\Delta I_l}{(C_1 + C_2) \times f_{sw o}} \quad \text{if} \quad \Delta I_l < I_{avg_{fw}}$$ (6.12)

where $C_1$ and $C_2$ are the on-chip capacitances of the output filter in Figure 6.11. Therefore, the undershoot voltage will not depend on the lower switching frequency of the input stage, which is the main idea behind the dual-frequency topology. If the positive load step size is larger than the freewheeling current, the output has to wait for the input stage to accumulate the deficit into the inductor (similar to the case of standard single-frequency buck converters, but better since only the deficit between the inductor current and the non-zero freewheeling current is needed), which introduces an additional component to the undershoot voltage. In this scenario, the worst-case undershoot voltage “$\Delta V_{us-wc}$” occurs at the last output of the converter (i.e. the least priority output) and can be approximated by:

$$\Delta V_{us-wc} \approx \frac{\Delta I_l}{(C_1 + C_2) \times f_{sw o}} + \frac{L (\Delta I_l - I_{avg_{fw}})^2}{2 \times (C_1 + C_2) \times (V_{in} - V_o)} \quad \text{if} \quad \Delta I_l > I_{avg_{fw}}$$ (6.13)

where $V_{in}$ is the input voltage, $V_o$ is the average of all the output voltages, and $L$ is the effective inductance of the input stage.

For negative load steps, the overshoot voltage is described by the same formula in Equation 6.12 irrespective of the freewheeling current level. The reason the overshoot is
described by a single equation that is not at all a function of the freewheeling current is because if the load step is negative, the inductor is disconnected from the load and its current escapes into the freewheeling switch, and thus the overshoot will just be determined by the load step size, the output capacitance, and the output switching frequency.

### 6.3.3 Interleaved Pulse-Skipping

The proposed comparator-based control shown in Figure 6.14 incorporates an interleaved pulse-skipping logic to improve dynamic response and light-load efficiency. The pulse-skipping logic details are shown in Figure 6.16 and the timing diagram of the scenarios where the $i^{th}$ output is served and where it is skipped are shown in Figure 6.17. The

![Diagram](image_url)

**Figure 6.16** The schematic diagram of the proposed interleaved pulse-skipping logic

operation is based on observing the output of the comparator “cmp”, which indicates whether the $i^{th}$ output needs energy in the current switching cycle. If it does not, the skipping
logic ensures that the $i^{th}$ output remains deactivated (i.e. skipped), and activates the $(i + 1)^{th}$ output instead. This mechanism greatly simplifies the design by eliminating the need for a minimum ON-time per cycle for each output, which otherwise would have been necessary as each output is activated only after the previous output is served. Additionally, by eliminating a minimum ON-time, the outputs can be regulated without limiting the maximum difference between their loads. Thus, unlike other SIMO topologies [10, 11], this pulse-skipping mechanism enables handling scenarios where the difference between the loads is large. Also, it improves the dynamic performance during falling DVS and load transient events as the output charge can be dissipated much quicker due to skipping.

Figure 6.17 The operation waveforms of the proposed interleaved pulse-skipping logic and for scenarios where the $i^{th}$ output is either served or skipped based on the states of the control comparator “cmp” and the skip comparator “skip_cmp”.

<table>
<thead>
<tr>
<th>$S_{o}(i-1)$</th>
<th>$S_{set}(i)$</th>
<th>$V_{cmp}(i)$</th>
<th>$S_{skip}(i)$</th>
<th>$S'_{Skip}(i)$</th>
<th>$R_{set}(i)$</th>
<th>$S_{o}(i)$</th>
<th>$S_{set}(i+1)$</th>
<th>$S_{o}(i+1)$</th>
</tr>
</thead>
</table>

Scenario where the $i^{th}$ Output is served

Scenario where the $i^{th}$ Output is skipped
Moreover, an additional comparator “skip_cmp” is used to compare the load “\(I_{o(i)}\)” of the \(i^{th}\) output to an arbitrary reference level “\(I_{th(i)}\)” such that when the load drops below that level, the \(i^{th}\) output is skipped for a number of cycles (set by the skipping counter), which effectively reduces the switching frequency, and thus improves light-load efficiency. However, to avoid the scenario of skipping all the outputs in a given switching cycle (which will cause a large increase in the freewheeling current), the signal “\(skip\_cycle\_select\_i\)” is used for the \(i^{th}\) output to select which output switching cycles during which this particular output is skipped. By interleaving the \(skip\_cycle\_select\_i\) signals for all the outputs, it is ensured that at least one output is activated in any given output switching cycle while preserving the pulse-skipping of all the outputs.

### 6.3.4 Dynamic Output Re-ordering

Due to the sequential nature of distributing energy to the outputs, the cross-regulation performance during rising DVS events at a given output is a strong function of the location of this particular output within the sequence. For instance, if a rising DVS event occurs at the last output in the sequence, accommodating it by serving the output for a longer period only affects the freewheeling current but none of the other outputs. However, if a rising DVS event occurs at an intermediate output in the sequence (say the 3\(^{rd}\) output), then all the following outputs have to wait for a longer period of time before they can be served, which causes cross-regulation transients at these outputs as illustrated in Figure 6.18(a). To circumvent this problem, dynamic output re-ordering is proposed. In this scheme, once a rising DVS command is issued to the output controller for a particular output, this output is temporarily shifted within the sequence to be served last in the switching cycle to ensure that extending its serving time in response to the DVS command does not affect all the other
outputs. However, once the control comparator associated with this particular output indicates that the output has arrived to its new reference level, the output is moved back to its initial location within the output sequence. This dynamic re-ordering of the outputs results in much improved cross-regulation performance during rising DVS events as shown in Figure 6.18(b).

Figure 6.18 Output waveforms for all the outputs with a rising DVS event occurring at the 3\textsuperscript{rd} output: (a) without dynamic output reordering, and (b) with the proposed dynamic output reordering.
6.4 Measurement Results

The proposed 4-output DF-DIMO converter with fully-integrated output filters is implemented in standard 65-nm CMOS technology. The die photo of the design is shown in Figure 6.19 with all the critical components highlighted, including the bond-wires used for the proposed 3rd-order output notch filters (two wires per output). The total area of the converter is 10.8 mm², where 7.2 mm² (~67% of the total area) is occupied by the 1.8V-rated on-chip capacitors used in the output filters (10 nF per output), while the rest of the area is
occupied by the input and output controllers, power switches, and input ringing suppression filters. Although all the outputs are at 1.2 V or less, 1.8V-rated capacitors were employed instead of the 1.2V-rated ones in order to minimize leakage and quiescent current and maximize efficiency. However, this comes at the expense of a hefty area penalty (i.e. 1.8V-rated capacitors occupy about double the area of the 1.2V-rated ones). Thus, this tradeoff must be carefully studied based on what is more important for each application. The input stage switching nodes “$V_{sw1<1>}$” and “$V_{sw1<2>}$”, inductor currents “$I_{ind1<1>}$” and “$I_{ind1<2>}$”, and the output stage switching node “$V_{swo}$” are measured in steady-state with 20-MHz and

![Figure 6.20](image-url) Measured steady-state waveforms of one of the switching nodes of the dual-phase input stage, the inductor currents, and the output stage switching node. The average of the inductor current per input phase is 280 mA
100-MHz input and output switching frequencies respectively. The results are shown in Figure 6.20 (only one of the input switching nodes are shown for clarity), where the output switching node is sequentially transitioning to the various output levels, then to the freewheeling switch at the end of each cycle. To demonstrate the effectiveness of the 3rd-order notch output filters, each output is measured with all outputs delivering their full 250-mA load (worst case scenario). For comparison purposes, the measurement is also performed with the bond-wire inductors shorted such that the output filters are reduced to the single-capacitor filter topology. Both cases are shown in Figure 6.21, where the voltage ripple is reduced from 200 mV to 40 mV due to the action of the proposed filter topology. The dynamic operation of the converter is tested by applying a periodic half-to-full load step to one of the outputs as shown in Figure 6.22, while all the other outputs are at full loads. The measurement is performed with and without bypassing the error amplifier “EA” in the output stage controller for comparison purposes. The settling time is less than 85 ns with overshoot/undershoot of less than 110 mV when the EA is enabled, and less than 20 ns with no overshoot/undershoot when the EA is bypassed (no overshoot/undershoot is a characteristic of comparator-only controllers). Although the EA slows down the dynamic response and introduces overshoots/undershoots, it improves DC load regulation by eliminating any load-dependent offsets (100mV without the EA as in Figure 6.22). It is worth noting that in both cases, no cross-regulation transients are observed at all the other outputs, which is a characteristic of the dual-frequency topology due to comparator-based control, freewheeling current reserve, and fast output switching frequency [19-21].
Figure 6.21 Measured output voltage ripple at full load conditions: (a) with single-capacitor output filter, and (b) with the proposed bond-wire-based 3\textsuperscript{rd}-order notch output filter.
Figure 6.22 Measured load transient response: (a) with the error amplifier, and (b) with the error amplifier bypassed. The load steps are applied through on-chip loads with 1-ns rise and fall times.
Figure 6.23 Measured DVS response: (a) with rising and falling DVS events at the 3\textsuperscript{rd} output only, and (b) with simultaneous rising and falling DVS events at the 2\textsuperscript{nd}, 3\textsuperscript{rd}, and 4\textsuperscript{th} outputs.
Figure 6.24 Measured response of one of the outputs to a rising DVS event: (a) with no output reordering, and (b) with the proposed dynamic output reordering.
Figure 6.25 Measured steady-state results showing (a) the operation of the proposed interleaved pulse-skipping when the last 3 outputs are operating at light-load conditions, and (b) the operation with the outputs loaded differently from each other to demonstrate robust operation even with large differences between the loads.
To demonstrate DVS performance, the response of one of the outputs to a 0.5-V reference step is measured while all other outputs are at full load and the average freewheeling current regulated to 150 mA. The results are shown in Figure 6.23(a), where the output settles at the new level within 70 ns with no observable cross-regulation transients at the other outputs. Moreover, simultaneous DVS operation was measured with different voltage steps and different polarities at 3 of the outputs as shown in Figure 6.23(b), where excellent cross-regulation is still preserved even with multiple outputs changing simultaneously; thanks to the high output switching frequency and the freewheeling current. To demonstrate the impact of the proposed dynamic output reordering on cross-regulation, the rising DVS response of one of the outputs is measured with and without dynamic output reordering for comparison. As shown in Figure 6.24(a), there is a significant cross-regulation transient at the last output when a rising DVS event occurs at the 3rd output if dynamic output reordering is disabled. This is because the output sequence is not changing during the DVS event. However, this cross-regulation transient is reduced significantly as shown in Figure 6.24(b) when dynamic output reordering is enabled since the 3rd output is moved to the last spot during the transition to accommodate the DVS event, and once the event is over, the normal output order is restored.

To demonstrate the interleaved pulse-skipping operation at light loads, three of the outputs are loaded with 50 mA, while one output is loaded with 100 mA. The results are shown in Figure 6.25(a), where one pulse is always skipped in all the lightly-loaded outputs, which effectively reduces their switching frequency to 50 MHz to improve efficiency. As shown, although all the lightly-loaded outputs are skipped for one pulse, the pulses being skipped are interleaved between the outputs to ensure that there is at least one output being served in any given output switching cycle. Moreover, Figure 6.25(b) shows the results with
Figure 6.26 Measured efficiency of the proposed converter: (a) versus load current, and (b) versus output voltage.
the outputs loaded differently from each other, which demonstrates robust operation even in conditions where a large difference between the loads exists.

The converter’s measured efficiency versus load current and output voltage is reported in Figure 6.26(a) and Figure 6.26(b) with different output filter configuration, along with an ideal LDO for comparison. The peak efficiency with the 3rd-order notch filters and the single-capacitor filters are 74% and 76% respectively. The drop in efficiency is due to bond-wire inductors conduction losses. Moreover, as shown in Figure 6.26(a), interleaved pulse-skipping improves efficiency by about 7% at 20-mA load.

The converter’s estimated loss breakdown at an intermediate load point is shown in Table 6.1. This shows that significant losses can be reduced with better on-chip input and output power routing, which was limited by the sheet resistance of the top-metal layer of the particular flavor of the technology used for this implementation. In other flavors of this technology, a thicker top-metal layer is available with 3-times less sheet resistance, which can contribute to improving efficiency. Moreover, better efficiency can be achieved using inductors with lower DCR and ACR, and if larger ripple voltage can be tolerated, the output

<table>
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<tr>
<th>Conditions:</th>
<th>Input stage</th>
<th>Output stage</th>
<th>Control circuits (Quiescent loss)</th>
<th>Total loss</th>
<th>Total output power</th>
<th>( \eta )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simulated</td>
<td>Power switches loss (conduction and switching)</td>
<td>Inductor loss (DCR=27 mΩ, ACR=3 Ω)</td>
<td>Power switches loss (conduction and switching)</td>
<td>Bond-wire filter loss (0.2Ω)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>50 mW</td>
<td>7 mW</td>
<td>70 mW</td>
<td>8 mW</td>
<td>4 mW</td>
<td>158 mW 480 mW 75.2%</td>
</tr>
<tr>
<td></td>
<td>(31.6%)</td>
<td>(4.4%)</td>
<td>(44.3%)</td>
<td>(5.1%)</td>
<td>(2.6%)</td>
<td></td>
</tr>
<tr>
<td>Measured</td>
<td></td>
<td></td>
<td></td>
<td>170 mW</td>
<td>480 mW</td>
<td>73.9%</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* Includes on-chip power routing, and package parasitics

**Table 6.1** Estimated loss breakdown of the DF-DIMO converter
Figure 6.27 Measurement setup used to characterize the proposed DF-DIMO converter
Figure 6.28 Printed circuit board used to characterize the proposed DF-DIMO converter
switching frequency can be reduced to improve efficiency at the expense of dynamic performance.

The measurements setup and the PCB used to test the converter are shown in Figure 6.27 and Figure 6.28, respectively, along with a performance summary of the DF-DIMO converter and how it compares to recently-reported topologies in Table 6.2.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Topology (Block)</td>
<td>DF SIMO</td>
<td>DF SIMO</td>
<td>SIMO</td>
<td>SIMO (4 active)</td>
<td>SIMO (4 active)</td>
<td>SIMO (4 active)</td>
<td>SIMO (4 active)</td>
</tr>
<tr>
<td># of Outputs</td>
<td>4</td>
<td>4</td>
<td>5</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>1.6–2.5 V</td>
<td>1.6–2.5 V</td>
<td>2.5 V</td>
<td>1.6 V</td>
<td>1.2 V</td>
<td>1.2 V</td>
<td>2.5 V</td>
</tr>
<tr>
<td>Output Voltage Range</td>
<td>0.6–1.2 V (4 outputs)</td>
<td>0.6–1.2 V (1 output)</td>
<td>1.1–2 V (1 output)</td>
<td>0.9 V–1.2 V</td>
<td>1.5 V–1.8 V</td>
<td>1.25–1.3 V</td>
<td>1.8 V–2.5 V</td>
</tr>
<tr>
<td>Maximum Load (Total)</td>
<td>1 A</td>
<td>1.10 mA</td>
<td>1.6 A</td>
<td>1.15 A</td>
<td>8 mA</td>
<td>90 mA</td>
<td>142 mA</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>30 MHz (input stage)</td>
<td>2 MHz (input stage)</td>
<td>2 MHz (input stage)</td>
<td>1 MHz (single frequency)</td>
<td>1.2 MHz (single frequency)</td>
<td>30 MHz (single frequency)</td>
<td>100 MHz (single frequency)</td>
</tr>
<tr>
<td>Inductor Range</td>
<td>20 µH</td>
<td>240 µH</td>
<td>All</td>
<td>15 µH</td>
<td>4.7 µH</td>
<td>2.2 µH</td>
<td>None</td>
</tr>
<tr>
<td>Output Capacitors</td>
<td>5.1 nF/output</td>
<td>All-On Chip</td>
<td>2.2 nF/output</td>
<td>2.5 nF</td>
<td>1 µF</td>
<td>4.7 µF</td>
<td>10 µF/output</td>
</tr>
<tr>
<td>Silicon Area</td>
<td>10.3 mm² (7.2 mm² of that is for the output capacitors)</td>
<td>10.3 mm² (7.2 mm² of that is for the output capacitors)</td>
<td>5.4 mm²</td>
<td>1.86 mm²</td>
<td>0.16 mm²</td>
<td>1.6 mm²</td>
<td>0.73 mm²</td>
</tr>
<tr>
<td>Maximum Output Voltage Ripple</td>
<td>40 mV</td>
<td>50 mV</td>
<td>40 mV</td>
<td>40 mV</td>
<td>50 mV</td>
<td>20 mV</td>
<td>16 mV</td>
</tr>
<tr>
<td>Peak Efficiency</td>
<td>70%</td>
<td>70%</td>
<td>70%</td>
<td>65%</td>
<td>60%</td>
<td>74%</td>
<td>70%</td>
</tr>
</tbody>
</table>

### DVS

<table>
<thead>
<tr>
<th>Load Step (ΔL)</th>
<th>Half-to-Full Load (ΔL = 135 nA)</th>
<th>Half-to-Full Load (ΔL = 75 nA)</th>
<th>Half-to-Full Load (ΔL = 250 nA)</th>
<th>Half-to-Full Load (ΔL = 8 mA)</th>
<th>Half-to-Full Load (ΔL = 75 nA)</th>
<th>Half-to-Full Load (ΔL = 250 nA)</th>
<th>Half-to-Full Load (ΔL = 8 mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overshoot / Undershoot</td>
<td>None without EA</td>
<td>None without EA</td>
<td>None without EA</td>
<td>None without EA</td>
<td>None without EA</td>
<td>None without EA</td>
<td>None without EA</td>
</tr>
<tr>
<td>Load Dependent Offsets</td>
<td>100 mV without EA</td>
<td>None with EA</td>
<td>100 mV with EA (Charge-based control)</td>
<td>150 mV (no EA)</td>
<td>Not Reported</td>
<td>105/65 mV</td>
<td></td>
</tr>
<tr>
<td>Settling Time</td>
<td>20 ns without EA</td>
<td>80 ns without EA</td>
<td>30 µs</td>
<td>100 µs</td>
<td>120 µs</td>
<td>Not Reported</td>
<td>Not Reported</td>
</tr>
<tr>
<td>Cross Regulation</td>
<td>None observed</td>
<td>None observed</td>
<td>None observed</td>
<td>None observed</td>
<td>None observed</td>
<td>None observed</td>
<td>None observed</td>
</tr>
</tbody>
</table>

**Table 6.2: Performance summary & comparison**

Compared to low-frequency SIMOs such as in [9, 13], the DF-DIMO requires much smaller inductance, uses only on-chip output capacitors, and has much faster dynamic response. Compared to high-frequency single-output buck topologies with on-chip passives such as in [24], the DF-DIMO can operate at higher input voltages (1.8 V instead of 1.2 V) while achieving similar efficiency because its lower input switching frequency allows using...
1.8V-rated power switches with reasonable switching losses. Moreover, it achieves 20-times faster DVS response with lower output switching frequency (3-times lower than [24]). Compared to high-frequency single-output switched-capacitor topologies such as in [5, 27], the DF-DIMO achieves 60-times faster DVS response compared to [5] since no dynamic topology reconfiguration is needed to preserve efficiency at different conversion ratios or load currents. Moreover, the DF-DIMO supports higher load current per output than [27] with better efficiency at almost the same switching frequency. Finally, compared to the DF-SIMO topology in [20], the DF-DIMO reduces the inductance required by a factor of 38, delivers an order of magnitude higher output power with half the voltage ripple. It also has faster falling DVS response due to pulse-skipping.
CHAPTER 7

CONCLUSION AND FUTURE WORK

A 1-A, 4-output DF-DIMO topology that can be used to realize multiple on-chip dynamic power supplies for multi-core DSPs is introduced in this dissertation. Due to its dual-phase 20-MHz input stage, only two 200-nH off-chip inductors are needed, while its integrated 3rd-order bond-wire-based notch output filters enable up to 250-mA load per output with less than 40-mV of voltage ripple. The 100-MHz comparator-controlled output stage and the 20-MHz freewheeling-current-controlled input stage, along with dynamic output reordering and interleaved pulse-skipping result in ultra-fast dynamic response with improved cross-regulation, DC load regulation, and light-load efficiency. There are several options to extend this work for future research.

7.1 Implementing the DF-DIMO Converter in Flip-chip Package Process

![Diagram](https://via.placeholder.com/150)

**Figure 7.1** The small inductors in the 3rd order notch filters can be implemented with the routing traces on the package substrate in flip-chip package
For the design in flip-chip packages, there are no bond-wires available, but the small inductors in the 3rd order notch filters can be implemented with the routing traces on the package substrate as shown in Figure 7.1, since the inductance of these routing traces can be made in the range of few nano-Henries which is at the same level of the inductances used in this DF-DIMO design. Moreover, the routing impedance for some of the pins in this package can be made very small. If these pins are designed to be the inputs of the power converter, the area of the on-chip input ringing suppression filters can be significantly reduced.

7.2 Multi-level input Stage for Inductor Current Ripple Reduction

In dual-frequency topology, the freewheeling current must be regulated to half of the inductor current ripple to maintain regulation, and a higher freewheeling current can

![Diagram of multi-level input stage](image)

**Figure 7.2** A multi-level input stage can be employed in the DF-DIMO converter to reduce the inductor current ripple without using a larger inductor.
significant degrades the efficiency due to excessive conduction loss. A multi-level input stage can be employed to reduce the inductor current ripple without using a larger inductor as shown in Figure 7.2, where the voltage regulated across the charge transfer capacitor $C_{tf}$ is always equal to half of the input voltage $V_{in}/2$. If the average voltage of the output switching node is higher than $V_{in}/2$, the input switching node will oscillate between $V_{in}$ and $V_{in}/2$. Otherwise, it will oscillate between $V_{in}/2$ and ground level. Therefore, the inductor current ripple can be significantly reduced due to smaller voltage across the inductor during energizing and de-energizing. In addition, since the voltage across the drain and source of the input device is reduced to half of the input voltage, the reliability of the input device can be improved.

### 7.3 DF-DIMO with Coupled Integrated Magnetic Inductors

To further reduce the total area of the system, the integrated magnetic inductor (~200nH) can be employed in the DF-DIMO to replace the off-chip inductors. As shown in Figure 7.3, these inductors are implemented on top of the metal layers and connect to the top metal through magnetic vias, where a coupled inductor pair can also be easily implemented by using this technology [36]. If the coupled inductors with proper coupling coefficient are employed in the DF-DIMO converter, higher efficiency or better transient response can be achieved.
Figure 7.3 The integrated magnetic inductor can be employed in the DF-DIMO converter to replace the off-chip inductors to further reduce the total area of the system
REFERENCE:


