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Logic element architecture for generic logic chains in programmable devices

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Logic element architecture for generic logic chains in programmable devices

Abstract

A reconfigurable device includes an arrangement of a plurality of cells and routing resources for transmitting signals between the cells. The plurality of cells comprises carry-select reuse cells, each of the carry-select reuse cells configured to provide for performing non-arithmetic operations using a reuse arithmetic carry chain interconnecting adjacent cells.

Disciplines

Electrical and Computer Engineering



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(54) **LOGIC ELEMENT ARCHITECTURE FOR
GENERIC LOGIC CHAINS IN
PROGRAMMABLE DEVICES**

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USPC **716/117; 716/121; 716/128**

(58) **Field of Classification Search** **716/117,**
716/121, 128
See application file for complete search history.

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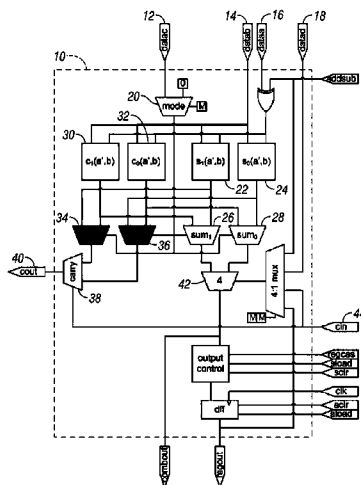
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(57) **ABSTRACT**

A reconfigurable device includes an arrangement of a plurality of cells and routing resources for transmitting signals between the cells. The plurality of cells comprises carry-select reuse cells, each of the carry-select reuse cells configured to provide for performing non-arithmetic operations using a reuse arithmetic carry chain interconnecting adjacent cells.

14 Claims, 8 Drawing Sheets



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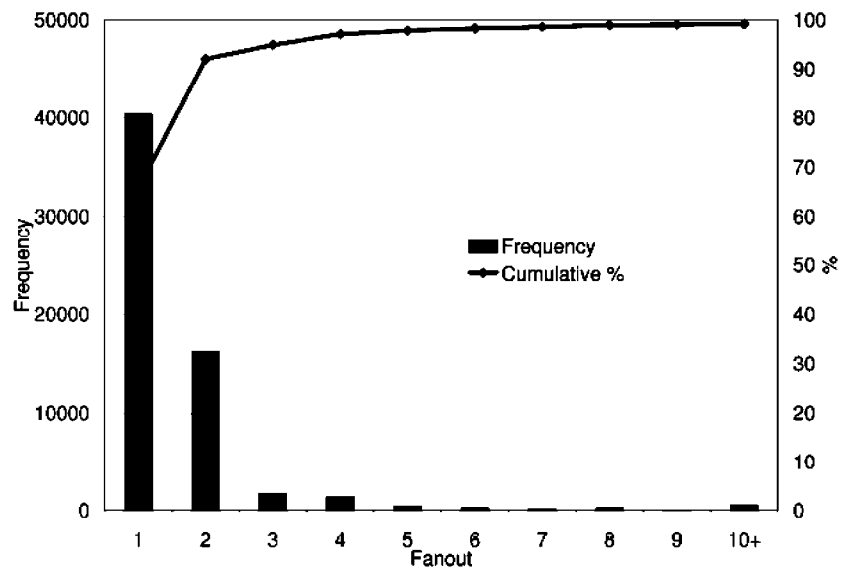


FIG. 1

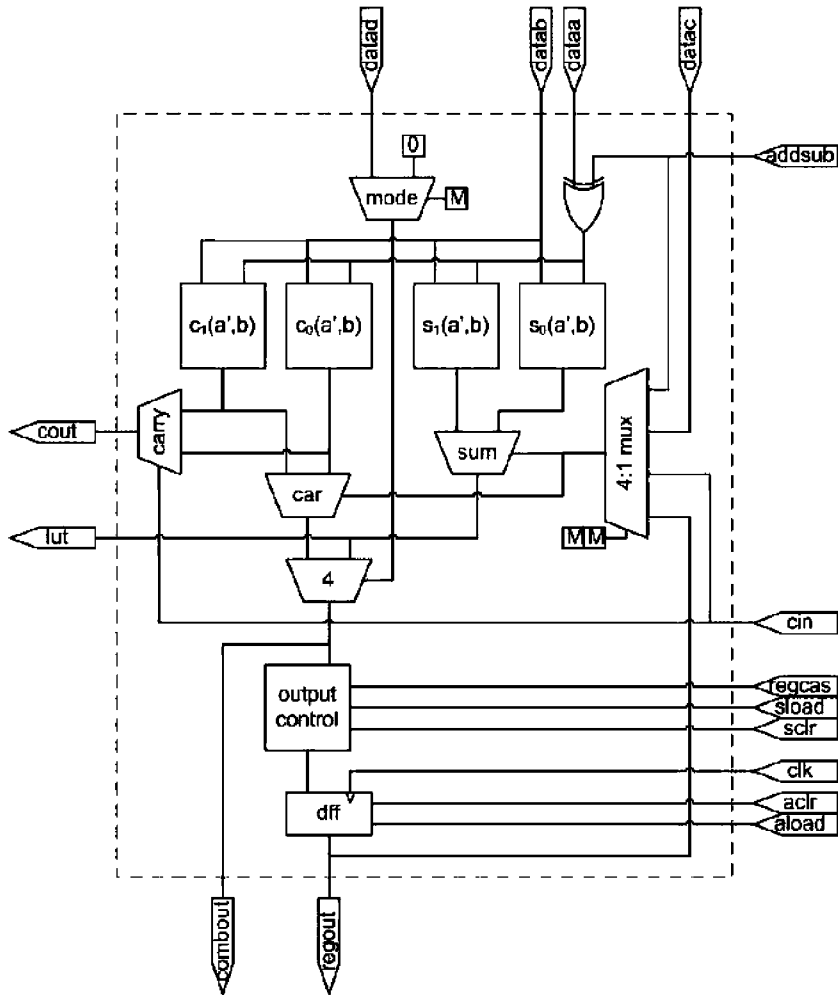


FIG. 2 (PRIOR ART)

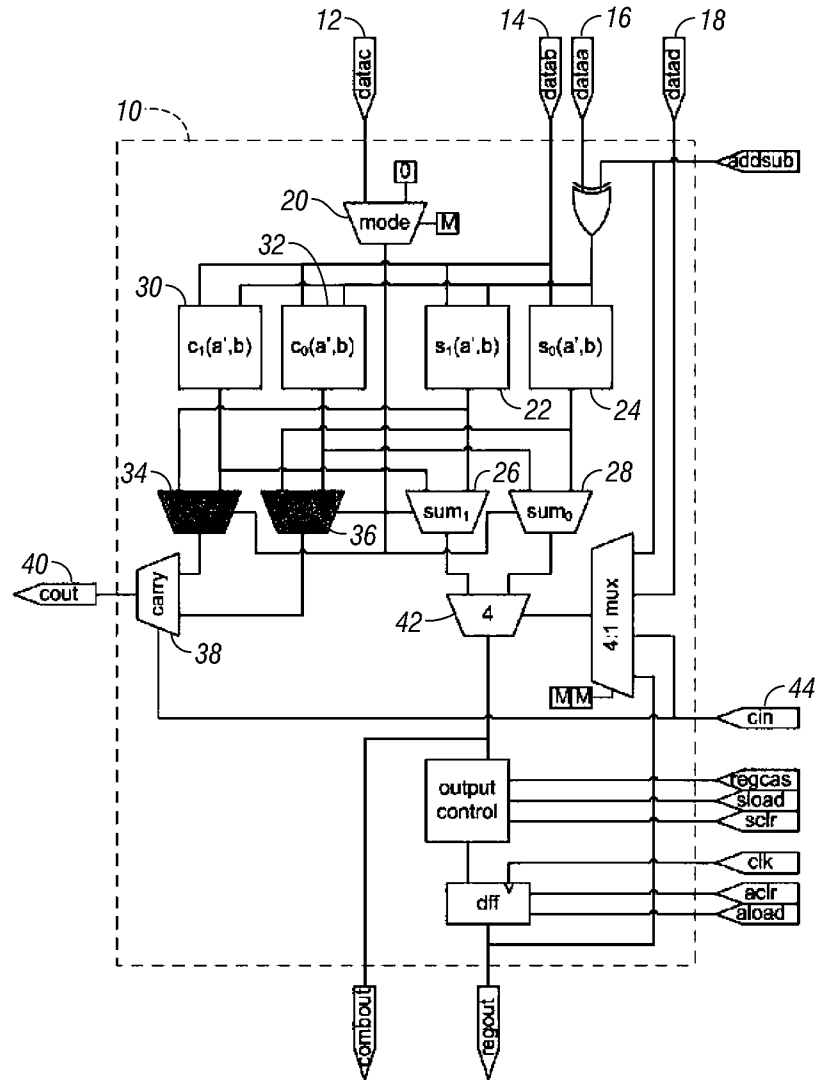


FIG. 3

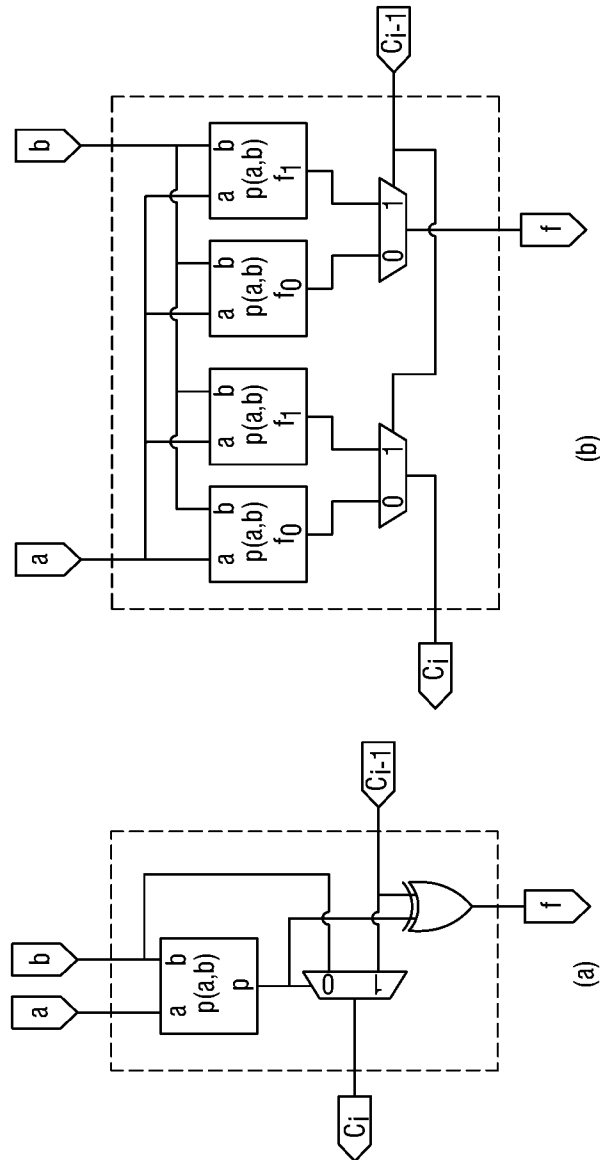


FIG. 4

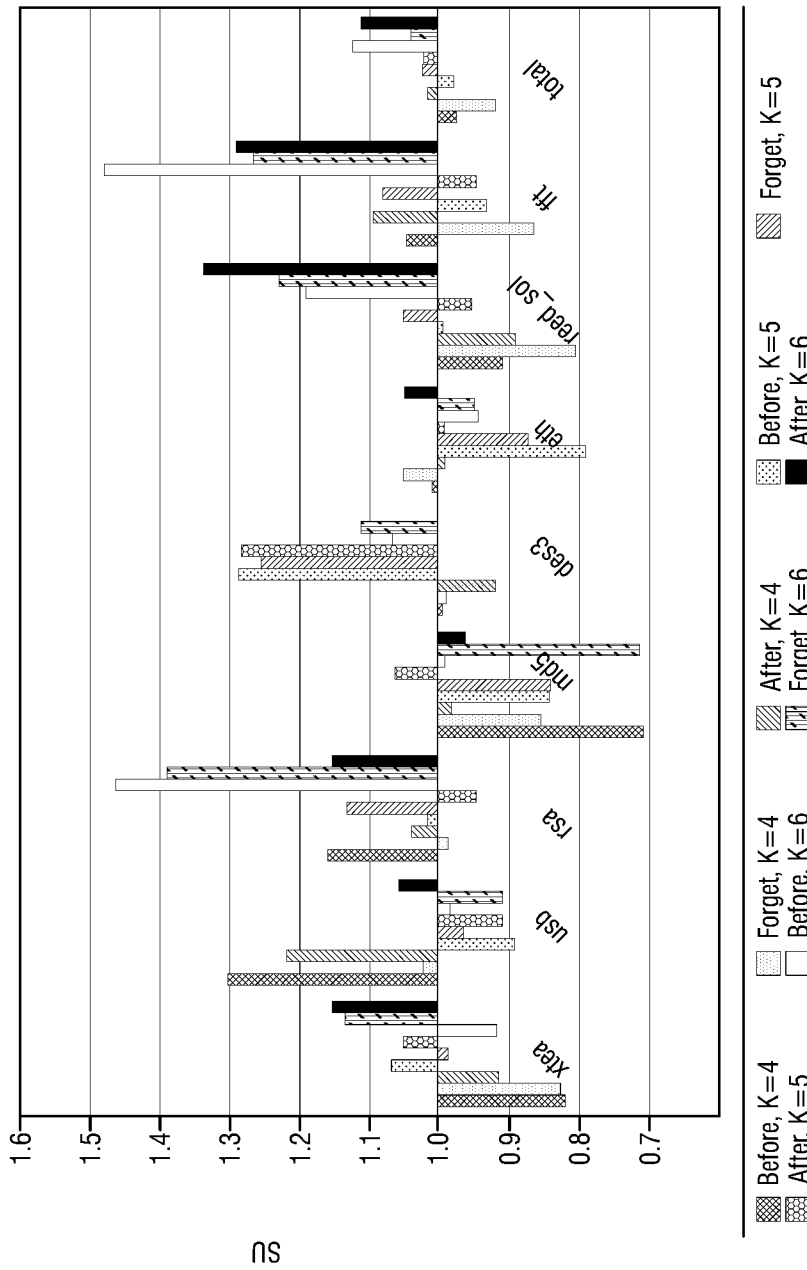


FIG. 5

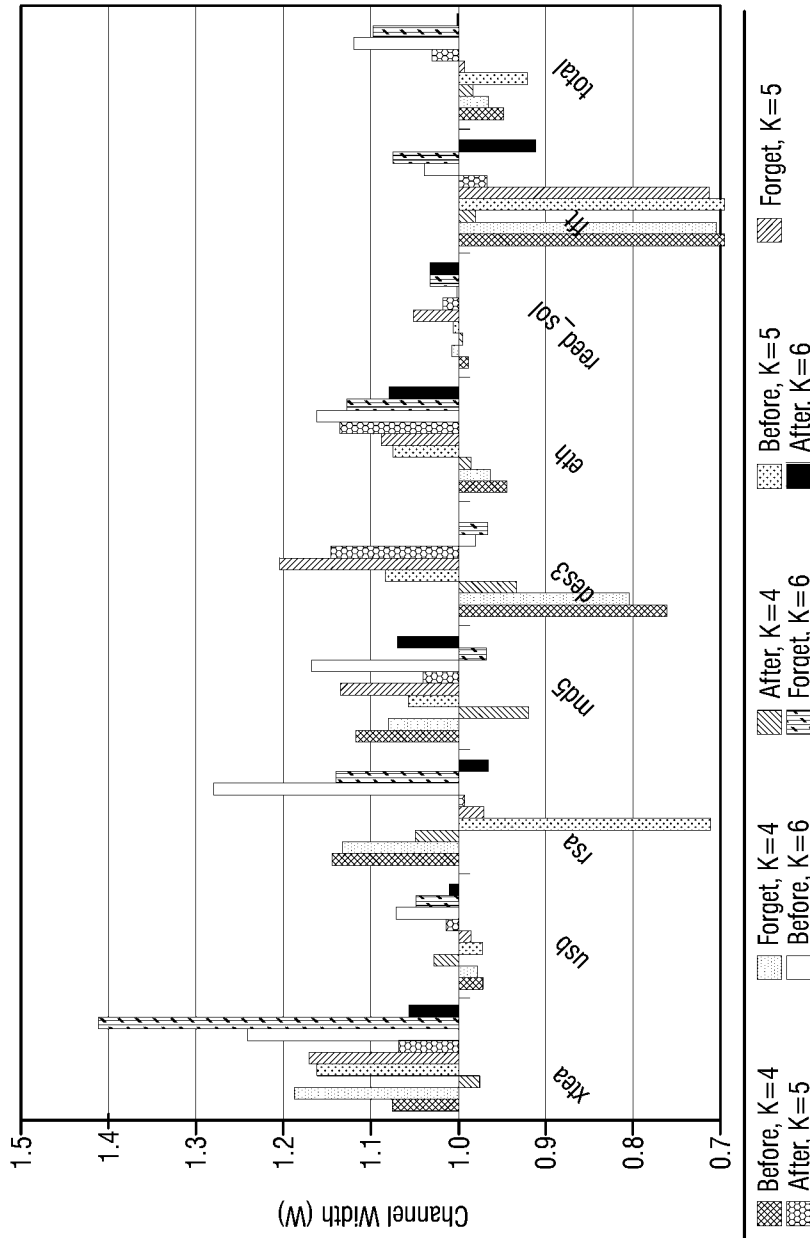


FIG. 6

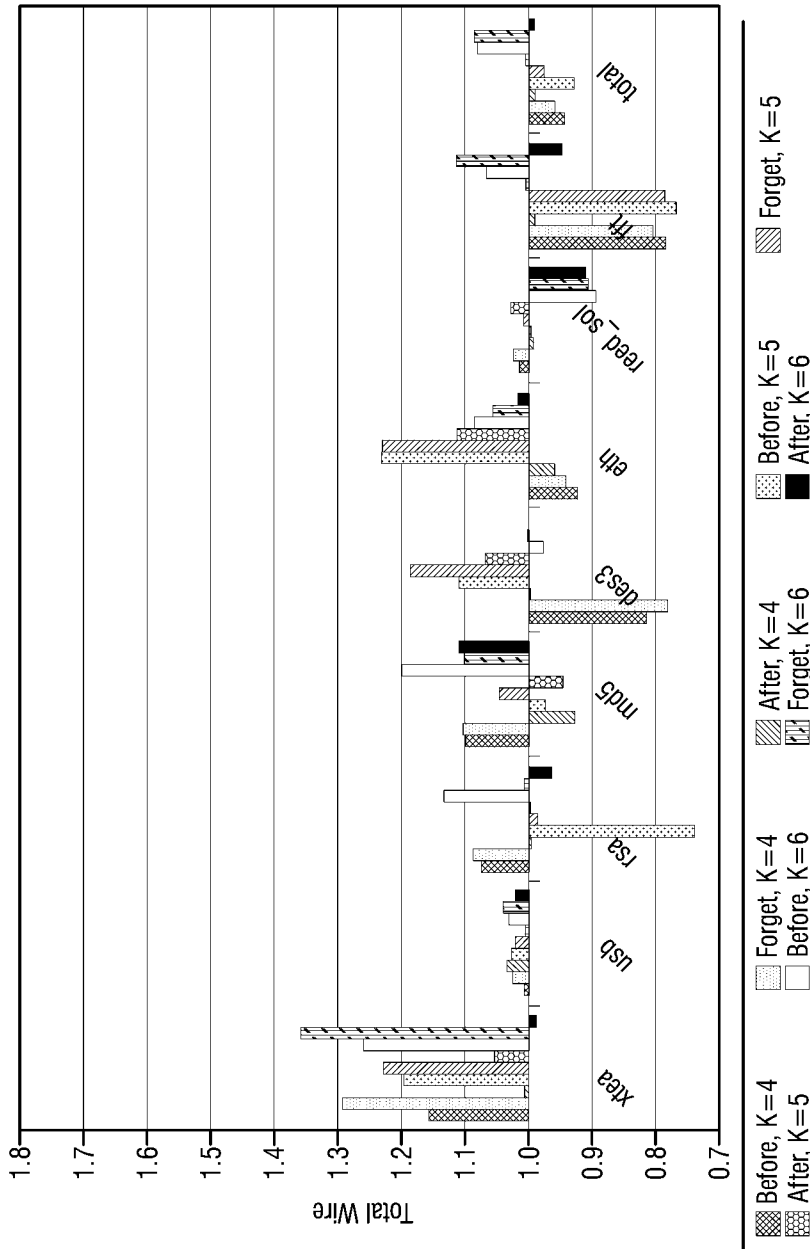


FIG. 7

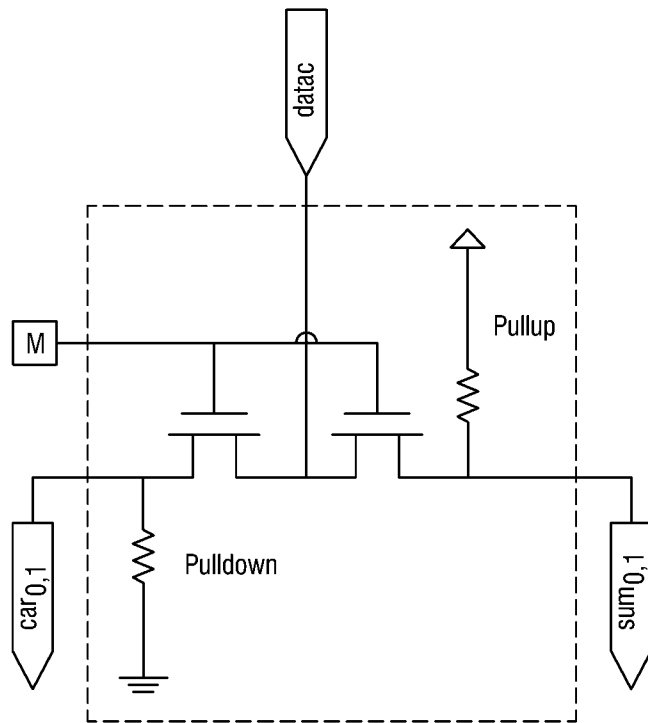


FIG. 8

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LOGIC ELEMENT ARCHITECTURE FOR GENERIC LOGIC CHAINS IN PROGRAMMABLE DEVICES

GRANT REFERENCE

This invention was made with government support under Grant No. CCF0311061 awarded by NSF. The government has certain rights in the invention.

FIELD OF THE INVENTION

The present invention relates to reconfigurable fabrics, and more particularly to carry chains used in reconfigurable fabrics.

BACKGROUND OF THE INVENTION

Carry chains in reconfigurable fabrics serve a very important, yet very specific purpose: to facilitate the efficient implementation of arithmetic functions. Carry chains allow arithmetic functions to bypass the performance-costly general routing array. However, if a carry chain is not used for an arithmetic function, it becomes a superfluous adjacent cell interconnection resource. There are several challenges to carry chain reuse for non-arithmetic chains, some architectural, while others are based on tool support. What is needed is a modified cell design that facilitates carry chain reuse.

Therefore, it is a primary object, feature, or advantage of the present invention to improve over the state of the art.

It is a further object, feature, or advantage of the present invention to provide a modified cell design that facilitates carry chain reuse.

It is a still further object, feature, or advantage of the present invention to provide a means of improving design performance at a minimal cost.

Another object, feature, or advantage of the present invention is to provide a means of improving design performance in a manner which is transparent to a designer.

One or more of these and/or other objects, features, or advantages of the present invention will become apparent from the specification and claims that follow.

BRIEF SUMMARY OF THE INVENTION

Commercially available SRAM-based Field Programmable Gate Arrays (FPGAs) have gained traction in the engineering community as a highly flexible and reusable embedded system design tool. FPGAs are also increasingly being incorporated into production designs because their programmability allows the addition of functionality, hardware fixes/upgrades, or fault tolerance by way of scrubbing or elimination of faulty components. Due to their increasing inclusion in deployed systems, the need to fully utilize every architectural resource is imperative so as to close the speed, area, and power consumption gap between FPGAs and ASICs. The carry chain is one resource that has yet to be exploited to its full capacity.

According to one aspect of the present invention, a reconfigurable device includes an arrangement of a plurality of cells and routing resources for transmitting signals between the cells. The plurality of cells comprises carry-select reuse cells, each of the carry-select reuse cells configured to provide for performing non-arithmetic operations reusing an arithmetic carry chain interconnecting adjacent cells.

According to another aspect of the present invention, a reconfigurable device including an arrangement of a plurality

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of cells and routing resources for transmitting signals between the cells. The plurality of cells comprises carry-select reuse cells, each of the carry-select reuse cells comprising carry chain elements, look up tables, and sequential logic and wherein the carry chain elements being configured to provide for performing non-arithmetic operations reusing an arithmetic carry chain interconnecting adjacent cells.

According to another aspect of the present invention, a device has an architecture which includes an arrangement of a plurality of cells and routing resources for transmitting signals between the cells. The plurality of cells includes carry-select reuse cells, each of the carry-select reuse cells comprising carry chain elements, look up tables, and sequential logic and wherein the carry chain elements being configured to provide for performing arithmetic operations and being further configured for performing non-arithmetic operations reusing an arithmetic carry chain interconnecting adjacent cells.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates distribution of net fanout.

FIG. 2 is a schematic of a carry-select traditional cell.

FIG. 3 is a schematic of a carry-select reuse cell.

FIG. 4 is schematic of a propagate-generate and carry-select addition logic.

FIG. 5 is a graph illustrating speedup of reuse flows over unmodified flow for LUT of 4, 5, and 6 inputs.

FIG. 6 is a graph illustrating required FPGA channel width of reuse flows over unmodified flow for LUT of 4, 5, and 6 inputs.

FIG. 7 is a graph illustrating total routed wire length for reuse flows over unmodified flow for LUT of 4, 5, and 6 inputs.

FIG. 8 is a schematic of a static mode output multiplexer.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Applications vary greatly from one to another—DSP applications are heavily arithmetic in nature, while many security algorithms are based on Boolean logic and use chains sparingly. For instance, an FFT is dominated by addition and subtraction with 57.6 percent cells in chains, while DES3, despite its complexity, predominately uses tabular look-ups with only 0.8 percent chain cells. FIG. 1 shows an aggregate distribution of net fanout for a sampling of designs available at OpenCores [4]. Greater than 60 percent of the nets in the designs are a direct connection between adjacent logic cells.

Carry chain reuse is defined as a logic chain that has been converted to use the arithmetic chain as a fast interconnect structure between adjacent cells. This forces these cells to be placed next to each other during place and route (PNR), and eliminates the need for that connection to traverse a configurable routing structure. In general, this sampling of designs seems to underutilize carry chains and could possibly benefit from their reuse.

This work presents a modified cell design that facilitates carry chain reuse. Post-technology map experiments show how reuse can benefit all applications. The academic tool flow of SIS [5], ChainMap [7], and VPR [2] is used to measure the effect of chain reuse on routing utilization and maximum clock frequency. The delimiting performance factors are identified and indicate that incorporating tool support into the design flow and making small changes to cell design have the ability to improve design performance at minimal cost and transparently to the designer.

A hardwired connection has been allocated in the Altera Stratix architecture [1] that is capable of connecting LUTs residing in the same block in a chain. This has the advantage of avoiding general routing for Boolean chains of up to 10 LEs, the size of a block in the Stratix architecture. The LUT chain is mapped by Quartus during PNR according to undisclosed metrics. Their functionality is similar to that of the architecture proposed by this work. The major difference between the approaches is that the LUT chain function can be replaced by a reusable carry chain. It is important to note that the Stratix II/III architectures appear to have discontinued the LUT chain.

FPGAs use ripple-carry schemes, or slight variations thereof, for area efficient arithmetic computation. The Xilinx Virtex series FPGAs are prime examples of highly-optimized ripple-carry use in commercial reconfigurable fabrics, using their LUT logic to provide a propagate signal as the selection input of a multiplexer choosing between generate and cell carry-in (cin) [6], as shown in FIG. 4(a). The Altera Stratix also uses ripple-carry as its base carry method, providing for a 2-level chain for Stratix, and parallel ripple-chains with LUT logic and dedicated full adders for the Stratix II [1]. The Stratix is based on the carry-select version of carry computation. Each multiplexer in FIG. 4(b) chooses between precomputed sum (f) and carry out (c_{i-1}) based on the cell carry in (c_{i-1}). The carry-select scheme in Stratix directly facilitates chain reuse. The carry in to each cell is directly mapped to the selection input of a multiplexer choosing between 2-LUTs. Logically, the carry in serves as the 3rd input in a 3-LUT meaning that any LE configured as a 3-LUT can use the native architecture to reuse the carry chain.

This invention is a Stratix-inspired reuse cell design for full-width LUT output. A K-LUT describes the ability of an LUT to implement any K-input Boolean function. Thus, a 4-LUT implements all Boolean operations with 4 inputs. Traditional carry-select based LEs working in random logic (normal) mode implement one K-input, 1-output function, and in arithmetic mode implement two independent (K-1)-input, 1-output functions with K-1 shared inputs. This invention supports the traditional normal and arithmetic modes, and in addition, provides the capability for a K-input, 2-output function.

Tool support for carry chain synthesis is limited. Current software packages, such as Altera Quartus II and Xilinx ISE, identify arithmetic carry chains through high-level HDL macros and primitives. The Xilinx V2P library guide denotes how wide homogeneous Boolean expressions (e.g. 16-input AND) can be formed using the carry chain, but synthesis does not identify and implement all such components, nor are the primitives recognized by ISE v8.2. The only recourse is for the designer to implement such expressions using low level LUT and carry chain primitives. The most common academic synthesis tool, SIS [5] doesn't support arithmetic chains in its internal representation.

FIG. 2 shows a rendition of the LE, similar to the stratix_1cell LE primitive, dubbed the traditional cell that will be used as the point of comparison to the reuse architecture depicted in FIG. 3. Several modifications have been made to the traditional cell that preserve its functionality and facilitate chain reuse. In the following description, dataa' will be used to refer to the output of the XOR gate with inputs dataa and addsub, while x will be used to denote an ambiguous component or signal.

In FIG. 3, a reuse cell 10 is shown. Data inputs datac 12, datab 14, dataa 16, datad 18, and cin 44 are shown. A mode multiplexer 20 is provided which receives input from datac 12 and may be used to set arithmetic or non-arithmetic mode. A

possible implementation of multiplexer 20 is shown in FIG. 8. LUTs s_1 22 and s_0 24 are shown, and serve the role of computing the traditional arithmetic sum for the cases when the carry in 44 is a binary 1 or 0. Sum multiplexers 26, 28 are provided and multiplexer 4 is used to compute a sum. Carry chain elements are also shown. LUTs c_1 30 and c_0 32 serve the role of computing the traditional arithmetic sum for the cases when the carry in cin 44 is a binary 1 or 0, and pass results through multiplexers car₁ 34 and car₀ 36. A carry multiplexer 38 is also shown which provides the carry output cout 40.

In arithmetic mode, the traditional cell computes the sum of dataa' and datab using LUTs s_1 and s_0 and the sum multiplexer, whose result is passed through multiplexer 4. The reuse cell on the other hand, passes each of the sum LUT values through a level of multiplexers and uses 42 (multiplexer 4) to compute sum. This is functionally equivalent when the mode multiplexer is set in arithmetic mode (i.e. static output). Similarly, carry computation is performed after allowing the LUT results to pass through multiplexers car₁ 34 and car₀ 36. Like the traditional design, carry computation is completed once the carry in to the cell is available. The additional level of multiplexing in the reuse design institutes a delay on the carry once dataa' and datab 14 become available. Only the first cell in a carry chain is affected because it is the only one dependent on the arrival of routing inputs. It is assumed that in an synchronous design all routing inputs become available at the same time, causing the carry chain to be the critical path of the circuit. All cells in the chain, with the exception of the first, have computed the carry for both cin conditions before the arrival of cin to the carry multiplexer 38. The sum computation expects identical latency, while the carry latency only differs for the first cell in a chain. Arithmetic mode preserves cout=f(dataa', datab, cin).

The normal operating mode of both cells is appreciably different. In the traditional cell the mode multiplexer passes routing input datad to multiplexer 4, while the reuse cell the mode multiplexer 20 passes datac to the car_x (34, 36) and sum_x (26, 28) multiplexers—a slight difference allowing the cout=f(dataa', datab, datac, cin) for non-arithmetic chains. The combout function is computed similarly in both cell designs, the difference being that the LUT mask is rearranged in the reuse cell. In arithmetic mode the carry and sum LUT outputs must pass through the car_x (34, 36) and sum_x (26, 28) multiplexers without performing a computation, which causes the middle nibbles of the 4-LUT mask to be interchanged in normal mode, as presented in the reuse mask in Table 3 and the traditional mask in Table 4. This is an innocuous change easily dealt with at the technology mapping stage. In summary, no extra delays are introduced in the reuse cell for Boolean operations, the cout can accommodate a f(dataa', datab, datac, cin), and the combout can be the same function as the traditional cell of three general inputs and an input from the 4:1 multiplexer. The 4:1 multiplexer options include an external data input, datax, cin, the register feedback of the cell, regout, and addsub. The only functionality difference between the two cells is the value of datax (datad for reuse, datac for traditional).

TABLE 3

inputs			normal		arithmetic	
cin/datad 44/18	datac 12	datab 14, data 16	comb- out 40	cout 40	comb- out 40	cout 40
0	0	xx	c_0 32	c_0 32	s_0 24	c_0 32
0	1	xx	s_0 24	s_0 24	s_0 24	c_0 32

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TABLE 3-continued

inputs			normal		arithmetic	
cin/datad 44/18	datad 12	datad 14, data 16	comb- out	cout 40	comb- out	cout 40
1	0	xx	c ₁ 30	c ₁ 30	s ₁ 22	c ₁ 30
1	1	xx	s ₁ 22	s ₁ 22	s ₁ 22	c ₁ 30

TABLE 4

inputs			normal		arithmetic	
datad 18	cin/datad 44/12	datad 14, data 16	comb- out	cout 40	comb- out	cout 40
0	0	xx	s ₀ 24	c ₀ 32	s ₀ 24	c ₀ 32
0	1	xx	s ₁ 22	c ₁ 30	s ₁ 22	c ₁ 30
1	0	xx	c ₀ 32	c ₀ 32	s ₀ 24	c ₀ 32
1	1	xx	c ₁ 30	c ₁ 30	s ₁ 22	c ₁ 30

Custom circuit layout and simulation results for the reuse and traditional cell in Table 1 indicate that c_{out_0} , the initial cell in a chain, and the combout for all cells both suffer a 1.01x delay at 3.3 v 0.6 μm process technology. Intermediate cells, $c_{out_{n-1,1}}$, experience no increase in delay. R:T gives the ratio of the reuse cell delay and area to that of the traditional cell.

TABLE 1

	$\mu\text{m} \times \mu\text{m}$	c_{out_0}	$c_{out_{n-1,1}}$	combout
Reuse	97.95 \times 82.35	6.04 ns	3.50 ns	5.94 ns
Trad	97.95 \times 79.95	6.01 ns	3.49 ns	5.90 ns
R:T	1.03	1.01	1.00	1.01

A caveat of this work is that the layout results obtained are not necessarily representative of commercial cell implementations. The assumptions are that the traditional and reuse cell designs have been treated equally and that the performance of the reuse cell relative to the traditional cell can be adequately estimated by assessing an overall performance penalty when applicable. It is applicable during the first cout computation in a chain and the combout of every cell in the design. In the overall cell layout, area is dominated by the 20 SRAM configuration bits, D flip-flop, pass transistor 4-LUT structure, and the output control. In this context, the two additional 2:1 pass transistor multiplexers of the reuse cell yield a 1.03x area increase.

Combining this invention with a generic logic chain assignment method such as that presented in [7] allows FPGA LEs to have equal access to the fast chain resources ubiquitous in today's commercial architectures. In experiments presented in [8], HDL chains are preserved through synthesis and technology mapping (after, normal), through only synthesis (before), and not preserved (forget). Each circuit is mapped to an FPGA with the minimum amount of component and routing resources required for implementation. LUT widths of 4, 5, and 6 inputs are tested.

Speedup is defined as the ratio of the critical path delay of the reuse cell to that of traditional cell; higher speedup indicates a performance increase for the reuse cell. The effect of this invention on the average speedup of circuits, as depicted in FIG. 5, is approximately 1.05x, with a minimum of 0.73x and maximum of 1.45x witnessed. Increasing the width of the LUT, the current trend in commercial architectures, generally yields higher performance increases for the reuse cell.

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The change in channel width is defined as the ratio of the channel width of the reuse cell to that of the traditional cell; higher channel width ratio indicates a performance decrease for the reuse cell. FIG. 6 indicates that an increase in speedup for the reuse cell often comes at the cost of an increase in the FPGAs required channel width. The average change in channel width is a 1.05x increase with a minimum of 0.7x and maximum of 1.4x observed. This indicates that an increase in the routing resources of an FPGA is required if performance increases are to be reaped by the invention.

The change in total routed wire length is defined as the ratio of the total routed wire length of the reuse cell to that of the traditional cell; higher total routed wire length ratio indicates a performance decrease for the reuse cell. FIG. 7 indicates that an increase in speedup for the reuse cell often comes at the cost of a small increase in the FPGAs required total routed wire length. The average change in total wire is neutral, at 1.0x, with a minimum of 0.78x and maximum of 1.35x observed. This indicates that this invention more completely uses the routing resources offered by an FPGA.

The present invention provides a way to reuse arithmetic carry chains in FPGAs to offer benefits to non-arithmetic operations. A modified cell architecture based on the carry-select ripple chain is presented and shown to increase delay through the cell by 1.01x and increase utilization by 1.03x. Traditional functionality is preserved at minimum cost, and the added delay in the carry chain is only an issue at the first cell in a chain. The result is an architecture that is able to pass its full K-LUT value along the carry chain. To study the effect of chain reuse for a commercial design tool and architecture, the chain assignment technique presented in [7] and the rest of the academic design flow were used by [8] for four separate strategies of treating HDL based arithmetic chains. Speedup, channel width ratio, and total routed wire length ratio results indicate that circuits can benefit from this invention's inclusion in commercial FPGA architectures. While some circuits often simultaneously increase performance and decrease routing consumption, others may do quite the opposite. The success of the invention in a particular application may depend on the characteristics exhibited by the design, such as number of arithmetic chain cells, number of cells in the design, the average fanout of each net, and, most importantly, the chain assignment algorithm chosen.

Logic chains may use the carry chain as a 0 delay interconnection structure regardless of HDL macros. The post-place and route experiments show chain reuse has great potential based in this invention's ability to obviate the difference between arithmetic and non-arithmetic chains. At a time when FPGA vendors are increasing the width of the LUT from 4 to 5 to 6 inputs and beyond, this invention provides a basis to support chain operations that exceed the minimal requirements of simple arithmetic chains in an efficient and minimally invasive manner. Such support combats the underutilization caused by 3-input arithmetic operations using a 6-input LUT.

Carry chain reuse can be a valuable addition to reconfigurable architectures and their design flow. Results indicate that even with naive algorithms, a design/algorithm pair can be found that can potentially increase maximum clock frequency, with an observed maximum of 1.45x, and decrease routing consumption, with an observed minimum of 0.7x, for the presented circuits. It is another step toward fully harnessing the complete computing capacity of FPGAs.

Therefore a configurable device which was carry chain reuse cells has been disclosed. The present invention contemplates numerous variation options and alternatives within the spirit and scope of the claimed invention.

All references listed are herein incorporated by reference in their entirety.

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What is claimed is:

1. A reconfigurable device including: an arrangement of a plurality of cells and routing resources for transmitting signals between the cells, wherein the plurality of cells comprises carry-select reuse cells, each of the carry-select reuse cells configured to provide for performing non-arithmetic operations using a reuse arithmetic carry chain interconnecting adjacent cells when a non-arithmetic mode input is received to provide a non-arithmetic mode and further configured to perform arithmetic operations using the reuse arithmetic carry chain when an arithmetic mode input is received to provide an arithmetic mode, wherein in the arithmetic mode, the carry-select reuse cells provide for two independent (K-1) input, 1-output functions with K-1 shared inputs; wherein in the non-arithmetic mode, the carry-select reuse cells provide for one K-input 1-output function; wherein the carry-select reuse cells further provide for a K-input, 2-output function; wherein K is a number of inputs of a lookup table associated with the carry select reuse cells. 30 35 40 45

2. The reconfigurable device of claim 1 wherein the reconfigurable device is a field programmable gate array (FPGA).

3. The reconfigurable device of claim 1 wherein the reuse arithmetic carry chain provides a carry output, the carry output providing an output of a function defined by the carry-select reuse cells for non-arithmetic chains. 50

4. The reconfigurable device of claim 1 wherein each of the carry-select reuse cells comprises carry chain elements, look up tables, and sequential logic configured to allow the reuse arithmetic carry chain to be used for arithmetic or non-arithmetic operations. 55

5. The reconfigurable device of claim 1 wherein the arrangement being at least partially determined by applying an algorithm for creating non-arithmetic chains. 60

6. A reconfigurable device including: an arrangement of a plurality of cells and routing resources for transmitting sig-

nals between the cells, wherein the plurality of cells comprises carry-select reuse cells, each of the carry-select reuse cells comprising carry chain elements, look up tables, and sequential logic and wherein the carry chain elements being configured to provide for performing non-arithmetic operations using a reuse arithmetic carry chain interconnecting adjacent cells when a non-arithmetic mode input is received to provide a non-arithmetic mode and further configured to perform arithmetic operations using the carry chain elements when an arithmetic mode input is received to provide an arithmetic mode, wherein in the arithmetic mode, the carry-select reuse cells provide for two independent (K-1) input, 1-output functions with K-1 shared inputs;

wherein in the non-arithmetic mode, the carry-select reuse cells provide for one K-input, 1-output function;

wherein the carry-select reuse cells further provide for a K-input, 2-output function; wherein K is a number of inputs of a lookup table associated with the carry select reuse cells.

7. The reconfigurable device of claim 6 wherein the reconfigurable device is a field programmable gate array (FPGA).

8. The reconfigurable device of claim 6 wherein the carry chain elements provide a carry output, the carry output providing an output of a function defined by the carry-select reuse cells for non-arithmetic chains.

9. The reconfigurable device of claim 6 wherein the arrangement being at least partially determined by applying an algorithm for creating non-arithmetic chains.

10. A device having an architecture comprising: an arrangement of a plurality of cells and routing resources for transmitting signals between the cells, wherein the plurality of cells comprises carry-select reuse cells, each of the carry-select reuse cells comprising carry chain elements, look up tables, and sequential logic and wherein the carry chain elements being configured to provide for performing arithmetic operations when an arithmetic mode input is received to provide a non-arithmetic mode and being further configured for performing non-arithmetic operations using a reuse arithmetic carry chain interconnecting adjacent cells when a non-arithmetic mode input is received to provide an arithmetic mode, wherein in the arithmetic mode, the carry-select reuse cells provide for two independent (K-1) input, 1-output functions with K-1 shared inputs;

wherein in the non-arithmetic mode, the carry-select reuse cells provide for one K-input, 1-output function;

wherein the carry-select reuse cells further provide for a K-input, 2-output function; wherein K is a number of inputs of a lookup table associated with the carry select reuse cells.

11. The device of claim 10 wherein the device is a field programmable gate array (FPGA).

12. The device of claim 10 wherein the carry chain elements provide a carry output, the carry output providing an output of a function defined by the carry-select reuse cells for non-arithmetic chains.

13. The device of claim 10, wherein in the arithmetic mode, a sum is computed using sum lookup tables, values from the sum lookup tables passing through a level of multiplexers and then an additional multiplexer to compute a sum.

14. The device of claim 13, wherein carry computation is performed after allowing lookup table results to pass through an additional level of multiplexing.