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Zhen Zhang
Iowa State University

Yifei Li
Iowa State University

Nathan M. Neihart
Iowa State University, neihart@iastate.edu

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Abstract

In this paper, a comparison between the concurrent multi-band and parallel single-band power amplifier architectures is analyzed. A generalized framework in which these two architectures can be compared in terms of cost, drain efficiency, output power, and linearity is developed. Results show that in general, a concurrent multi-band power amplifier will have worse performance than a parallel single-band amplifier for class-A operation, to the point that it is not a viable substitution. Class-B and class-C operation, however, remain viable alternatives for area savings without a large drop in efficiency and output power.

Keywords

Concurrent power amplifier (PA), Efficiency

Disciplines

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Comments

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Architecture Comparison for Concurrent Multi-Band Linear Power Amplifiers

Zhen Zhang, Yifei Li and Nathan M. Neihart
Dept. of Electrical and Computer Engineering
Iowa State University, Ames, USA
{zhenz, yifei, neihart}@iastate.edu

***Abstract*—In this paper, a comparison between the concurrent multi-band and parallel single-band power amplifier architectures is analyzed. A generalized framework in which these two architectures can be compared in terms of cost, drain efficiency, output power, and linearity is developed. Results show that in general, a concurrent multi-band power amplifier will have worse performance than a parallel single-band amplifier for class-A operation, to the point that it is not a viable substitution. Class-B and class-C operation, however, remain viable alternatives for area savings without a large drop in efficiency and output power.**

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I. INTRODUCTION

As modern wireless communication continues to evolve, users are requiring increased functionality from their wireless devices. Cellular telephones, for example, must support a wide array of different frequency bands and communication standards. It should come as no surprise that there is a heavy burden being placed on the design of the transmitter and specifically, the power amplifier (PA). The PA is typically the primary performance bottleneck in most transmitter designs due to its large size and heavy tradeoff between efficiency and linearity.

Currently, there are two popular approaches for supporting the increasing number of carrier frequencies: 1) use multiple, parallel single-band PAs [1] and 2) use a single PA with a narrow-band response that can be dynamically reconfigured to support different carrier frequencies [2, 3]. Using parallel single-band PAs is the most straightforward, but results in large area and increased component count. The area and component count can be reduced by using a tunable narrow-band PA, but this approach can support only a single carrier frequency at any given time and is therefore unable to support new multi-band communication techniques such as concurrent carrier aggregation that is part of the new LTE-A standard.

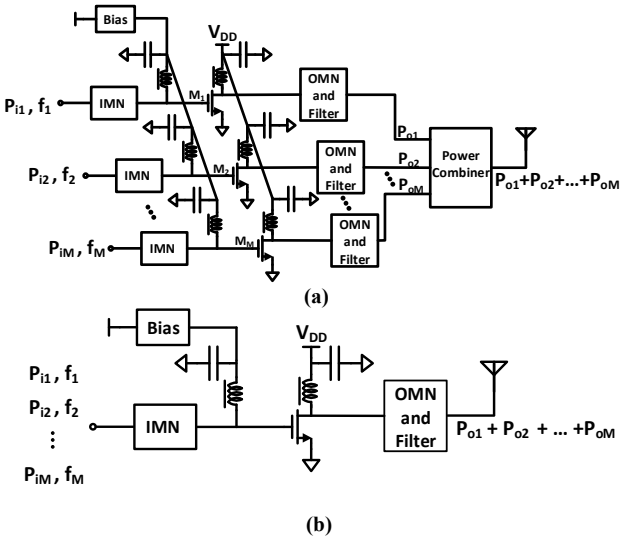

Fig. 1. Schematic showing architectures of (a) parallel single-band power amplifier and (b) concurrent multiband power amplifier.

This has led to a recent interest in the design of concurrent multi-band PA architectures, capable of supporting multiple bands *simultaneously* [4–6]. This approach seems to provide an elegant solution to supporting multiple carrier frequencies, but there is evidence that these systems have a reduced efficiency and output power [6]. At this point, however, performance trade-offs for concurrent multi-band PAs is largely empirical but it is evident that the theory that has been built up around single-band PAs does not accurately predict the performance of concurrent multi-band PAs. Moreover, the performance of concurrent multi-band PAs depends on the number of supported carrier frequencies, their location, and their relative amplitudes.

Given the various performance trade-offs, how is the PA engineer to evaluate the suitability of any one architecture? The focus of this paper is to provide a means for performing a relative comparison between different architectures capable of supporting multiple carrier frequencies simultaneously that is accurate over a wide range of frequency separations, number of supported bands, and modes of operation. This will be accomplished by performing a quantitative comparison between a concurrent multi-band and parallel single-band architectures in terms of cost (i.e., component count), linearity, efficiency, and output power, as well as analyze the causes of these differences.

II. ANALYTICAL PERFORMANCE COMPARISON

This section compares the parallel single-band PA (Fig. 1(a)) to the concurrent multi-band PA (Fig. 1(b)). In order to make a fair comparison, only linear-mode PAs with CMOS transistors (neglecting parasitic capacitances) and lumped-element L-match networks are considered with M carrier frequencies.

A. Component Count and Area

The parallel single-band architecture will be considered first. Each of the parallel PAs will require two components, each, for the input and output matching networks. Therefore an M-band architecture will require $2M$ components for each of the matching networks. Similarly, $2M$ choke inductors and $2M$ bypass capacitors will be required. While it may appear from Fig. 1(a) that these choke/bypass components can be shared, doing so will lead to unacceptable levels of leakage from one

TABLE I. COMPONENT COUNT FOR PARALLEL SINGLE-BAND AND CONCURRENT DUAL-BAND ARCHITECTURE

Component List	Number of Components	
	Parallel Single-band	Concurrent Multi-band
Input L-Match Network	2M	2M
Output L-Match Network	2M	2M
RF Choke Inductor	2M	2
RF Bypass Capacitor	2M	2
Power Combiner	1	0
Power Transistor	M	1
Total	9M+1	4M+5

band to the next due to the reduced isolation between paths. In addition to the M transistors that will be required, the parallel single-band architecture will also require a diplexer to combine all of the signals together for wireless transmission.

The concurrent multi-band architecture, on the other hand requires fewer components. Only a single transistor and therefore only a single set of RF choke/bypass components are required. Moreover, since the component signals are already summed together, no diplexer is required. There is, however, no reduction in the component count of the matching networks. A single-band L-match network can be modified to provide matching at multiple frequencies, simultaneously, by changing it to a bandpass structure [7] and so $2M$ components are still required for each of the input and output matching networks.

The component count for each M-band architecture is summarized in Table I, where it is seen that the parallel single-band architecture requires M times the number of the choke inductors, bypass capacitors, and transistors compared to the concurrent multi-band architecture. This is important because the transistor and the choke inductors will typically dominate the overall area and cost. In addition, the parallel single-band architecture requires a diplexer which can have an area of several cm^2 further increasing the area [8]. Conservatively, the parallel single-band architecture will consume approximately twice the area of the concurrent multi-band architecture.

B. Linearity

A primary difference is the fact that a single nonlinear device must process multiple carrier frequencies, simultaneously, in the concurrent multi-band architecture. The concurrent multi-band architecture will, therefore, suffer from nonlinear distortion in the form of gain compression, which will impact the overall output power, and intermodulation (IM) and harmonic distortion, which will affect the number of potential carrier frequencies that can be supported. Since the parallel single-band architecture only processes a single carrier frequency in each path, it will not suffer from these effects.

These effects will be investigated by modeling the transistor as a large-signal nonlinear transconductor where the drain current is expressed as [9]:

$$I_d(t) = \begin{cases} 0 & V_g(t) \le 0 \\ 3V_g^2(t) - 2V_g^3(t) & 0 < V_g(t) < 1 \\ 1 & V_g(t) \ge 1 \end{cases} \quad (1)$$

where $V_g(t)$ is the input gate-source voltage for the MOSFET and for an M-band input is expressed as:

$$V_g(t) = V_{gDC} + Asin(\omega_1 t) + Asin(\omega_2 t) + \cdots + Asin(\omega_M t) \quad (2)$$

where V_{gDC} is the DC bias voltage and A and ω_M are the amplitude and frequency of each carrier signal, respectively. The normalized transfer function is shown in Fig. 2.

1) Gain Compression Degradation

By expanding (1) using a power series, we can express the amplitude of the M^{th} fundamental as:

$$A_{fund} = A\alpha_1 + \frac{3}{4}A^3\alpha_3 + \frac{3}{2}A^3\alpha_3(M-1), \quad (3)$$

where α_1 and α_3 are the 1st- and 3rd-order coefficients. It is important to note that the overall amplitude of any component will be limited by gain compression imposed by the large amplitude of the other components. In particular, note the presence of the third term in (3) which indicates that the severity of this problem will increase with M. The 1 dB compression point is similarly reduced as can be seen in the following expression:

$$A_{1dB} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \cdot \sqrt{\frac{0.11}{2M-1}}. \quad (4)$$

2) Intermodulation And Harmonics

Perhaps the largest impact of the nonlinear distortion comes in the form of IM and harmonic distortion. Great care must be taken to ensure that there is no overlap between any of the desired carrier frequencies in (2) and the IM and harmonic components generated by the nonlinear distortion of the transistor. This can be facilitated through the use of a Volterra series.

The output of an n^{th}-order nonlinear system with M input frequencies can be express as [10]:

$$y(t) = \frac{1}{2}\sum_{k=1}^{n}\left(\frac{k!}{2^{k-1}m_1!m_2!\cdots m_M!}\prod_{i=1}^{M}(A^{m_i})\,H_k e^{j2\pi f_\Sigma t}\right) \quad (5)$$

where H_k is the Fourier transform of the Volterra kernel of k^{th} order, and m_i is a vector of length n and is populated from the set of numbers $\{0, 1, 2, \cdots, n\}$ such that $\Sigma_M m_i = n$. The term f_Σ represents the frequency location of the nonlinear distortion component and is expressed as:

$$f_\Sigma = \sum_{i=1}^{M}\sum_{k=1}^{m_i} f_i \quad (6)$$

where f_i is a vector of length M and is equal to $f_i = \{\pm f_1, \pm f_2, \cdots, \pm f_M\}$. For example, for $n = 3$ and $M = 2$, one possible realization of m_i is $\{2, 1, 0\}$ and $f_i = \{\pm f_1, \pm f_2\}$ and $f_\Sigma = \pm f_1 \pm f_1 \pm f_2$ resulting in the following locations for nonlinear distortion components: $2f_1 + f_2$, $2f_1 - f_2$, and f_2.

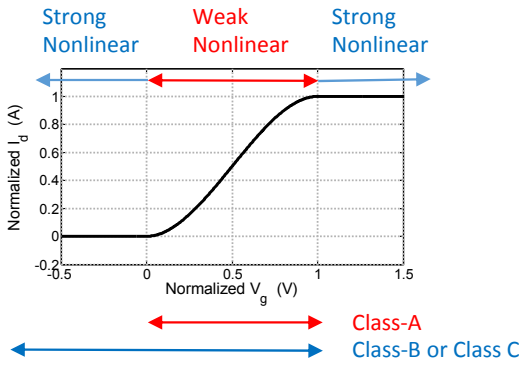

Fig. 2. Transistor transfer function showing both strong and 3rd-order weak nonlinearity.

For completeness, the amplitude of the nonlinear distortion components can also be extracted from (5) as:

$$A_{NL} = \frac{n!}{2^{n-1}m_1!m_2!\cdots m_M!}\frac{1}{A}\prod_{i=1}^{M}(A^{m_i})\frac{H_n}{H_1} \quad (7)$$

where H_n/H_1 can be simplified to the Taylor series coefficients α_n/α_1 of (1) because the system is assumed to be time invariant.

It is important to while (5)–(7) describes both harmonic distortion as well as intermodulation (IM) distortion (in terms of amplitude and frequency location), all possible permutations of the vector m_i must be used in order to obtain a complete list of the nonlinear distortion components. The total number of components, however, can be expressed as:

$$N_{NL} = \frac{(M+n-1)!}{n!(M-1)!}. \quad (8)$$

C. Drain Efficiency

It is easily shown that the parallel single-band architecture follows conventional theory when calculating drain efficiency, i.e., the maximum theoretical efficiency for class-A and B operation is 50% and 78.5%, respectively. The drain efficiency of class-C is dependent on the biasing conditions. Therefore, the following analysis focuses solely on the concurrent multi-band architecture.

Work in [6] analyzed the dependence of the maximum efficiency of a concurrent dual-band ($M = 2$) class-B PA on the relative amplitudes in each band. It was shown that the theoretical efficiency was lowest (~ 62%) when the amplitudes were equal and approached 78.5% when one amplitude was much larger. The analysis in [6], however, did not include the dependence of the efficiency on the relative frequency spacing nor did it consider more than two bands, which is the focus of the following analysis.

1) Concurrent Multi-Band Class-A Operation

When calculating the efficiency, the amplitude of each carrier frequency, A, is set such that the maximum value of $V_g(t)$, V_{gmax}, is normalized to 1 V in all cases. This is equivalent to setting a fixed maximum drain current and scaling the input to achieve maximum output power. Since (2) is a transcendental equation, V_{gmax} cannot be solved for directly. Instead, a Taylor series expansion is used to approximate (2) with a polynomial of the following form:

$$V_g(t) = V_g(k) + \sum_{i=1}^{n}\frac{V_g^{(i)}(k)}{i!}(t-k)^i + R_n \quad (9)$$

where k is an arbitrary constant and R_n is the Lagrange remainder which indicates the overall accuracy of the approximation. Since $V_g(t)$ is periodic, only a single period need be considered and instead of using a single Taylor series approximation to represent the entire period, the value of R_n can be reduced by using multiple expansions, each covering a small portion of a single period. For class-A operation $V_{gDC} = V_{gmax}$ and $I_d(t)$ can be found by substituting (9) into (1).

As previously discussed, the drain current will contain extra frequency components due to nonlinear distortion and these should not be included when computing output power. The load current is therefore calculated assuming that only the fundamental tones are present and that all other frequency components are ideally filtered out. The load current can now be expressed as:

$$I_L(t) = A_{f1}\sin(\omega_1 t) + A_{f2}\sin(\omega_2 t) + \cdots + A_{fM}\sin(\omega_M t) \quad (10)$$

where the amplitudes of the fundamentals, A_f, are obtained from a Fourier series expansion of (1).

Finally, the drain efficiency is:

$$\eta = \frac{P_{RF}}{P_{DC}} = \frac{I_{L,RMS}^2}{I_{DC}\cdot I_{L,max}} \quad (11)$$

where $I_{L,RMS}$ and $I_{L,max}$ are the RMS and maximum value of (10), respectively, and I_{DC} is the average value of the drain current given in (1).

2) Concurrent Multi-Band Class-B Operation

The calculation of the efficiency of a concurrent multi-band class-B architecture is conducted in a manner very similar to the class-A case. The only difference is that the DC gate voltage, V_{gDC}, in (2) is set to 0 V. Note that while V_{gDC} clips at 0 V, $V_g(t)$ is normalized *before* the clipping, so V_{gmax} still equals 1 V. Therefore, (11) can still be used to calculate the drain efficiency, but the load current, $I_L(t)$, must be calculated using the new clipped version of $V_g(t)$.

In fact, this analysis can be easily extended to include class-AB and class-C operation by simply adjusting V_{gDC} to have a value that is either greater than 0 V (class-AB) or less than 0 V (class-C).

III. Simulated Efficiency Results

Fig. 3(a), 3(b), and 3(c) shows the simulated maximum drain efficiency of a concurrent multi-band PA with $M = 3$ (tri-band) for class A, B, and C modes of operation, respectively. The drain efficiency in Fig. 3 is plotted as a function of the carrier frequency ratios f_2/f_1 and f_3/f_1. The dashed green lines indicate the location of either IM components or harmonic components and are therefore unsupported.

It is seen that the efficiency varies as a function of the carrier frequency ratios. The amount of variation is 7.4%, 12.8%, and 10.5% for class-A, class-B, and class-C modes of operation, respectively. This variation is due to the variation in the peak-to-average ratio (PAR) in the drain current that results from summing different carrier frequencies and can be expressed as: $PAR = I_{dmax}/I_{DC}$. This is illustrated more clearly in Fig. 4 which shows two different drain current waveforms: I_{d1} with $f_2/f_1 = 1.4$ and $f_3/f_1 = 2.6$ and I_{d2} with $f_2/f_1 = 1.8$ and $f_3/f_1 = 3.4$. The drain current, I_{d1}, has a $PAR_1 = 5.29$resulting in $\eta_1 = 62.1\%$. The drain current, I_{d2}, has a $PAR_2 = 6.16$ resulting in $\eta_2 = 54.3\%$, a drop of approximately 8%.

It must also be pointed out that the overall efficiency will depend upon the number of supported bands. When the results shown in Fig. 3 are compared to the case when $M = 2$ (dual-band) it is seen that there is a drop in overall efficiency. The efficiency for a concurrent dual-band class-A, B, and C PA is 30.5%–33.8%, 66.2%–73%, and 84.5%–94.6%, respectively. Notice that the maximum drain efficiency for tri-band class-A is approximately 4% below the *minimum* efficiency for a dual-band class-A. Finally, the efficiency of the parallel single-band architecture for class-A, B, and C operation was 50%, 78.3%, and 83%, respectively. Fig. 5 shows the probability of achieving a given efficiency for both concurrent multi-band and parallel single-band architectures each with $M = 2$ and $M = 3$.

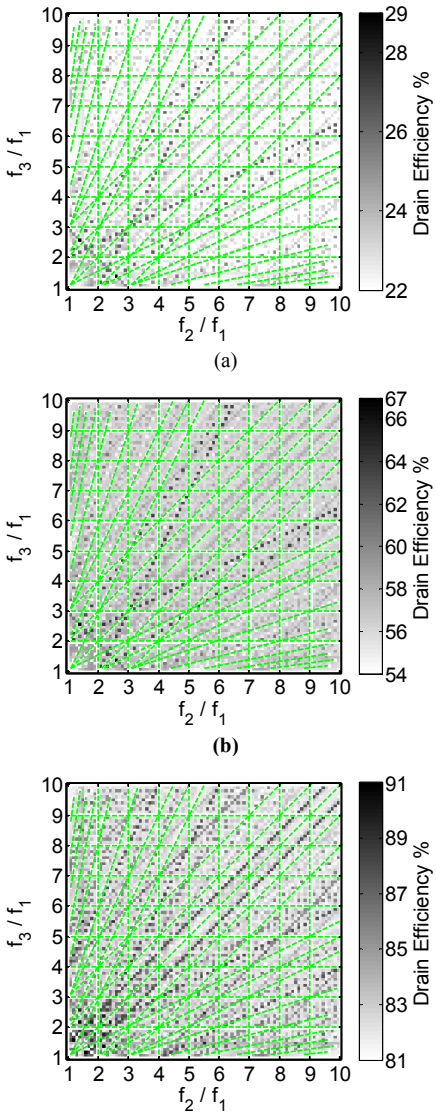

Fig. 3. Simulated drain efficiency versus2-D frequency ratio for (a) class-A, (b) class-B, and (c) class-C

Finally, the output power is investigated. Both architectures have a maximum drain current, I_{max}, which cannot be exceeded. In the parallel single-band architecture, each path can support a signal current with amplitude of I_{max}. In the concurrent multi-band architecture, however, the amplitude of the total summed drain current (obtained from (9) and (1)) must be lower than I_{max} which results in each component having an amplitude of approximately I_{max}/M. The result is that the maximum output power in each band is reduced by a factor of approximately M.

IV. Conclusion

In this paper, two approaches to multi-band PA design have been compared. Interestingly, despite the large interest in concurrent multi-band PA design, if they are to serve as a viable replacement, then emphasis should be placed on class-B or C since the drop in efficiency in class-A too severe. Moreover, this approach will only be suitable for concurrent dual- or tri-band. Beyond three bands, the linearity and output power will be too

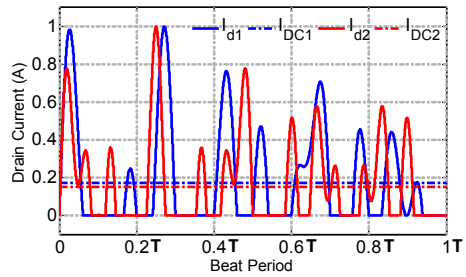

Fig. 4. Class-B drain current and DC current illustrating different PAR. $PAR_1 = 5.29$, $\eta_1 = 62.1\%$, and $PAR_2 = 6.16$, $\eta_2 = 54.3\%$

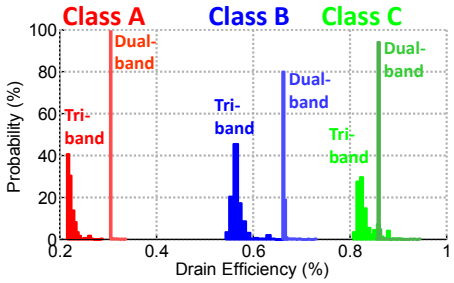

Fig. 5 Probability distribution of drain efficiency for concurrent dual-band and tri-band operation for class-A, B, and C modes of operation

severely limited. In addition, linearity will be a unique challenge in concurrent multi-band architectures and advanced linearization techniques will be more important than ever. This analysis considers only linear operation. Given the trend that seen in Fig. 5, it is expected that concurrent switch-mode PAs will have better relative performance.

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