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Keywords

Power Amplifier, Class-F, Optimum Bias

Disciplines

Electrical and Computer Engineering

Comments

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Time-Domain Analysis of Optimum Bias Point in Inverse Class-F Power Amplifiers

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Abstract—The optimum bias point for an inverse class-F power amplifier is discussed in this paper from a time-domain point of view. It is shown that the inverse class-F power amplifier should be biased in shallow triode region where the bias current is slightly higher than DC current when driven into compression. Lower bias currents can cause significant efficiency degradation due to peaking in the drain-source voltage. Simulation results show that drain efficiency at 6dB over drive drops from 83.4% to 65.2% when bias current is reduced by 34% from optimum bias current. Moreover, it is shown that if the bias current is too high, then the efficiency under power back off is reduced.

Keywords—Power Amplifier; Class-F; Optimum Bias

I. INTRODUCTION

RF power amplifiers (PA) are among the most important components in mobile devices as they consume large amounts of power. A highly efficient power amplifier can largely extend the battery life of a mobile device. High efficiency also relaxes heat dissipation issues, thereby reducing cost.

The class-F power amplifier was introduced in the 1990's [1-3] and has become a popular choice for RFPA designs [4-6]. In ideal class-F operation, the load network presents the desired impedance at the fundamental frequency, an ideal open-circuit at all odd-harmonics of the fundamental, and an ideal short-circuit at all even-harmonics of the fundamental. In this way, the intrinsic drain voltage takes the shape of a square wave while the intrinsic drain current takes the shape of a half-wave rectified sine wave. Because of this, a class-F PA can theoretically achieve 100% drain efficiency. There are limitations to this approach in practice however, and in the early 2000's the inverse class-F (class-F⁻¹) was introduced as a means to increase the realizable drain efficiency [4, 5, 7]. In class-F⁻¹ operation, the load network presents an ideal short-circuit at all odd-harmonics of the fundamental and an ideal open-circuit at all even-harmonics of the fundamental. Such a termination generates a half-wave rectified sinusoidal drain voltage and a square wave drain current.

It has been shown that the drain efficiency of class-F⁻¹ is a function of the transistor's bias. More precisely, drain efficiency is maximized when the PA is biased at high current levels [4, 8]. This observation is primarily empirical, however, and while it has been shown through simulation and measurement results, the theory behind this dependence has never been fully discussed. It proves important, however, to understand this dependence from a theoretical perspective in the face of new developing technologies such as dual-band and multi-band

class-F/F⁻¹ PAs. This paper presents a time-domain analysis of the optimum bias condition for class-F⁻¹.

II. TIME-DOMAIN ANALYSIS OF THE OPTIMUM BIAS POINT FOR CLASS-F⁻¹ PAS

A. Inverse Class-F PA Model

An ideal class-F⁻¹ PA with a generic load network is shown in Fig. 1. The square-wave drain current is achieved by overdriving the transistor [9]. Ideal class-F⁻¹ PAs require significant over-drive in order to for the transistor to behave like an ideal switch, which is not practical in actual PA implementations. In the following analysis, the over-drive level is indicated by the clip angle, α , as shown in Fig. 2. The drain current can now be expressed in terms of α using the following piece-wise linear function:

$$I_{ds}(\theta) = \begin{cases} I_{max}, & \frac{\alpha}{2} > \left| \theta - \frac{\pi}{2} \right| \\ 0, & \frac{\alpha}{2} > \left| \theta - \frac{3\pi}{2} \right| \\ \frac{I_{max}}{2 \cos(\alpha/2)} \cos\left(\theta + \frac{\pi}{2}\right) + \frac{I_{max}}{2}, & otherwise \end{cases} \quad (1)$$

Exploiting the symmetry in the drain current waveform, the conduction angle can be simply expressed as $2\pi - \alpha$. It is worth pointing out that unlike many other classes of operation, the conduction angle in class-F⁻¹ does not determine the bias current. This is because the conduction angle changes with input power whereas the bias current will not. This is illustrated further in the next subsection.

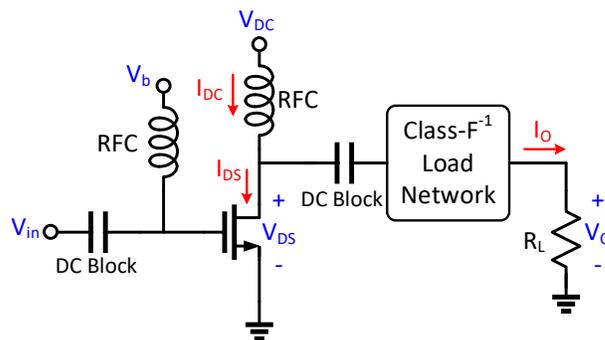


Fig. 1 Schematic of an ideal inverse class-F power amplifier.

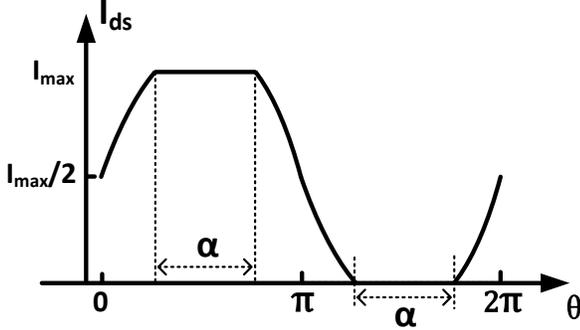


Fig. 2 Drain current waveform of an inverse class-F PA showing the clip-angle α .

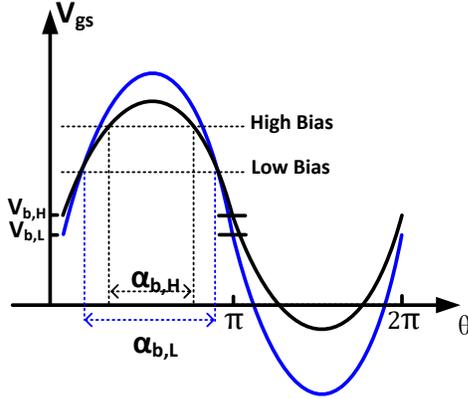


Fig. 3 Input signal waveform for different bias conditions to maintain constant maximum drain current, I_{max}

B. Definition of Drain Bias Current and DC Current

To fully understand the effect of transistor bias on the drain efficiency, a distinction must be made between the transistor bias current, I_b , and the DC supply current, I_{DC} . This distinction is a direct result of the non-linear behavior of the overdriven transistor. The bias current, I_b , is determined by the DC bias voltage applied to the gate, V_b , when $V_{ds} \geq V_b - V_{th}$:

$$I_b = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_b - V_{th})^2 \cdot (1 + \lambda(V_b - V_{th})) \quad (2)$$

The DC current, on the other hand, is equal to the time-average value of the drain current, and in the case when the drain current is a square-wave, $I_{DC} = I_{max}/2$. The conditions for which $I_b \neq I_{max}/2$ will be discussed in the next subsection.

The value of I_{max} is set by the supply voltage and the desired RF output power. Assuming a drain voltage is an ideal half-wave rectified sine wave, then for a given RF output power, P_{out} , and DC supply voltage, V_{DC} , the maximum drain current can be expressed as:

$$I_{max} = \frac{4P_{out}}{\pi V_{DC}} \cdot f(\theta) \quad (3)$$

where

$$f(\theta) = \frac{\pi}{2} \left(\frac{4 \cos(\alpha/2)}{2 \sin(\alpha/2) \cos(\alpha/2) + \pi - \alpha} \right). \quad (4)$$

Finally, using (3) and (4) the required load resistance can be calculated as:

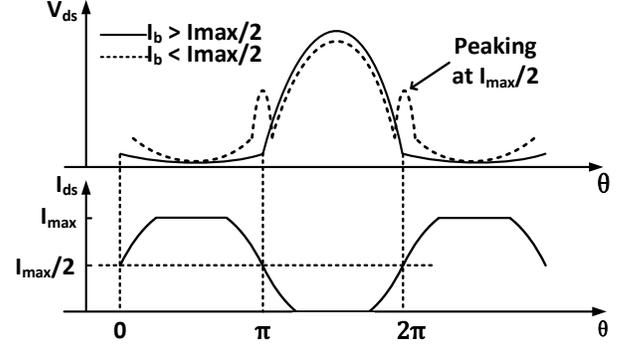


Fig. 4 Drain voltage and current waveforms for different bias conditions. Unwanted peaking occurs at $\theta = \pi$ when $I_b < I_{max}/2$.

$$R_L = 2P_{out}/I_L^2 = (V_{DC}\pi)^2/(8P_{out}) \quad (5)$$

where $I_L = I_{max}/f(\theta)$ is the amplitude of the sinusoidal current flowing through the load (i.e., the fundamental component of I_{max}).

To simplify the upcoming analysis and facilitate a discussion of amplifiers with different bias conditions, I_{max} and R_L will be kept constant for all bias conditions. The supply voltage and corresponding output power will then change accordingly. Moreover, as the bias point changes, the clip angle, α , and hence the required input power, will also change because lower bias points require increased input power in order to maintain a constant value for I_{max} [4]. This is illustrated in Fig. 3, where $V_{b,H}$ and $V_{b,L}$ are two different bias voltages leading to the same I_{max} .

C. Optimum Bias Condition for Inverse Class-F PA

To see how the bias current will affect the drain efficiency in class-F¹ PAs, it is important to examine the drain current waveform for different gate overdrive levels. Referring to Fig. 1, when the transistor is not driven past its compression point, the transistor will be operating in the linear region and the drain current, I_{ds} , will be a sinusoidal signal centered around the bias current, I_b . In this case, the time-average value of the drain current will be equal to the bias current, I_b , but drain efficiency is low due to heavy overlap between non-zero drain voltage and drain current.

As input power increases, however, and the transistor is driven further into saturation, the drain current begins to clip and take on a square-wave shape, as shown in Fig. 2. In this case, the time-average value of the drain current will approach $I_{max}/2$. The problem comes when the instantaneous input voltage is equal to V_b (e.g., when $\theta = \pi$). At this instant in time, the drain bias inductor forces a constant current of $I_{max}/2$ to flow through the transistor, but, in general, $I_b \neq I_{max}/2$. This conflict is resolved by a change in the drain voltage that is dependent on the bias current.

In general, for the half-cycle of $0 < \theta < \pi$, the transistor remains in the triode region and the drain voltage is near zero. We now consider what happens at the instant in time when $\theta = \pi$ for two different bias conditions. For the case when $I_b > I_{max}/2$, at $\theta = \pi$ the transistor tries to sink more current than

the drain bias inductor can supply. Therefore, the drain voltage decreases in order to push the transistor further into the triode region. The total drain voltage waveform for this bias condition is shown as the solid line in Fig. 4. This is the desired shape for class-F⁻¹ PAs as it results in the minimum overlap between non-zero drain voltage and non-zero drain current. We term this bias condition as ‘biased in triode’ because $V_{ds} < V_{in} - V_{th}$ when $\theta = \pi$.

Alternatively, when $I_b < I_{max}/2$, when $\theta = \pi$, the drain bias inductor forces the transistor to conduct a larger drain current than set by V_b . The result is that the drain voltage must increase, pushing the transistor into the saturation region in order to satisfy Kirchhoff’s current law. The drain voltage for this bias condition is shown as the dashed line in Fig. 4. As the bias current is further reduced, the magnitude of the peaking in the drain voltage increases. The peaking in the drain voltage increases the overlap between the non-zero drain voltage and drain current thereby increasing the power dissipated in the transistor. Moreover, the peaking in the drain voltage causes a reduction in the amplitude of the load voltage leading to a reduced output power. These two effects result in a significant reduction in drain efficiency. We term this bias condition as ‘biased in saturation’ because $V_{ds} > V_{in} - V_{th}$ when $\theta = \pi$.

The above discussion indicates that a class-F⁻¹ PA should be biased with $I_b > I_{max}/2$. Further increasing the bias current does not result in significantly improved drain efficiency. In fact, if the bias current is too high the efficiency under power back-off will be degraded. This bias point is independent of frequency. We now validate this analysis using simulation.

III. SIMULATION RESULTS

The optimum bias condition, discussed in Section II, is verified through simulation of the class-F⁻¹ PA shown in Fig. 1. It is assumed that the load network presents 25 Ω to the transistors at the fundamental frequency and an ideal open- and short-circuit at all even- and odd-order harmonics, respectively. For each bias point under consideration, the supply voltage, V_{DC} , is adjusted to maintain a constant $I_{max} = 1 A$ and hence, $I_{DC} = 0.5 A$.

Transient simulations of the amplifier shown in Fig. 1 were performed under two different bias conditions, $I_{bL} = 0.35 A$ and $I_{bH} = 0.53 A$, when $V_{ds} = V_b - V_{th}$. Since $I_{DC} = 0.5 A$, we see that the first case is biased in saturation while the latter is biased in triode. In both cases, the input power is adjusted such that the PA is at 6 dB overdrive. The simulated drain current and drain voltage are shown in Fig. 5 and Fig. 6, respectively. In order to maintain a constant value for I_{max} , the DC supply voltage was set at 14 V for $I_b = 0.35 A$ and 10.5 V for $I_b = 0.53 A$. Notice, however, that the amplitude of the drain voltages in Fig. 6 are approximately equal. This is due to the constant I_{max} and R_L and results in approximately equal output power for each bias condition.

As expected, a larger clip angle, α , is seen in Fig. 5 for the smaller bias condition. As seen in Fig. 6, for $I_b > I_{DC}$, the drain voltage has the desired half-wave rectified sinusoidal shape, resulting in minimum overlap between the non-zero drain voltage and drain current. When the bias current is decreased,

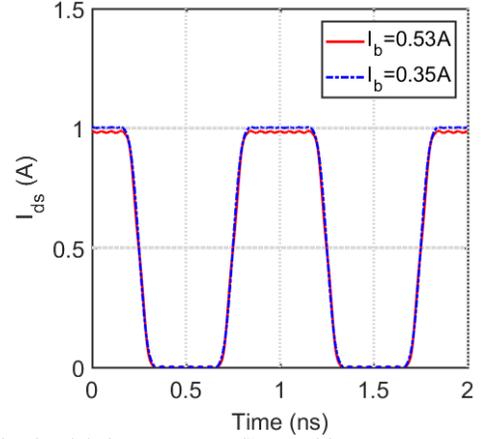


Fig. 5 Simulated drain current at 6 dB over drive

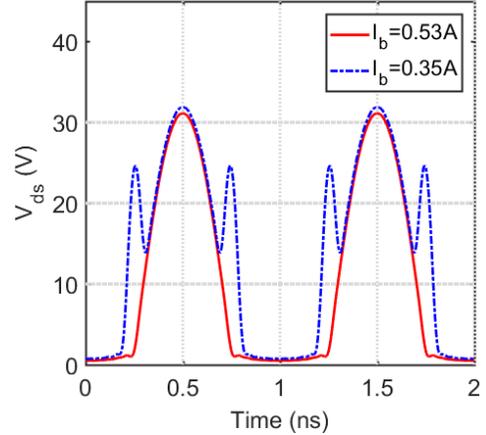


Fig. 6 Simulated drain voltage at 6 dB over drive

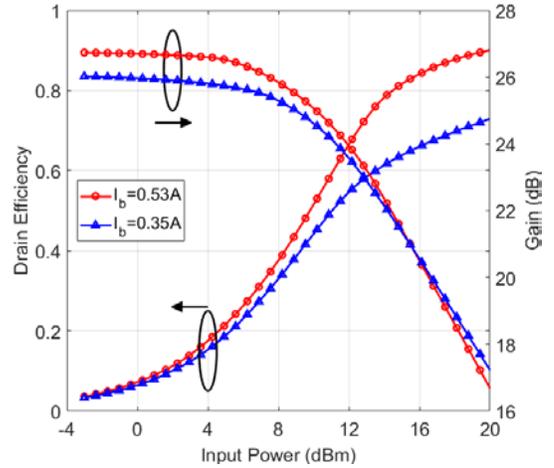


Fig. 7 Drain efficiency and power gain under $I_b = 0.35 A$ and $I_b = 0.53 A$

however, there is significant peaking in the drain voltage in order for the transistor to carry the 0.5 A when the instantaneous AC input voltage is zero. This peaking results in an increase in the power dissipation in the transistor. Because the output powers are the same for the two bias conditions, there will be a significant reduction in drain efficiency for the case when $I_b = 0.35 A$.

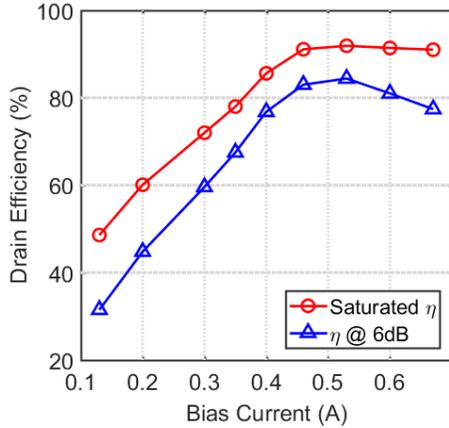


Fig. 8 Peak drain efficiency and drain efficiency under 6 dB over drive as a function of bias current.

To illustrate the level of degradation in drain efficiency due to non-optimal biasing, the simulated drain efficiency and power gain for the two bias conditions are shown in Fig. 7. At 6 dB overdrive, when $I_b = 0.35$ A, the drain efficiency is 67% with an output power of 36.8 dBm, and a power gain of 20 dB. When $I_b = 0.53$ A, however, the drain efficiency is 84% with an output power of 36.5 dBm, and a power gain of 20.7 dB. To explore this dependence further, Fig. 8 plots the saturated drain efficiency and the drain efficiency at 6 dB overdrive for various bias conditions.

It can be seen that the saturated drain efficiency starts to flatten out at $I_b = 0.4$ A while the drain efficiency at 6 dB over drive begins to saturate at $I_b = 0.46$ A and peaks at $I_b = 0.53$ A. Further increases in the bias current actually degrades the drain efficiency at 6 dB over drive. This is because, as discussed in Section II, when I_b is too large, the drain efficiency drops faster as power backs off. Fig. 8 shows similar saturated drain efficiency (red curve) beyond $I_b = 0.53$ A, however, as power backs off to 6 dB over drive (blue curve), drain efficiency drops more for higher bias currents, resulting in lower efficiency. This is also illustrated in Fig. 9, where the drain efficiency and power gain are plotted for $I_b = 0.53$ A and $I_b = 0.67$ A. It can be seen that, at $I_b = 0.67$ A, the drain efficiency drops faster as the input power is reduced. In addition, the power gain also decreases faster for increasing input power. So while the amplifier should be biased with a current large enough to avoid peaking in the drain voltage, the bias current should not be too high. The optimal bias condition of a class-F⁻¹ PA is to bias it in shallow triode region, in other words, the bias current should be slightly larger than $I_{max}/2$ of the transistor.

IV. CONCLUSION

The optimum bias condition for a class-F⁻¹ power amplifier is discussed from a time-domain perspective. It is found that the bias current should be slightly larger than the DC supply current in order to maximize drain efficiency. As the bias current is reduced below the DC supply current, peaking in the drain voltage leads to significant reductions in drain efficiency. Conversely, if the bias current is too high with respect to the DC

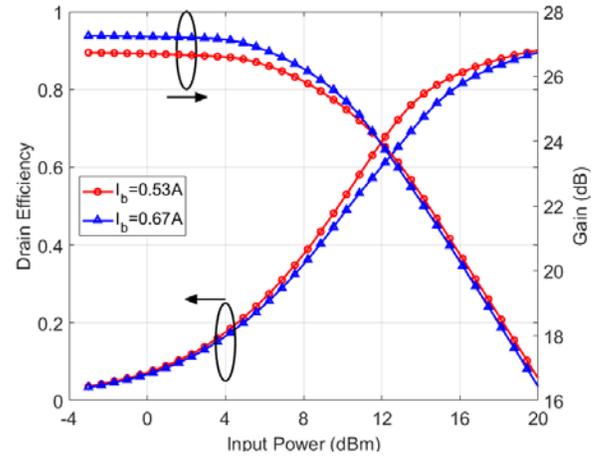


Fig. 9 Simulated drain efficiency and power gain under $I_b = 0.53$ A and $I_b = 0.67$ A

supply current, then the drain efficiency at power back off is degraded. These results were verified through simulation results.

ACKNOWLEDGMENT

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