New Memory Technologies

Nishtha Bhatnagar
Iowa State University

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New Memory Technologies

By

Nishtha Bhatnagar

A creative component report submitted to the graduate faculty in partial fulfillment of the requirements for the degree of MASTER OF SCIENCE

Major: Electrical Engineering

Program of Study Committee:
Prof. Vikram Dalal, Major Professor
Prof. Long Que, Co-Major Professor

Iowa State University
Ames, Iowa
2018
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- My thanks to Prof. Long Que who provided me feedback and gave me valuable suggestions. I was first introduced to data during my summer work in Dr Que’s lab where I was working on Brain Cells where I had to keep a track of number of regenerating bran cells. This acquired knowledge helped me to solve problems at industrial level
- Big thanks to Micron Technology for providing me this great opportunity that helped me to grow as a person. I was exposed to an industrial environment where I worked upon my weaknesses and strengthened the abilities I already possessed
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- Team Members at Micron for their guidance and support
- My family and friends for being my inspiration and constantly supporting and encouraging me
Abstract

Memory is used to store the data. Semiconductor memory can be used as our computer’s cache memory, in our mobile applications, in memory cards of our cameras. To meet the growing needs for memory, variety of different memories are used like DRAM, SRAM, etc. With the rapid growth in the requirement of memories new memory technologies are being developed and considerable amount of research is invested in these new memory technologies. One of a very new memory technology is 3DXP Memory. 3DXP is a type of Non-Volatile memory which has very high density and high speed as compared to any other Non-Volatile memory. It can be used in various applications like Genomics, sensing. In this report, I would like to introduce 3DXP Memory development and my work as a 3DXP Yield Enhancement Electrical Failure Analysis Engineer. In my creative component I was required to read and understand the literature about how different memories work. I was also assigned to do an internship on 3DXP Memory at Micron Technology Inc from March 12, 2018 through August 3, 2018. During my master’s degree I took some courses like Semiconductor Physics, Microelectronics Fabrication Techniques, Digital VLSI and Statistics which helped me to learn and apply the knowledge to solve problems at industrial level.
Chapter 1. Introduction

**Memory**
Memory is a Physical device which stores data on permanent or temporary basis. It is just like a human brain which stores all the information. From the clicked pictures in our cameras to the text messages in a mobile phone, memory is needed everywhere. It contains a circuit that stores large array of digital information.

Memory can be classified into below categories:

![Memory Classification](image)

**Volatile Memory**
This type of memory requires power to retain the data. It loses its content as soon as power is turned off.
*Examples:* SRAM memory, DRAM memory
*Usage:* It is used in computer’s main memory

**Non-Volatile Memory:**
This memory stores the information even if the power is turned off. It can permanently store the information.
*Examples:* NAND Flash, NOR Flash, 3DXP Memory
*Usage:* It is used in Laptops, Tablets, MP3 player, phones

The semiconductor industry is growing at a very fast rate and the demands of the customers are also increasing day by day. So, to satisfy their requirements researchers are innovating new memory technologies. One such technology is 3DXP Memory which is fastest the Non-Volatile memory till date.
Chapter 2. Background Information

Overview of Different types of Memory

2.1 SRAM (Static Random-Access Memory)

SRAM Memory[4] is a class of Volatile Memory which has very fast Read and Write operations. It is widely used in Cache Memory.

Construction

![SRAM Memory Cell]

Figure 2. 1 SRAM Memory Cell

It consists of two cross coupled inverters i.e. four transistors to store each bit of data. Also, there are two access transistors (here M5 and M6) which are used to control the access to the storage cell during Read and Write operations. As it contains 6 transistors to store a bit, its structure is complex, and it consumes more power.

Working

![Cross-coupled inverters]

Figure 2. 2 Cross-coupled inverters

Retaining:
Cross coupled inverters act like a feedback loop and help in retaining the data.

Writing:
We have to give a high voltage on the WL, so that the MOSFET switches close and provide access to the memory cell. BL and BL_Bar will act like an input.

Example: If we want to store logic 1 inside the memory cell, we will give input at BL as logic 1 (high voltage) and BL_Bar as logic 0 (ground) so that both the bit-lines force the logic values into the memory cell.
Reading:
The bit-line is pre-charged to Vdd/2 and WL is at a high voltage. If the memory cell has logic 0 stored in it, the BL will go low and BL_Bar will go high. Hence, the difference would be negative which would be sensed by a sense amplifier. If Logic 1 is stored, then BL will go high and BL_Bar will go low. Hence, the difference would be positive.

<table>
<thead>
<tr>
<th>Memory cell</th>
<th>BL</th>
<th>BL_bar</th>
<th>Difference</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Low</td>
<td>High</td>
<td>Negative</td>
</tr>
<tr>
<td>1</td>
<td>High</td>
<td>Low</td>
<td>Positive</td>
</tr>
</tbody>
</table>

Table 2. 1 Read Operation

2.2 DRAM Memory (Dynamic Random-Access Memory)

DRAM Memory[7] is also a Volatile Memory and is cheaper than SRAM. It is used in computer’s Main Memory, PDAs, game machines, digital audio devices, et cetera.

Construction

Each memory cell has a capacitor and an access transistor. Data is stored in DRAM as charge on a capacitor. Capacitor is either charged to full Vdd level (Logic 1) or ground (Logic 0).[3] This memory requires refresh due to charge leakage through the capacitor every time a read operation is performed. Since, we need to recharge the capacitor again and again in order to restore the data, it is called as “Dynamic RAM”. Its structure is less complex than SRAM because only one access transistor and one capacitor is used.
Working

Writing:
WL remains high to close transistor switch. If we want to write Logic 1, we will give high voltage to BL. If we want to write Logic 0, then we will connect BL to ground.

Reading:
We can read what’s stored in DRAM Memory by turning the access transistor ON and this output goes into the BL which will further go into the sense amplifier. If the sensed voltage is more than the reference value (Vdd/2) then it is as considered Logic 1 else, it is Logic 0.

2.3 Flash Memory

Flash Memory is a Non-Volatile memory which has very high density. It is used in SSDs, Memory sticks, cameras. It uses the concept of floating gate MOSFETs.

Construction

![Figure 2. 5 Floating Gate MOSFET](image)

It uses floating gate MOSFET[8] to store data. It consists of two gates, 1) a floating gate which is electrically isolated and not connected to any metal contacts, 2) a control gate which is connected to the gate terminal.

The two gates are separated by a thick oxide layer called as an Inter-Poly Dielectric or a Blocking Oxide and the other oxide layer is called as a Tunnel Oxide.

Working

Reading:

![Figure 2. 6 Floating Gate Charge States in Logic 0 and 1](image)
Value 0 will have higher threshold voltage than value 1 due to accumulation of negative charges on the floating gate.
We will give a voltage between threshold voltage of logic 0 and threshold voltage of logic 1 and will measure the current. If there is no current, then it’s a logic 0 else a Logic 1.

**Programming:**

NAND Memory uses Quantum Tunneling [5] mechanism for programming. When high negative voltage is applied on the control gate the barrier shape changes. The electrons in the channel see a triangular barrier which is easy to pass than rectangular barrier. The electrons move from channel into the floating gate.

NOR Memory on the other hand uses hot electron injection effect [5] for programming the memory cell. When some gate to source voltage is applied a channel is created. When we apply source to drain voltage some electrons start accelerating and hence, the kinetic energy of these electrons increases. When electrons gain sufficient energy which is greater than the oxide barrier, these electrons start jumping over the oxide barrier and end up in the floating gate.
Erasing:

![Erase Operation Diagram](image)

**Figure 2.10 Erase Operation**

Erase operation in both NAND and NOR can be done by Quantum Tunneling mechanism. When high positive voltage is applied to the control gate, the electrons in the floating gate cross the barrier goes and go into the p substrate.

**NOR Flash Structure:**

![NOR Flash Structure Diagram](image)

**Figure 2.11 NOR Flash**

**Read**

We will apply an intermediate voltage (between threshold of Logic 1 and 0) to the cell we want to read and low voltages to all other floating gate MOSFETs to make sure they do not conduct.

**Program (Logic 0):** High voltage is given to the drain and a gate voltage greater than threshold voltage to the memory cell we want to program.

**Erase (Logic 1):** High negative gate voltage is applied, and value of all floating gate cells are set to 1 by quantum tunneling mechanism.

**NAND Flash Structure:**

![NAND Flash Structure Diagram](image)

**Figure 2.12 NAND Flash**

**Read**

We will apply an intermediate voltage (between threshold of Logic 1 and 0) to the cells we want to read and high voltages to all other floating gate MOSFETs, so that they are conducting. We also have to turn on the Bit Line Select and Ground Select transistors.
Program (0): High positive gate voltage is applied to the memory cell we want to program in order to program it through quantum tunneling.

Erase (1): High negative gate voltage is applied, and value of all floating gate cells are set to 1 by quantum tunneling mechanism.

### 2.4 3DXP Memory

![Figure 2. 13 Memory Trend](image)

New revolutionary Non-Volatile memory after 36 years with improved performance. It was announced in 2015 and is a joint venture of Intel and Micron. The production is in Lehi, Utah.

It's a faster, transistor-less, stackable and inexpensive memory. It is not limited by number of programs cycles hence, has high endurance. It also has high density and low latency as compared to NAND. [3]

It can be used in variety of applications such as Gaming, Pattern recognition and Genomics.

**3DXP Architecture**

![Figure 2. 14 3DXP Memory Architecture](image)

This memory uses cross-point array architecture, perpendicular BL and WL connect submicroscopic columns.

It consists of memory cell which stores single bit data and a selector which enables memory cell to be written or read without using a transistor.

Thin layers of memory can be stacked to boost density.
Working

Each memory cell can be individually addressed by selecting its top and bottom line, i.e. BL and WL. [2]
It uses phase change material with different resistances for storing data. Amorphous state to store logic 0 and crystalline state to store logic 1. Selector device is used to access the device.
It consumes very less power than NAND and has more write/read speeds than any non-volatile memory.

Summary

<table>
<thead>
<tr>
<th></th>
<th>SRAM</th>
<th>DRAM</th>
<th>NAND</th>
<th>NOR</th>
<th>3DXP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data stored</td>
<td>As state of digital</td>
<td>As charge on capacitor</td>
<td>By trapping charge on a floating gate</td>
<td>By trapping charge on a floating gate</td>
<td>By changing resistance of the material</td>
</tr>
<tr>
<td>Refresh</td>
<td>Not required</td>
<td>Required</td>
<td>Required after 10 years</td>
<td>Required after 10 years</td>
<td>Required after 10 years</td>
</tr>
<tr>
<td>Type</td>
<td>Volatile</td>
<td>Volatile</td>
<td>Non Volatile</td>
<td>Non Volatile</td>
<td>Non Volatile</td>
</tr>
<tr>
<td>Read and Write</td>
<td>Very fast</td>
<td>Fast</td>
<td>Slow Read, Very slow Write</td>
<td>Faster than NAND</td>
<td>Faster Read and Write than NAND</td>
</tr>
<tr>
<td>Density</td>
<td>Low</td>
<td>High</td>
<td>Very High</td>
<td>Medium</td>
<td>Very High</td>
</tr>
<tr>
<td>Applications</td>
<td>Cache memory</td>
<td>Main memory</td>
<td>Digital cameras, memory sticks</td>
<td>SSDs, Memory sticks</td>
<td>Mobile applications, Gaming</td>
</tr>
</tbody>
</table>

Table 2. 2 Summary
Chapter 3. Work as 3DXP Engineer

Work on 3DXP Memory

Worked as Yield Enhancement Electrical Failure Analysis Engineer. Interacted with Process Integration, process, probe and product engineers. Analyzed probe, parametric and fab data to identify yield issues. Published and presented reports on analysis in meetings. Applied knowledge of silicon fabrication steps to identify and troubleshoot yield issues. [2]

![Micron Internship Timeline](image)

Figure 3. 1 *Micron Internship Timeline*

Responsibilities included to identify interactions between process modules and equipment to detect fail mechanisms. I was also responsible to monitor the end of line performance to identify unexpected shift.

Micron is a world leader in memory technology solutions. It manufactures DRAM, NAND, NOR, 3DXP, SSDs. It was founded in 1978 and CEO is Sanjay Mehrotra.
Chapter 4: Projects and Discussion on 3DXP Memory

4.1 3DXP Training

Project Goal:
Project aim was to gain basic understanding of 3DXP-20 series working and 3DXP architecture and to complete online trainings on SPC, Statistics, JMP and Yield3 training. Introduction to YE Tools like Unix, Putty, Micron central, Data Daemon.

Outcomes:
After undergoing some trainings, I was able to extract probe data from Yield3 and I analyzed data using JMP. I performed probe to inline correlation and simple data mining like good vs bad analysis. I also supported few SWRs which helped in applying data extraction techniques, preparation and process knowledge and used them to make analysis.

4.2 Special Work Request (SWR) Analysis

Project Goals:
Goal for this project was to complete SWR Analysis using YE tools by deadline. Also, had to interact with respective process owners and learn, understand the particular process like Lithography, Etching. Aim was to present conclusive solutions in the weekly meetings.

Outcomes:

![Figure 4.1 Number of dies failing in a wafer seen in ESDA software](image)

Green: Good Dies
Orange: Bad Dies

I got exposed to interact with SWR owner and PI Engineer from both R&D and manufacturing fabs. I was given opportunity to focus on small portion of the process flow and analyze how changes in particular process can affect electrical metric. I used ESDA (Enhanced software for data analysis) to map the failing bins in a wafer. Example- Worldline fails due to short circuits identified by particular pattern on map. I also presented analysis and gave recommendations to the process owners.

Process:

A new SWR Request came with a recipe change from the process owner, it included one control group set of wafers on which old process was used and few experimental
group wafers where new process was introduced. I had to extract the process data from Yield3 and analyze the data in JMP. I had to check for any toggles in comparison with other control group wafers. Final step was to electrically analyze the data and find the causes about the failing dies. Main goal was to find the size and shape of the defect, density of defect, defect location and causes of defect.

**Figure 4. 2 Underexposure causing shorts**

*Example:* Word-line-Word-line shorts caused due to under exposure during Lithography.

**Figure 4. 3 Underexposure led to WL-WL shorts which led to selecting two memory cells**

### 4.3 Weekly Trend Analysis

**Project Goals:**
To Perform probe trend analysis and highlight shift needs to be followed up and to present outcomes in weekly group meetings.

**Outcomes:**
In this project I worked on weekly tracking of defined set of critical yield metric and flagged unexpected trend seen like more fails due to new reticle mask change, I also checked for potential shift cause and performed correlations. I was exposed to JMP Scripting Language and I also automated Weekly trends analysis. I was also able to highlight fails and worked on follow up items.

**Process:**
I had to extract all lots fabrication data of that week and I wrote a script for weekly trends that selected and sorted the most important metrics which had the greatest number of fails out of 600-1000 metrics. The script could tell about the causes of fail
and the trend’s direction. I could focus more on the top metrics rather than visually seeing all 600 metrics.
Example:

Figure 4.4 Reticle mask change led to higher fails
Chapter 5. Conclusion

The main aim was to do a literature survey on all existing memories and to work on 3DXP Memory at Micron Technology. After reviewing the literature and working as 3DXP YE Engineer I can say 3DXP is a very promising Non Volatile memory which is 1000X times faster than NAND Memory [2]. It also has 10X more density than DRAM. It has low cost and low latency in nanoseconds as compared to NAND which is in microseconds. The lifetime is also not impacted by number of write cycles. 10 series has dual decks and 20 series have quad decks with higher densities. During my internship I was able to produce yield reports to increase yield and find the causes of the fails. I was also able to automate Weekly Trends so that just by a click engineers could see which electric metrics are failing for the particular week and their respective causes. This helped in making the weekly trends analysis more effective.
References