Calculation of defect densities in nano-crystalline and amorphous silicon devices using differential capacitance measurements

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Calculation of defect densities in nano-crystalline and amorphous silicon devices using differential capacitance measurements

by

Daniel Norbert Congreve

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in partial fulfillment of the requirements for the degree of

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Major: Electrical Engineering

Program of Study Committee:
Vikram L. Dalal, Major Professor
    Rana Biswas
    Mani Mina

Iowa State University
Ames, Iowa
2011

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Abstract

A technique for determining trap densities as a function of energy in semiconductors is presented. Through differential capacitance measurements, trap states can be accurately measured and profiled within the bandgap as a function of energy.

Measurements were carried out on samples made at the Microelectronic Research Center at Iowa State University. Hydrogen profiled nano-crystalline silicon samples and amorphous samples were made in a VHF-PECVD reactor. ITO was deposited using RF sputtering to serve as the top contact.

Defects for amorphous silicon were shown to be Gaussian approximately .7 eV below the conduction band, on the order of $10^{15} - 10^{16}$ cm$^{-3}$ depending on deposition. This agrees with both external a-Si measurements and C-V defect measurements.

Defects in nano-crystalline silicon were studied as a function of oxygen present in the material. Five different depositions were carried out with varying amounts of oxygen (0, 9, 18, 27, and 36 sccm). The defect densities of each device were then measured. A large increase in defect densities corresponding to an increase in oxygen content is shown. Thus it is critical to minimize oxygen contamination during device fabrication.

This measurement technique is detailed for the first time on amorphous and nano-crystalline silicon. Through extensive de-noising procedure it produces results with greater accuracy than previous attempts. It provides an excellent non-destructive look at the defect profile of a solar cell and can easily be applied to other photovoltaic materials such as organics.
1. Introduction

1.1 Our Energy Future

World energy demands are skyrocketing. By 2050, it is estimated that electrical energy demand will pass 30 terawatts, over 3 times the energy we currently use. Our current energy profile cannot meet the needs of our growing world while keeping CO$_2$ emissions in check. Oil is starting running out and its price Keeps increasing. Worse, the United States is operating at a severe oil trade imbalance, consuming 21.7% of the world's oil despite producing only 8.5% of it [2]. This creates both economic and national security issues.

Figure 1-1. The worldwide oil trade balance is shown. Note that much of the imports to the United State comes from politically unstable areas (Venezuela, Middle East, Libya, etc). This puts enormous geopolitical stress on the government. The development of domestic energy would be a huge coup both politically and economically. [2]
Nuclear, haunted by the memories of Three Mile Island and Chernobyl, fails to garner any public support. Our nuclear infrastructure is aging, with every American plant at least 27 years old and ground broken on only two new plants [3]. Wind has shown excellent potential to ease demand, yet it is currently propped up by federal credits set to expire in 2012 [4]. If they expire, the cost per megawatt-hour will approximately double as compared to plants installed before the expiration [4]. This leaves the uncertain future of wind at the hands of an increasingly cost-conscious government. Other green technologies – tidal, geothermal, etc. – can make contributions to our energy needs, but each has problems of its own and none can approach the large quantity of energy needed. It appears that solar will play one of the largest parts in our future energy portfolio. With over 120,000 terawatts of sunlight falling on the earth, capturing but a sliver of that energy would significantly ease energy demand and reduce our carbon footprint. Solar does suffer from several drawbacks, the most prominent being cost and efficiency. Intelligent research, however, can reduce the cost of solar cells and boost their efficiencies, allowing them to be cost effective with traditional power sources.

<table>
<thead>
<tr>
<th>Program</th>
<th>Expiration Deadlines for Wind Projects</th>
</tr>
</thead>
<tbody>
<tr>
<td>Section 1603 Cash Grant</td>
<td>Begin construction by 12/31/11, place in service by 12/31/12</td>
</tr>
<tr>
<td>DOE Section 1705 Loan Guarantee</td>
<td>Begin construction by 9/30/11</td>
</tr>
<tr>
<td>Bonus Depreciation Schedule</td>
<td>Place in service by 12/31/11 for 100% first-year bonus depreciation, 12/31/11 for 50% bonus</td>
</tr>
<tr>
<td>Production Tax Credit and Investment Tax Credit</td>
<td>Place in service by 12/31/12</td>
</tr>
</tbody>
</table>

Figure 1-2. The projected cost for wind for different tax breaks scenarios are shown at left and the current wind tax breaks are shown at right. Case 1 utilizes just the Production Tax Credit (PTC) available in 2008 and private equity. Case 2 utilizes all four wind programs. Case 3 uses private equity assuming the PTC is renewed, and Case 4 uses private equity assuming the PTC is not renewed. Clearly the tax credits are a crucial part of the success of wind power. [4]
1.2 The Solar Industry

Solar power can be separated into two groups: concentrating solar power (CSP) in which concentrated sunlight heats water which drives turbines, and photovoltaics (PV) in which semiconductor materials directly convert photons to electricity. Solar, particularly photovoltaics, has exploded in recent years despite its high cost as compared to non-renewable resources. The United States, despite some of the best solar real estate in the world, ranks fourth in PV installation, trailing Germany, Spain, and Japan [5]. These three countries have much more aggressive solar policies, helping their industry.

The solar industry is actually quite diverse, consisting of a wide range of materials. These can be grouped into various categories, each
with their own positives and negatives as shown in Table 1-1. The best research efficiencies of various technologies to date are shown in Figure 1-6. III-V devices (purple) dominate the efficiency scales, reaching as high as 42.4%, but these devices are extremely costly to build and have no real use in terrestrial applications. Crystalline silicon (blue) is by far the dominant technology. It combines excellent electrical properties with mature processing technology. It has poor light absorption, however, requiring large amounts of fairly expensive material to be competitive. It is nearing the limit of its efficiencies. Thin films (green) offer great material savings but still require fairly expensive processing. Organics offer extremely cheap processing yet are quite inefficient and degrade rapidly.

Figure 1-6. The photovoltaic conversion efficiencies over the last 35 years are shown. Though traditional crystalline silicon (blue) and multijunction III-V cells (purple) dominate the absolute efficiency, their high cost gives advantages to the thin film (green) and organic (orange) technologies. [7]
<table>
<thead>
<tr>
<th>Material</th>
<th>Positives</th>
<th>Negatives</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>III-V Junctions</td>
<td>• Extremely high efficiencies</td>
<td>• Extremely costly to produce</td>
<td>• Holds record efficiency</td>
</tr>
<tr>
<td></td>
<td>• Very lightweight</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Mature processing technology</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Crystalline Silicon</td>
<td>• High efficiencies</td>
<td>• Costly processing</td>
<td>• Dominant terrestrial technology</td>
</tr>
<tr>
<td></td>
<td>• Mature processing technology</td>
<td>• High material requirements due to poor absorption</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Little room for efficiency increases</td>
<td></td>
</tr>
<tr>
<td>Cu(In, Ga)Se$_2$</td>
<td>• Highest thin film efficiencies</td>
<td>• Rarity/cost of indium</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Thin film</td>
<td>• Poor large-area consistency</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Expensive processing</td>
<td></td>
</tr>
<tr>
<td>Cadmium Telluride</td>
<td>• Moderate efficiencies</td>
<td>• Toxic</td>
<td>• Dominant thin-film technology</td>
</tr>
<tr>
<td></td>
<td>• Thin film</td>
<td>• Materials fairly rare</td>
<td></td>
</tr>
<tr>
<td>Amorphous/Nano-Crystalline Silicon</td>
<td>• Thin film</td>
<td>• Relatively low efficiencies</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Good absorption properties</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Easily adapted to tandem junction</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Organic</td>
<td>• Potentially extremely cheap to produce</td>
<td>• Very low efficiencies</td>
<td>• Very young technology</td>
</tr>
<tr>
<td></td>
<td>• Can easily be coated on flexible substrates</td>
<td>• Immediately degrade in the presence of light/O$_2$/humidity</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Easily adapted to tandem junction</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Thin film</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 1-1. A comparison between competing photovoltaic technologies is presented. The materials are listed in order of best efficiencies. The bottom four are thin-film technologies and thus require much less material, yet suffer from low efficiencies.
1.3 Amorphous and Nano-crystalline Silicon Thin Film Solar Cells

Traditional crystalline solar cells are built using a p-n junction. Due to their crystalline nature, they tend to have long diffusion lengths, allowing for excellent carrier capture across long distances. Amorphous and nano-crystalline silicon lack this long-range order, however. Carrier collection becomes a non-trivial issue. To solve this, engineers created a p-i-n structure. Intrinsic (undoped) silicon is placed between the traditional p and n layers, allowing the electric field created by the junction to be spread over greater distances, aiding carrier collection. The band diagrams and physical structure of traditional crystalline cells and thin film p-i-n junctions are compared in Figure 1-7.

![Figure 1-7](image-url)

Figure 1-7. A traditional p-n structure (a) provides electric field support to areas very close to the junction. In contrast, a p-i-n structure (b) allows the electric field to be spread over the width of the i-region, aiding in carrier collection. The structures of a p-n junction solar cell (c) and p-i-n junction solar cell (d) provide different advantages depending on the material used.
Crystalline silicon cells, with excellent diffusion lengths, consist of a simple p-n junction, as shown in Figure 1-7(c). Bus bars are used to aid in top current collection. A-Si and nc-Si do not have a long diffusion length, however. Therefore they use the electric field in the junction to aid carrier collection through the use of an i-layer. The i-layer spreads the electric field out over greater distance, allowing more carriers to be captured. This design is critical to the success of low diffusion length materials such as amorphous and nano-crystalline silicon.

A typical a-Si solar cell, shown in Figure 1-7(d), consists of several layers. The bottom is some type of metallic back contact, allowing for carrier collection. An n+ layer is then deposited, followed by a layer of intrinsic silicon. Care must be taken that as few impurities as possible exist in this layer. A p+ layer is deposited on top of this, followed by a transparent conducting oxide (TCO). This layer acts as an anti-reflective coating (ARC) and provides carrier collection. Typical TCOs include Zinc Oxide (ZnO) and Indium Tin Oxide (ITO).
1.4 Device Fabrication

Standard a-Si or nc-Si devices are both fabricated on stainless steel substrates approximately 1.5 inches by 1.5 inches. In order to prevent contaminants from entering the cell, the substrates are boiled in an acetone bath, rinsed in methanol, boiled in a 1:1:1 ammonium hydroxide: oxygen peroxide: water bath and sonicated in methanol. They are then placed into a plasma-enhanced chemical vapor deposition (PECVD) reactor. The reactor (Figure 1-8) allows gas to flow over the substrate, depositing material onto it at a uniform rate. The reactor creates plasma at 46 MHz.

![Figure 1-8. A simplified diagram of a PECVD reactor. Gases flow across the substrate and allow for very controllable deposition. Vacuum pumps are used to reduce the pressure to a workable level.][1]

The system is first pumped down to below .5 µT to remove any possible contaminants. For both nc-Si and a-Si cells, the n+ bottom layer is deposited first, using silane (SiH₄) as the silicon source and phosphene (PH₃) as the dopant source. The silane
is diluted with H$_2$ gas. The n+ layer is grown to approximately .25-.3 μm thick at a
temperature of 300C and a pressure of 50mT. For an a-Si sample, the i-layer is grown
approximately .3 μm thick at 200C. A small second intrinsic layer is deposited to match
p+. For a nc-Si sample, the i-layer is grown to approximately .9 μm thick. On top of both
an amorphous/nano-crystalline/amorphous p+ layer is deposited. The bottom amorphous
serves as nucleation sites for the nano-crystalline, which contains the majority of the
dopant atoms from the diborane (B$_2$H$_6$). Finally, an a-Si cap layer prevents the nc-Si from
oxidizing. To contact the device, ITO is RF sputtered at 13.5 MHz at 100W. Typically
λ/4 thicknesses are used, so approximately 70nm is deposited.

Samples measured for C-f are typically mesa etched to reduce short current and
improve noise. Black wax is deposited on top of the devices. The sample is then
immersed in a 10:3:3 de-ionized water: HNO$_3$: HF solution until the exposed silicon is
removed. It is then placed in a water bath to remove the acid then tri-cloro ethane to
remove the wax. It is then submersed in an acetone bath, methanol bath, and water bath
in quick succession. The sample is annealed for half an hour to dry and repair any
damage that may have been done. This anneal improves sheet resistance [17].
2. Theory and Literature Review

2.1 Defects in Semi-Conductors

When a physical defect appears in a crystalline lattice, such as an impurity or a broken bond, trap states can be created in the bandgap. These are states that can contain electrons and holes, just like the states created by the crystal lattice, except that these states occur mid-bandgap. These states will greatly affect the performance of the device, as derived below. A plot of various impurities and their respective location in the bandgaps of various materials is given in Figure 2-1.

![Figure 2-1. Different impurities will cause states in the bandgap of semiconductors. Often these states are intentional, such as the dopant states created by boron and phosphorous in silicon. Other impurities are less desirable, specifically those which create states near the middle of the gap. [8]](image-url)
For a single trap at a given energy level, four possible transitions are possible: electron capture, electron emission, hole capture, and hole emission [8]. It can easily be shown that for a single level trap the rate of recombination $R$ can be written as

$$R = \frac{np - n_i^2}{\tau_p(n_1 + n) + \tau_n(p_1 + p)}$$  \hspace{1cm} (2.1)

where $n$ and $p$ are the carrier concentrations and $\tau$ is the minority carrier lifetime. If we further assume low level injection, the recombination simplifies down to

$$R = \frac{\Delta n}{\tau_n}$$  \hspace{1cm} (2.2)

for p-type material. Recombination is controlled by the number of excess minority carriers available to recombine in a region, and is inversely proportional to the lifetime, that is, the average time a charge lasts before recombining. In a solar cell, the number of excess carriers is fixed for a given light intensity, so effort must be taken to improve the lifetime.
2.2 Measured Defects in nc-Si

As shown above, minority carrier lifetimes are a critical photovoltaic parameter. One of the major contributors to decreased lifetimes is trap states. A study using reverse recovery transients clearly showed that increased defects led to decreased lifetimes [14] in nc-Si. This result is detailed in Figure 2-2. Further, it was shown that defects are on the order of $10^{15}$ cm$^{-3}$, depending on deposition conditions.

![Figure 2-2. The lifetime of a material is greatly affected by the presence of defect states within the material. This result was calculated for nc-Si at the Microelectronics Research Center at Iowa State University. The measurement was made using reverse recovery transient techniques [14].](image)

In 2005 our group showed a direct relation between the doping levels in nc-Si and the calculated defect density [16]. The results are shown in Figure 2-3. Doping the material clearly creates large number of trap states. Though this was doped using phosphorus or boron, the same results apply to oxygen contamination, which is effectively a dopant.
Hugger, Cohen, *et al* studied the effects of excess oxygen in nc-Si [15]. They found that oxygen contamination greatly increased the deep defects within the sample. This agrees with measurements, as oxygen tends to form midgap states (see Figure 2-1). They found that oxygen contamination could increase deep defects up to an order of magnitude, destroying device performance (Figure 2-4).

Hugger also demonstrated the presence of trap states approximately near midgap [18]. He offered a model for the optical absorption of these states that varied based upon the crystallinity of the sample. Highly crystalline materials tend to absorb at about .6 eV, while less crystalline would tend towards 1.2 eV (Figure 2-5).
Figure 2-4. Excess oxygen creates defect states in a material. These defect states ruin the device performance. [15]

Figure 2-5. Two proposals for the optical absorption in nc-Si. In more crystalline materials (a), the absorption focused upon \(0.6\text{eV}\), while more amorphous materials (b) showed a \(1.2\text{eV}\) absorption. A Gaussian trap at midgap agrees with both external and internal findings.
3. Characterization Methods

3.1 C-V Measurements

It can easily be shown that

\[ \frac{C}{A} = \frac{1}{2} \left[ \frac{2q\varepsilon}{V_0 + V_R} N_{\text{scr}} \right]^{1/2} \]  

for a p+n junction where \( V_R \) is the applied reverse biased voltage. By plotting \((A/C)^2\) versus voltage and extracting the slope, we can calculate the charge in the region, \( N_{\text{SCR}} \).

Kimerling studied the effects that defects would have on this measurement [12]. He demonstrated that, assuming homogenous trap densities, the measured defect density would change as a function of position. When measuring traps near the junction, one measures \( N_D \) (Figure 3-1). In non-crystalline intrinsic materials, this corresponds to trap states near the conduction band (ie, tail states). When measurements are made deeper in the gap, the sum \( N_D + N_T \) is calculated. Thus, by subtracting the two we can get an accurate picture of defect densities deep in the material. In order to measure traps near the junction, low reverse bias is used. Measuring deeper traps is done at high reverse biases (ie, a wide junction). A sample C-V measurement is shown in Figure 3-2, demonstrating the two distinct regions in the device. Measurements were made at low frequencies and high temperatures to activate the deep traps.
Figure 3-1. The measured defect density changes as a function of position [11].

Figure 3-2. The C-V curve clearly shows two separate regions. The one at low reverse bias corresponds to $N_D$, while the curve at high reverse biases represents the sum of $N_D$ and $N_T$. 
3.2 Differential Capacitance Measurements

Capacitance versus frequency measurements allow for a in-depth study of defect profiles, as pioneered by Walter [13]. The lower in the bandgap a trap is, the longer it takes to emit its electron, assuming constant attempt to escape frequency (Figure 3-3). From basic carrier conservation, the capacitance contribution of a single trap state can be calculated. After integration over energy and space, the number of traps can be solved for

\[ N_t(E_\omega) = -\frac{U_d}{qw} \frac{dC}{d\omega} \frac{\omega}{kT} \]  \hspace{1cm} (3.2)

where \( U_d \) is the built in voltage, \( w \) is the width of the i-layer, \( k \) is Boltzmann's constant and \( T \) is the temperature in degrees Kelvin. \( E_\omega \) is the energy at which traps can respond to a given frequency, defined as

\[ E_\omega = kT \ln\left(\frac{2\nu}{\omega}\right) \]  \hspace{1cm} (3.3)

where \( \nu \) is the attempt to escape frequency of the material.

Taking into account how the AC signal changes over the junction, a more accurate equation can be written

\[ N_T(E_\omega) = -\frac{U_d^2}{w[qU_d - (E_{fp0} - E_\omega)]} \frac{dC}{d\omega} \frac{\omega}{kT} \]  \hspace{1cm} (3.4)
Figure 3-3. Traps deep in the band gap emit much slower than traps near the band edge. This allows us to measure them using differential capacitance techniques. A high frequency capacitance measurement may only reach the red line, and only the fast emitting traps will be detected. A measurement at a lower frequency may be able to reach the green line and thus detect both the fast emitting and medium emitting traps. By differentiating the measurement, we can figure out the contribution of just the medium emitting traps. This is the basic idea of the differential capacitance approach.
4. Measurement Parameters

4.1 Measurement Set-Up

The measurement stage was built in house by the author and is shown below. The stage (1) supports the sample. It is constructed of aluminum, chosen for its excellent heat conduction. The aluminum block is connected to a heater (2) with thermal paste in between to enhance conduction. A thermocouple (3) allows for accurate feedback of temperature information. The device is contacted through the use of two low noise gold probes (4) which can be moved using the dials on the right. Low noise cables (5) connect the probes to the meter, a Quadtech 1920 LCR Meter. This can be operated manually or controlled using a computer.

Figure 4-1. The measurement device used for C-f measurements, including the stage (1), heater (2), thermocouple (3), probes (4) and low noise cables (5).
Figure 4-2. The equivalent circuit of the Quadtech 1920 LCR meter.

The Quadtech uses the equivalent circuit in Figure 4-2 to measure circuits, using the equation

$$Z_x = R_s \left( \frac{E_x}{E_s} \right)$$

(4.1)

4.2 Noise Considerations

Capacitance measurements suffer from noise, particularly at low frequencies. Because this method requires taking the derivative of a capacitance curve, small noise in the capacitance causes quite noisy data in trap densities. Therefore, all efforts must be taken to reduce noise as much as possible. This will be done through two methods: minimizing the noise in the measurements and de-noising the data upon calculation.

4.2.1 Measurement Noise

As discussed above, the setup was constructed to minimize noise at every juncture of the measurement. However, the electrical settings of the Quadtech must be optimized as well. Noise is quantified in the following manner. A nc-Si sample was loaded onto the
stage. Ten measurements of its capacitance value were taken in rapid succession. The coefficient of variation of these samples is then calculated. The coefficient of variation is defined as the ratio between the standard deviation of the sample to the mean, that is

\[ CV = \frac{\sigma}{\mu} \]  

(4.2)

where \( \sigma \) is the standard deviation of the samples and \( \mu \) is the mean of the samples.

Essentially, the coefficient of variation is a normalized standard deviation that allows for comparison of noise even when the capacitance value changes, such as across different frequencies. It will be expressed as a percentage for this document. Unless otherwise stated below, measurements were taken at the following parameters: room temperature, 20 Hz frequency, 0V DC bias, 100mV AC measurement voltage, and 0 second delay before measurements. 20 Hz was selected because this is the typical frequency regime of high noise.

Before electrical profiling began, the probes were tested. It was found that several days of heavy operation would cause a great increase in noise. The sample was measured as described above. The probes were then gently cleaned with a KimWipe and isopropyl alcohol to remove any particles from their surface. The sample was immediately re-measured. The results can be found in Table 4-1. The CV improved by a factor of 24.97. Clearly, keeping the probes clean is vital to this measurement. It is standard procedure to clean the probes before each set of measurements.
Table 4-1. The capacitance measurements taken to profile the noise inherent in the C-f measurement set-up. Clearly, cleaning the probes is critical to a successful measurement. No valid conclusions can be made when the data varies as much as it does before cleaning was performed. Cleaning the probes is done before each set of measurements; this experiment was performed to demonstrate the necessity to the reader.

Next, the electrical properties of the Quadtech LCR meter were profiled. Only the results will be presented here. First, frequency effects were studied. Because of the necessity of varying frequency for the measurement, this is not a true optimization. It is critical, however, to understand how the noise affects the measurements. It is immediately clear from Figure 4-3 that noise is inversely proportional to the frequency. This is bad news for our measurements - the most important data (that is, deep traps) comes from low frequency measurements. Thus we must take great care to reduce the noise in the measurement.

Perhaps the most important electrical property is the AC signal voltage. This is the value of the small AC voltage applied to the sample in order to carry out the measurement. Too low of a value makes detecting changes difficult, while too large of a value can cause unwanted effects as the small signal regime is left. This is clearly shown
Figure 4-3. The coefficient of variation decreases rapidly with increasing frequency. At 500-1000Hz, successive measurements show virtually no noise. Because the most interesting data is taken at the inherently noisy low frequencies, care must be taken to reduce noise as much as possible.

Figure 4-4. The AC signal voltage is a critical parameter of the measurement. It is clear that approximately 100mV provides the least noisy sample. Too far from this value in either direction greatly increases sample noise. As mentioned above, this measurement was taken at 20 Hz with no DC bias and at room temperature.
in Figure 4-4. An AC signal voltage of 100mV provides the least noise. This value is used for all measurements. The Quadtech 1920 allows for averaging of measurements, that is, it will take a certain number of measurements and provide the average value. The CV results for this are presented in Figure 4-5. The theoretical noise improvement (proportional to the square root of number of samples) is plotted in red. Noise is greatly reduced by increasing the number of samples averaged. It is typical to use an average of at least 3 in current measurements. Noisier samples and noisier conditions (such as higher temperature) may require more averages.

![CV vs. Number of Samples Averaged](image)

**Figure 4-5.** Increasing the number of samples averaged greatly reduces noise and is of great use. Theoretically, noise should reduce proportional to the square root of the number of samples averaged, and this is plotted with the red line.

Further optimization was done, but in the interest of brevity only the results are mentioned here. A 25 ohm source impedance was chosen. The median measurement was
also shown to reduce noise, though not as sharply as increasing the number of averages. Finally, increasing the delay before measurements showed no appreciable effect on noise.

4.2.2 Wavelet De-noising

The development of wavelet de-noising of C-f was mainly done by Shantan Kajjam, however it bears brief mentioning here. Traditional de-noising is done through the use of a high pass filter. Because it removes high frequencies indiscriminately, it often removes interesting information that we would like to keep. Rather than breaking a signal into sin waves of varying frequency, a wavelet transform breaks a signal into wavelets of different scales (Figure 4-6). This process has several advantages over traditional Fourier transforms. The most significant for our application is that it can de-noise a sample without losing high frequency data through a process called thresholding. This discards only the details exceeding a user-set limit, allowing for de-noised signals that maintain their sharp high frequency peaks [9].

An example of a de-noised trap density is given in Figure 4-7. All de-noising was done with the wavelet toolbox in MATLAB. Interested readers are referred to [9]. Though this technique is quite useful for noisy data, advances in measurement noise reduction have generally reduced the noise to an acceptable level. Therefore, unless otherwise stated, results in this document will not have been filtered. Even though less data is lost through this process, filtering inevitably reduces the quality of the results. It is this author's belief that so long as the results are relatively noise-free that they be presented as is to endow as full an understanding as possible upon the reader.
Figure 4-6. A traditional Fourier transform breaks the signal into sin waves of differing frequencies. A wavelet transform breaks the signal down into wavelets of different scales and positions. [9]

Figure 4-7. De-noising helps to make a signal more clear, yet some information is still lost in the process.
5. Results and Analysis

5.1 Trap Density in Crystalline Silicon

Before studying non-crystalline materials, a check of the measurement strategy must be made. To do so, crystalline silicon was measured to serve as a baseline. Because of the crystalline nature of the material, trap levels should be exceedingly low. The measured capacitance as a function of frequency is shown in Figure 5-1. Unfortunately, measurements below 500 Hz proved too noisy to give valid data. Indeed, even the capacitance measurements above 500 Hz were quite noisy. This is a simple cause: the capacitance values of the crystalline silicon sample are quite small. Thus noise measured in tenths of picofarads, trivial for non-crystalline measurements, now plays a large role. Still, the point of this test is not to establish an exact measurement of trap states in crystalline silicon; hundreds of papers do so. Rather, it is used as a baseline for further measurements.

If the traps are assumed to be approximately constant throughout the bandgap,

\[
\frac{dc}{d\omega} \cdot \omega \text{ must be a constant. This means that capacitance as a function of frequency must be a logarithmic function. Clearly, after accounting for noise, this is the case in Figure 5-1. Thus,}
\]

Thus,

\[
\frac{dC}{d\omega} = -\frac{2.89}{\omega A} \frac{pF}{rad \ cm^2}
\]

where \(A\) is the area of the device, 9mm\(^2\). Thus, using the formulation in 3-4,

\[
N_t(E_\omega) \approx -\frac{U_d}{qw} \frac{dC}{d\omega} \omega = 1.08 \times 10^{13} \ cm^{-3} eV^{-1}
\]
Figure 5.1. (Top) The capacitance decreases as a function of frequency, though noise made measurements imprecise. This is due to the small values being measured in comparison with a-Si and nc-Si samples; this makes noise a larger factor. (Bottom) The calculated trap density is approximately constant. The negative trap states corresponds to the points in the C-f curve that increase with frequency and are due to noise. The diode had an area of 9mm$^2$. 

\[ y = -0.289 \ln(x) + 74.498 \]
\[ R^2 = 0.919 \]
We can then calculate the total trap density by integrating over energy. Since trap density is a constant with respect to energy

\[ N_t = N_t(E_\omega) \times E_g = 1.2 \times 10^{13} \text{ cm}^{-3} \]  

(5.3)

Thus it is observed that crystalline silicon has extremely low trap densities, as should be the case. It is important to note that the noise in the sample actually caused the trap density calculations to increase by a factor of 2. The reason is immediately clear when one compares the derivative of the function and the trendline.

5.2 Trap Density in Amorphous Silicon

Capacitance-frequency measurements were taken at six temperatures for 2-14758, a chemically annealed amorphous silicon sample. The higher temperature allowed for measuring much deeper traps, almost to the midgap. The capacitance measurements and results are plotted in Figure 5-2. Clearly, these traps fit a Gaussian profile quite well. The matched Gaussian has an \( E_0 \) of .7 eV, a \( \sigma \) of .19 eV, and \( N_0 \) equal to \( 4 \times 10^{16} \text{ cm}^{-3} \text{ eV}^{-1} \). Integrating this Gaussian over the bandgap gives a trap value of \( N_t = 1.35 \times 10^{16} \text{ cm}^{-3} \). Low frequency C-V measurements calculated a deep trap density of \( 1.2 \times 10^{16} \text{ cm}^{-3} \). Thus we see excellent agreement between C-V and C-f measurements, and the discrepancies are within experimental error.

We observe that the measured value for trap densities is three orders of magnitude higher than that for crystalline silicon. This is inherent in the nature of the material. The midgap states are created by the dangling bonds that constitute the material’s amorphous nature.
Figure 5-2. (Top) Capacitance measurements as a function of temperature and frequency. Higher temperature increases the emissions from traps, increasing the overall capacitance. (Bottom) The trap densities are found to fit a Gaussian profile quite well. Integration of this profile agrees with trap densities from C-V measurements.
5.3 Trap States in Nano-Crystalline Silicon

Capacitance - frequency measurements were taken at various temperatures for five different nano-crystalline silicon samples. One sample was created as described above. The next four were created in the presence of oxygen in order to study its effects. They were created at 9, 18, 27, and 36 sccm, respectively. The trap density was then measured for each sample and can be found in Figure 5-3. The profile at midgap as a function of oxygen was also determined. The results are shown in Figure 5-4.

Figure 5-3. The trap profile of samples created in the presence of oxygen. A clear tendency towards increased traps is shown with increasing oxygen.
Thus it is observed that increased oxygen greatly increases the defect density of nc-Si devices, and therefore harms the performance. These agree very well with both internal [14] and external [15] measurements. Comparison of Figures 5-4 and 2-4 yield very strong agreement.
6. Conclusion

This project attempted to demonstrate a new way to look at trap densities - specifically to see how they varied in energy, something that few other methods could accomplish. This was accomplished through the use of differential capacitance measurements. For the first time measurements of this type were made on amorphous silicon and nano-crystalline silicon.

It was shown that defects in crystalline silicon are approximately constant across the bandgap, with values that agreed exceedingly well with outside sources. It was demonstrated that traps in amorphous silicon were Gaussian in nature situated at approximately .7 eV below the conduction band. Finally it was confirmed that increased oxygen would greatly increase the defect densities in nano-crystalline silicon, damaging device performance.

This method allows for complete understanding of traps in semiconductor materials. It agrees well with both internal and external measurements and calculations. It is non-destructive and can easily be used as a diagnostic tool for device analysis, using only commonly available components. It is certainly a valuable tool to any photovoltaic designer who implements it.
7. References


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