1-13-2017

Transparent Ohmic Contacts for Solution-Processed, Ultrathin CdTe Solar Cells

J. Matthew Kurley  
*University of Chicago*

Matthew G. Panthani  
*Iowa State University, panthani@iastate.edu*

Ryan W. Crisp  
*Colorado School of Mines and National Renewable Energy Laboratory*

*See next page for additional authors*

Follow this and additional works at: https://lib.dr.iastate.edu/cbe_pubs

Part of the Chemical Engineering Commons, and the Nanoscience and Nanotechnology Commons

The complete bibliographic information for this item can be found at https://lib.dr.iastate.edu/cbe_pubs/379. For information on how to cite this item, please visit http://lib.dr.iastate.edu/howtocite.html.
Transparent Ohmic Contacts for Solution-Processed, Ultrathin CdTe Solar Cells

Abstract
Recently, solution-processing became a viable route for depositing CdTe for use in photovoltaics. Ultrathin (∼500 nm) solar cells have been made using colloidal CdTe nanocrystals with efficiencies exceeding 12% power conversion efficiency (PCE) demonstrated by using very simple device stacks. Further progress requires an effective method for extracting charge carriers generated during light harvesting. Here, we explored solution-based methods for creating transparent Ohmic contacts to the solution-deposited CdTe absorber layer and demonstrated molecular and nanocrystal approaches to Ohmic hole-extracting contacts at the ITO/CdTe interface. We used scanning Kelvin probe microscopy to further show how the above approaches improved carrier collection by reducing the potential drop under reverse bias across the ITO/CdTe interface. Other methods, such as spin-coating CdTe/A2CdTe2 (A = Na, K, Cs, N2H5), can be used in conjunction with current/light soaking to improve PCE further.

Disciplines
Chemical Engineering | Nanoscience and Nanotechnology

Comments
This document is the Accepted Manuscript version of a Published Work that appeared in final form in ACS Energy Letters, copyright © American Chemical Society after peer review and technical editing by the publisher. To access the final edited and published work see DOI: 10.1021/acsenergylett.6b00587. Posted with permission.

Authors
J. Matthew Kurley, Matthew G. Panthani, Ryan W. Crisp, Sanjini U. Nanayakkara, Gregory F. Pach, Matthew O. Reese, Margaret H. Hudson, Dmitriy S. Dolzhnikov, Vadim Tanygin, Joseph M. Luther, and Dmitri V. Talapin

This article is available at Iowa State University Digital Repository: https://lib.dr.iastate.edu/cbe_pubs/379
Transparent Ohmic Contacts for Solution-Processed, Ultrathin CdTe Solar Cells

J. Matthew Kurley, Matthew G. Panthani, Ryan W. Crisp, Sanjini U. Nanayakkara, Gregory F. Pach, Matthew O. Reese, Margaret H. Hudson, Dmitriy S. Dolzhnikov, Vadim Tanygin, Joseph M. Luther, and Dmitri V. Talapin

Department of Chemistry and James Franck Institute, University of Chicago, Chicago, Illinois 60637, United States
Department of Chemical and Biological Engineering, Iowa State University, Ames, Iowa 50011-2230, United States
Department of Physics, Colorado School of Mines, Golden, Colorado 80401, United States
National Renewable Energy Laboratory, Golden, Colorado 80401, United States
Center for Nanoscale Materials, Argonne National Laboratory, Argonne, Illinois 60439, United States

Supporting Information

ABSTRACT: Recently, solution-processing became a viable route for depositing CdTe for use in photovoltaics. Ultrathin (~500 nm) solar cells have been made using colloidal CdTe nanocrystals with efficiencies exceeding 12% power conversion efficiency (PCE) demonstrated by using very simple device stacks. Further progress requires an effective method for extracting charge carriers generated during light harvesting. Here, we explored solution-based methods for creating transparent Ohmic contacts to the solution-deposited CdTe absorber layer and demonstrated molecular and nanocrystal approaches to Ohmic hole-extracting contacts at the ITO/CdTe interface. We used scanning Kelvin probe microscopy to further show how the above approaches improved carrier collection by reducing the potential drop under reverse bias across the ITO/CdTe interface. Other methods, such as spin-coating CdTe/AxCdTe3 (A = Na, K, Cs, N2H4), can be used in conjunction with current/light soaking to improve PCE further.

Given the increasing interest in solar energy, creating high-quality absorber layers with efficient electrical contacts becomes increasingly important. CdTe is currently the most impactful thin-film photovoltaic (PV) technology, with over 10 GW installations. CdTe solar cells provide the lowest cost-per-Watt (~$0.25/W) among current PV technology. Even after 40 years of research, new insights into solar cell improvements, with regards to contacting CdTe, are being discovered. Most of the research has focused on physical vapor-deposited CdTe, namely, close-space sublimation (CSS) and sputtering, the leading technologies for highly efficient CdTe photovoltaics. The majority of solar cells utilize highly doped semiconductors, usually zinc telluride (ZnTe), as a buffer layer for the Ohmic contact to CdTe. Often, copper-doped ZnTe (ZnTe:Cu) has been used as an electron-blocking layer at the back contact in the superstrate configuration (illumination through substrate rather than through substrate). Recently, the power conversion efficiencies (PCEs) of solar cells utilizing the substrate configuration (light shining through top contact) were improved with the aim of using cheaper, flexible metal foils or polymers over more traditional rigid, glass substrates. Transparent Ohmic contacts are vital for development of tandem PV devices and allow for the creation of transparent photovoltaics to collect excess light from windows. Currently, only a few studies have produced such contact to CdTe. Ultrathin device designs also help to overcome limitations from Te scarcity by utilizing CdTe layers less than 500 nm thick. These thin layers are difficult to achieve through more standard deposition methods, such as close-space sublimation or sputtering.

Along with exploring more efficient contacts to CdTe, new methods for solution-processing CdTe have been investigated. Spin-coated, sintered CdTe nanocrystals (NCs) were first utilized in solar cells by Gur et al. in 2005 with PCE reaching about 2.9%. Further improvements by Jasieniak et al. increased PCE to around 7% by transitioning the n-type top layer to NC zinc oxide (ZnO) and fine-tuning the deposition parameters of CdTe. Panthani et al. and MacDonald et al. found devices can reach efficiencies of over 10% by using indium-doped ZnO (ZnO:In) deposited via a sol–gel method. In their reports, they...
Pursuant to the DOE Public Access Plan, this document represents the authors' peer-reviewed, accepted manuscript.

The published version of the article is available from the relevant publisher.

Figure 1. Schematic (a) and cross-sectional SEM image (b) of control device stack with ITO/CdTe/ZnO:In/Al geometry. (c) J–V curves of experimental (squares) and modeled (lines) devices under AM1.5G illumination progressively current/light soaked. Input parameters for modeled J–V curves can be found in the Supporting Information. (d) Cross-sectional SKPM data showing the topography (pink) with the normalized potential difference at +1 V (black), +0.5 V (red), −0.5 V (orange), −1.0 V (green), −1.5 V (blue), and −2.0 V (purple) bias across the device. (e) Band diagram created from AMPS-1D model and SKPM of potential difference depicting the origin of the potential difference spike under reverse bias (−1 V).

Determined illuminating the devices under solar simulated light (AM1.5G) at high forward bias (~3 V) increased device efficiency from ~3–4% to >10% PCE. Roussillon et al. demonstrated nonuniformity at interfaces can affect the photovoltage distribution within thin-film solar cells. Light and voltage can promote the formation of a blocking layer through an electrochemical reaction, balancing the nonuniformity. Later, Roussillon et al. demonstrated interfacial modification between a transparent conductive oxide and a semiconductor by using current/light soaking can establish a stronger built-in field. Such current/light soaking is believed to improve the band alignment at the interface between indium–tin oxide (ITO) and CdTe. PCE does not last, partially decaying over the course of 24 h and eventually diminishes to slightly better than the efficiency immediately after fabrication. While current/light soaking can be used multiple times, it is not a viable method for maintaining high efficiency.

We explored novel, solution-processed routes that are versatile, enabling transparent contacts, and removes the need for current/light soaking. Few approaches for creating effective electric contacts to CdTe have been explored in conjunction with these new materials processing techniques. Fewer studies have determined effective methods for transparent Ohmic contacts to CdTe. In this work, we studied a variety of methods for making transparent contacts to CdTe, including spin-coated Te, etched copper-doped CdTe (CdTe:Cu), and sputtered ZnTe:Cu. The open-circuit voltage ($V_{oc}$) improved dramatically by using these layers between ITO and CdTe, called interfacial layers, with $V_{oc}$'s reaching almost as high as 700 mV without current/light soaking. Unlike the $V_{oc}$ from current/light soaked devices, the device performance remained for well over a week. We used AMPS-1D modeling software developed by McElheny et al. to model the one-dimensional device geometry outlined by Panthani et al. and MacDonald et al. to better understand the current/light soaking treatment.

As-made devices created by Panthani et al. and MacDonald et al. required current/light soaking that partially degraded over the course of 1 week (Figure S7). This limitation to device performance was believed to be caused by the ITO/CdTe interface (Figure 1).

An as-made control device (Figure 1a,b) was investigated using cross-sectional scanning Kelvin probe microscopy (SKPM) to spatially resolve the electrostatic potential distribution across the device stack (Figure 1d). It showed a pronounced potential difference drop under reverse bias at the ITO/CdTe interface (Figure 1e). This barrier occurs because of poor contact between ITO and CdTe. Interestingly, the electric field is fairly constant throughout the majority of the CdTe absorber layer, indicating the depletion region spans most of the layer (green, Figure S8). Modeling, using AMPS-1D, closely agrees with the $J$–$V$ curves achieved through experiment (Figure 1e). It is important to note the inability of the model to account for inhomogeneity of the layers. However, general trends in the device stack can be elucidated. A systematic approach of matching the modeled device curve to the experimental results is outlined in the Supporting Information. As previously believed, the device performance improves as the work function of ITO (front contact) deepens. The short-circuit current density ($J_{sc}$) 235
improves slightly while the fill factor (FF), Voc, and PCE all increase dramatically. Jsc increases because the field strength throughout the device becomes strong enough to extract more of the electron−hole pairs generated from the absorption of photons without an increase in reverse bias. The difference between the Voc before (black, Figure 1c) and after (blue, Figure 1c) current/light soaking, ~340 mV, can be accounted for by the change in the front contact potential barrier, ~350 meV (Figures 2a,c and S5).

Normally, the work function of ITO ranges from 4.8 to 5.0 eV based on manufacturer specifications (Thin Film Devices Inc.). Using the specifications as a guide, the input parameters (outlined in the Supporting Information) were adjusted to create close agreement between experimental and modeled device performance. From the device parameters inputted, the work function of ITO is approximated at ~5.0 eV before current/light soaking (Figure 2a). The modeled work function lies on the deeper side of the range but still agrees with previous reports.27,28 Oxygen plasma cleaning, the treatment used to hydrophilize the substrates in preparation of spin-coating,29 was shown to increase the work function of ITO by removing surface adsorbates. Ding et al. found the work function of ITO was actually even higher, ~5.2 eV.27 We modeled heavily doped CdTe at the interface between ITO and the CdTe absorber layer to determine if such a method would improve Voc (Figure 2b,d). It improved by over 300 mV, indicating such a method might be useful in forming a transparent Ohmic contact to CdTe.

As-made devices with the geometry outlined by Panthani et al.19 and MacDonald et al.30 exhibit nonideality in forward bias. The nonideality occurs when one (or both) of the electrode(s) contain a barrier for extraction to the majority carrier(s). It is widely considered that rollover is caused by poor carrier collection dictated by thermionic emission (eq 1).31

\[ J_t = A^*T^2e^{-\Phi_b/kT} \]  

where \( J_t \) is saturation current, \( A^* \) the Richardson constant, \( T \) temperature, \( e \) the charge of an electron, \( \Phi_b \) the barrier potential, and \( k \) Boltzmann’s constant.

\( J−V \) curves under approximated AM1.5G illumination over a range of temperatures (Figure 3a) were taken to calculate a potential barrier. As the temperature increases, the barrier increases.
became less effective at blocking carriers from being captured, causing rollover to lessen. \( \frac{J}{T^2} \) was determined by applying a fit to the two regimes of linearity for each curve and calculating the intersection point (Figure S9). The potential barrier can be calculated by linearizing the relationship between \( J \) and \( T \) (eq 2).

\[
\ln \left( \frac{J}{T^2} \right) = -\frac{q\Phi_b}{k} \frac{1}{T} + \ln(A^*)
\]

When \( \ln \left( \frac{1}{T} \right) \) is plotted versus \( \frac{1}{T^2} \), the slope and y-intercept become \(-\frac{q\Phi_b}{k}\) and \(\ln(A^*)\), respectively. Linear fits using this method tend to overemphasize the lower-temperature points by decreasing their relative contribution to variance. The Richardson constant (222.6 mA/cm²/K²) for every curve was kept constant, and only \( \Phi_b \) was varied (Figure 3b). As \( \Phi_b \)
increases, $J_t$ will decrease significantly as well. The approximation of $\sim 0.35$ eV closely matches with the experimental data.

There are three major attributes interfacial layers (Figure 4a) must possess to become applicable contacts to CdTe: transparent, stable, and form an Ohmic contact to p-type CdTe. Interfacial layers must allow light to pass so the CdTe absorber layer can generate electron–hole pairs. They must also be stable over long periods of time to prevent considerable device degradation, otherwise current/light soaking would be a preferred option. Finally, interfacial layers must possess a deep work function (Fermi level) so as to prevent a Schottky-like contact to CdTe. We found etched CdTe:Cu (Figures 4b, 5a), Te (Figure 5b), and ZnTe:Cu (Figure S12a) worked well as interfacial layers.

A common method for establishing Ohmic contact to lightly doped CdTe is to increase carrier concentration at the CdTe/metal interface (Figure 2 b,d). Not only is it easier to create Ohmic contact to heavily doped CdTe, but also there would be no differences in the conduction or valence bands, no issues with materials incompatibility, and no adverse side reactions because it is the same material. Modeling of heavily doped CdTe located at the ITO/CdTe interface shows it could work to improve $V_{oc}$.

Attempts at creating heavily doped CdTe made by adding Cu-containing salts alone proved ineffective at improving $V_{oc}$. Most likely, Cu diffused out of the initial layer through the grain boundaries during the deposition of the CdTe absorber layer. In an attempt to prevent Cu from diffusing away from the ITO/CdTe interface, a saturated solution of NH$_4$I in IPA was used to impregnate the film with $I^-$. $I^-$ was shown to inhibit grain growth, which requires recrystallization to combine smaller grains into larger ones. Diffusion requires the same recrystallization processes, so the intention was to use $I^-$ to keep Cu in the interfacial layer. However, by simply soaking in a saturated NH$_4$I solution, $V_{oc}$ did not improve (black, Figure 4b). Another approach to forming Ohmic contact to CdTe is through a 10 volume % iodine/methanol etch. Along with pure saturated NH$_4$I solution, 0.375% I$_2$ solution in IPA was added to the NH$_4$I solution and used to soak the first layer. Mixing I$_2$ and I$^-$ forms $I_3^-$ in situ, indicated by a peak in ultraviolet–visible absorption at 236 nm (Figure S10a) and the solution turning yellow (Figure S10b). The samples were all soaked for 10 min to test how the etch concentration affects contact to ITO. An increase in $I_3^-$ concentration increases the etch rate, which will make the material more Te-rich. None of the samples with I$_2$ added required current/light soaking to achieve larger $V_{oc}$’s (Figure 4b).

Concentration is only one method of adjusting the properties of the final layer. Time can be used to control to what extent the etch proceeds. As shown in Figure S10, Cd 3d, Te 3d, and Cl 2p XPS were performed on etched CdTe:Cu soaked for 0 (black), 1 (red), 10 (blue), and 120 min in 0.375% I$_2$ solution in IPA. XPS helps determine time scales for each step of the etch (Figure S10d–f). The Te (Figure S10d) concentration relative to Cd (Figure S10e) increases with longer etch times. Most likely, Cd is solubilized by $I^-$ and removed from the film. Additionally, the extra peaks in the original Te XPS trace (black, Figure S10d) disappear. Previous accounts attribute those peaks to oxidized Te (TeO$_x$). Finally, all traces of Cl (black, Figure S10f) are removed within the first minute of the soak, indicating solubilization of surface CdCl$_2$. The likely explanation for these phenomena is reduction of TeO$_2$ with NH$_4$I (eq 3) and oxidation of CdTe to Te with Cd being solubilized (eq 4). Also, a well-known reaction between Cu(II) and $I^-$ should take place (eq 5).

<table>
<thead>
<tr>
<th>Chemical Reaction</th>
<th>Equation</th>
</tr>
</thead>
<tbody>
<tr>
<td>TeO$_2(s) + 4$NH$_4^+ + 6I^-$</td>
<td>(3) 238</td>
</tr>
<tr>
<td>$\rightarrow Te(s) + 2$H$_2$O + 2I$_3^-$ + 4NH$_3$</td>
<td></td>
</tr>
<tr>
<td>CdTe(s) + I$_3^-$ -&gt; Te(s) + Cd$^{2+} + 3$I$^-$</td>
<td>(4) 239</td>
</tr>
<tr>
<td>2Cu$^{2+} + 5$I$^-$ -&gt; 2CuI + I$_3^-$</td>
<td>(5) 240</td>
</tr>
</tbody>
</table>

Figure 5. (a) $J$–$V$ curves of CdTe solar cells under AM1.5G illumination. Cells were made using etched CdTe:Cu interfacial layer devices with 0.375% I$_2$ added to saturated NH$_4$I in IPA soaked for 0 (black), 1 (red), 3 (green), and 5 (blue) minutes followed by CdTe interfacial layer deposition. (b) SKPM scans showing the normalized potential difference at $\pm$1 V bias for the control device (black), 1 min (red), and 5 min (green) etched CdTe:Cu interfacial layer devices with 0.375% I$_2$ added to saturated NH$_4$I in IPA. (c) $J$–$V$ curves under AM1.5G illumination for interfacial layer devices using Te dissolved in NH$_4$I, 0.1 M (black), 0.5 M (red), and 1.0 M (blue) Te in NH$_4$I, spin-coated at 3000 rpm onto ITO-coated glass and annealed at 350 °C for 30 min followed by CdTe interfacial layer deposition. (d) $J$–$V$ curves under AM1.5G illumination without current/light soaking for interfacial layers using Cu or Ag to dope CdTe. Cu$_2$Te NCs added to CdTe NCs (black), CuCl$_2$ added to CdTe NCs (red), Cu electrochemically deposited (green), or Ag NWs spin-coated (blue) onto ITO-coated glass for the first layer followed by CdTe interfacial layer deposition. (e) $J$–$V$ curves under AM1.5G illumination for 0.375% I$_2$ added to saturated NH$_4$I etched CdTe:Cu etched for 5 min interfacial layer device immediately after fabrication (black) and aged for 1 week (red). (f) $J$–$V$ curves under AM1.5G illumination for spin-coated at 3000 rpm 0.1 M Te in NH$_4$I annealed at 350 °C for 30 min interfacial layer device immediately after fabrication (black) and aged for 1 week (red).
$V_{oc}$ increased, to a point, with a longer etch time (Figure 5a). Eventually, the entire CdTe film can be dissolved (120 min, Figure S10c). Devices made with etched CdTe:Cu interfacial layer yielded efficiencies of ~7.0% for PCE with 514 mV, 21.9 mA/cm², and 63% for $V_{oc}$, $J_{sc}$, and FF, respectively. Average values on one substrate were ~6.1% for PCE with ~510 mV, ~19.3 mA/cm², and ~63% for $V_{oc}$, $J_{sc}$, and FF, respectively. The largest discrepancies lie with $J_{sc}$ which is typical of the methods employed for CdTe deposition. With better control over processing conditions, devices are expected to become more efficient and consistent.

Etched CdTe:Cu interfacial layer devices etched for 1 and 5 min with 0.375% I₂ added to saturated NH₄I in IPA along with the control device were measured using cross-sectional SKPM (Figure Sb). Both the control device (black, Figure Sb) and 1 min etched CdTe:Cu (red, Figure Sb) devices showed a potential change at the ITO/CdTe interface under reverse bias. However, with the 5 min etched CdTe:Cu (green, Figure Sd) device, the feature is absent. $V_{oc}$ is improved significantly, ~250 mV, for the device etched for 5 min, so an absence of the potential drop agrees with device improvement. Under forward bias, there is a large potential drop for the device etched for 5 min (black, Figure 4d), indicating a barrier to extracting electrons. There is a sharp drop at the CdTe/ZnO:In interface under reverse bias (green, Figure 4d), believed to be caused by locally doping CdTe. Doping of the CdTe absorber layer shortens the depletion region, which causes the potential drop to occur in a narrower area. If the field does not span the entire CdTe layer, then electrons and holes would need to diffuse to the contacts, increasing the likelihood of recombination. This can explain the loss of $J_{sc}$ as etch time increases (Figure 5a).

Another approach to the formation of transparent Ohmic contact to CdTe involved a thin layer of Te. Te can be solution-processed from polytelluride (Te₅⁻) ions dissolved in N₂H₄ (eq 6).

$$2n\cdot\text{Te} + 5N₂H₄ → 4N₂H₅ + 2Te₅⁻ + N₂$$  

N₂H₄ can reduce Te to Te²⁻, but not fully to Te⁵⁻, giving the solution a deep purple color. Upon spin-coating and annealing at 200 °C, the purple Te²⁻ solution transitions back to elemental Te. The CdTe NC solution wets the surface of the CdTe layer, so the CdTe absorber layer is easy to deposit on top to finish the device stack. When the concentration of Te in N₂H₄ is varied, the thickness of the interfacial layer can be changed, influencing the overall device performance (Figure S12).

Mott–Schottky analysis (Figure S12b) illustrates the improvement in built-in potential ($V_{bi}$) of the as-made devices, leading to an increase in $V_{oc}$. Lines of the linear region were drawn to estimate $V_{bi}$ by extending them to the x-intercept. The estimations for $V_{bi}$ match closely to measured $V_{oc}$’s (Table S6). Differences between $V_{bi}$ and $V_{oc}$ arise from discrepancies with the linear fit in Mott–Schottky measurements as well as differences in the measurements themselves. Because Mott–Schottky measurements are taken in the dark versus J–V being taken under AM1.5G illumination, there are subtle differences in the potential differences measured. Te layers that are too thick result in reduced $J_{sc}$ because Te absorbs light. When EQE is measured (Figure S12c), it becomes clear that making the Te layer thicker increasingly attenuates the light reaching the CdTe layer. The differences in $J_{sc}$ follow the same trends in EQE. As the Te layer gets thicker, EQE drops, but more dramatically with green light (~500 nm). By increasing the spin-coating speed to 3000 rpm and changing the annealing temperature to 350 °C, J–V characteristics improved (Figure 5c).

Increasing spin-coating speed thinned the layer to allow more light to reach CdTe, and increasing the annealing temperature makes the Te layer more crystalline. Te is less likely to diffuse through the grain boundaries in a crystalline state over an amorphous state. FF was significantly improved from a decrease in series resistance, as seen by the slope at $V_{oc}$. By exploring different processing conditions, the device performance can be even higher. Devices with spin-coated Te yielded efficiencies of ~7.0% for PCE with 597 mV, 19.7 mA/cm², and 59% for $V_{oc}$, $J_{sc}$, and FF, respectively. Average values on one substrate were ~6.1% for PCE with ~597 mV, ~19.0 mA/cm², and ~52% for $V_{oc}$, $J_{sc}$, and FF, respectively. The largest differences once again were from $J_{sc}$.

Attempts at simply adding Cu salts to the CdTe NC ink failed to produce an appreciable difference in device performance (red, Figure 5d). Cu most likely diffused through the grain boundaries, removing substantial amounts of Cu from the ITO/CdTe interface. Ag nanowires (blue, Figure 5d) completely shorted the device. Electroplated Cu failed to improve contact between ITO and CdTe (green, Figure 5d). $J_{sc}$ was probably diminished by a combination of mirroring and oxidation. Depositing Cu in the form of Cu₃Te NCs proved to be a viable method for improving contact between ITO and CdTe (black, Figure 5d). By trapping Cu in a lattice instead of pushing it to the grain boundaries, the $V_{oc}$ improved dramatically. The best device yielded PCE as high as ~8.6% for PCE with 685 mV, 21.3 mA/cm², and 59% for $V_{oc}$, $J_{sc}$, and FF, respectively. Unfortunately, this method proved to be rather inconsistent. Further optimization will be necessary to improve batch-to-batch reproducibility.

$V_{oc}$ for $Γ/1Γ$-etched CdTe:Cu and spin-coated Te remained high through the course of a week without considerable change (Figure 5e,f). Long-term degradation of device performance can be partially attributed to the formation of an intermetallic between Al and Ag. Pfeifer et al. observed a degradation of Ag-coated Al electrical contacts over time attributed to the formation of resistive intermetallics, Ag₅Al and Ag₃Al. All devices were made with the Al/Ag interface degrade in such a manner. However, $V_{oc}$ changed little, indicating etched CdTe:Cu and spin-coated Te created stable Ohmic contacts over longer periods of time than current/light soaking.

Because it has already found use for Ohmic contacts in conventional devices, another possible material for creating a transparent Ohmic contact to CdTe is ZnTe:Cu. It has a wider band gap (2.35 eV) than CdTe and is more easily doped p-type with Cu. With its conductive band above that of CdTe, ZnTe acts as an electron-blocking layer, preventing recombination at the back contact. All of these factors make ZnTe:Cu a possible interfacial layer. A sputtered layer of copper-doped zinc telluride (Figure S13a) proved effective at improving $V_{oc}$ SKPM showed ZnTe:Cu (Figure S14) interfacial layer devices demonstrated similar device response to etched CdTe:Cu soaked for 5 min.

Solution-processed ZnTe:Cu was attempted by starting with (N₂H₄)₂ZnTe prepared using the methods outlined by Mitzi et al. Adding Cu to N₂H₄ had its own challenges. N₂H₄ is a strong enough reducing agent to reduce Cu in CuCl to Cu metal, making solubilizing Cu halide salts difficult. Acetonitrile coordinates to Cu(1) metal centers well enough to prevent reduction, but it is not strong enough to prevent a reaction between Cu(1) and ZnTe. A brown suspension developed from the formation of Cu₃Te as the two solutions were mixed. Cu is not the only element to dope ZnTe. Romeo et al. showed Sb can dope ZnTe p-type by lying on the Te site of the lattice. Kovalenko et al. determined a preparation for Sb₃Te₅$\cdot$N₂H₆
which mixes with (N₂H₄)₂ZnTe without reacting. When enough is added, V_{oc} can improve to as high as 573 mV (Figure S13b). However, J_{sc} decreases substantially, making PCE even lower than the control device without current/light soaking.

Interestingly, current/light soaking still improves V_{oc} in the lower Sb₂Te₃ content interfacial layer devices (Figure 6a).

The overall device performance improved for both cases, but more noticeably for the device with Sb₂Te₃−N₂H₄ added. (N₂H₄)₂ZnTe alone was too resistive to improve greatly with current/light soaking. However, a slight addition of Sb₂Te₃−N₂H₄ added to (N₂H₄)₂ZnTe was spin-coated onto ITO-coated glass and annealed at 200 °C for 30 min followed by CdTe absorber deposition. (b) J−V curves under AM1.5G illumination after current/light soaking for interfacial layers using spin-coated ZnTe, Sb₂Te₃−N₂H₄ (0%, black and 1%, red by mole) added to (N₂H₄)₂ZnTe was spin-coated onto ITO-coated glass and annealed at 200 °C for 30 min followed by CdTe absorber deposition.

The overall device performance improved for both cases, but more noticeably for the device with Sb₂Te₃−N₂H₄ added. (N₂H₄)₂ZnTe alone was too resistive to improve greatly with current/light soaking. However, a slight addition of Sb₂Te₃−N₂H₄ added to (N₂H₄)₂ZnTe was spin-coated onto ITO-coated glass and annealed at 200 °C for 30 min followed by CdTe absorber deposition. (b) J−V curves under AM1.5G illumination after current/light soaking for interfacial layers using spin-coated ZnTe, Sb₂Te₃−N₂H₄ (0%, black and 1%, red by mole) added to (N₂H₄)₂ZnTe was spin-coated onto ITO-coated glass and annealed at 200 °C for 30 min followed by CdTe absorber deposition.

Table 1. Compiled Data of the Best Device Performance without Current/Light Soaking

<table>
<thead>
<tr>
<th>interfacial layer</th>
<th>PCE (%)</th>
<th>V_{oc} (mV)</th>
<th>J_{sc} (mA/cm²)</th>
<th>FF (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>no interfacial layer</td>
<td>4.0</td>
<td>385</td>
<td>24.5</td>
<td>38</td>
</tr>
<tr>
<td>etched CdTe:Cu</td>
<td>7.0</td>
<td>514</td>
<td>21.9</td>
<td>63</td>
</tr>
<tr>
<td>spin-coated Te</td>
<td>7.0</td>
<td>597</td>
<td>19.7</td>
<td>59</td>
</tr>
<tr>
<td>CdTe:Cu from Cu(I)₅Te NCs</td>
<td>8.6</td>
<td>685</td>
<td>21.3</td>
<td>59</td>
</tr>
<tr>
<td>sputtered ZnTe:Cu</td>
<td>4.8</td>
<td>552</td>
<td>15.5</td>
<td>57</td>
</tr>
<tr>
<td>spin-coated ZnTe</td>
<td>2.4</td>
<td>573</td>
<td>7.7</td>
<td>53</td>
</tr>
</tbody>
</table>

The best device achieved PCE of ~12.7% with 726 mV, 24.6 mA/cm², and 71% for V_{oc}, J_{sc}, and FF, respectively. Typical values on one substrate were ~11% for PCE with ~700 mV, ~23 mA/cm², and ~70% for V_{oc}, J_{sc}, and FF, respectively. While CdTe/(N₂H₄)₂CdTe₂ does not create an Ohmic contact, it can be useful in combination with layers that do.

In conclusion, we described a variety of methods for improving V_{oc}, showing long-term stability without the need for current/light soaking. Many of the methods use solution-processing and are easily integrated into typical device fabrication processes.

All methods described above improve the contact between ITO and CdTe but have different limitations that require further optimization (Table 1). Some contacts need to increase transparency, consistency, or conductivity, all of which can be improved by testing different processing conditions. Two methods, etched CdTe:Cu and spin-coated Te, have better longevity than current/light soaking (Table S7).

Chemical engineering of the ITO/CdTe interface does not always eliminate the need for current/light soaking. At the same time, such treatments improve V_{oc} and overall device performance of current/light soaked devices. We saw such behavior in devices with a spin-coated layer of ZnTe precursor doped with Sb₂Te₃ (Table S8). Spin-coated interfacial layers of CdTe NCs capped with A₂CdTe₂ ligands (A = Na, K, Cs) also improve V_{oc} and PCE as the alkali cation increases in size, presumably because of lower diffusivity (Table S8). All of the methods we explored are compatible with one another. A combination of ZnTe:Cu, Te, and CdTe/(N₂H₄)₂CdTe₂ could be used to form a graded device stack. Te and CdTe/(N₂H₄)₂CdTe₂ would act as a barrier, preventing Cu from diffusing into the CdTe absorber layer. All of these layers are transparent, making dual transparent electrodes possible (Figure S5). One can envision utilization of such electrodes in semitransparent PV devices and tandem cells. A general strategy for interfacial engineering discussed in this study offers guidelines for improving performance and stability of other PV and photodetector devices that utilize solution-processed semiconductors.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsenergylett.6b00587.

Experimental procedures, spectral data, and structural and electrical characterization (PDF)
Solar Cells. 

**ACKNOWLEDGMENTS**

This work was supported by the Office of Naval Research under grant number N00014-13-14090, by the NSF MRSEC Program under Award No. DMR-14-20703, by the Department of Energy (DOE) Sunshot program under Award Number DE-EE0005312, and by II-VI Foundation.

**REFERENCES**


(12) Parilla, P. A.; Callahan, R.; Dabney, M. S.; Berry, J. J.; Talapin, D. V.; Luther, J. M. Nanocrystal Grain Growth And Device Architecture For High-Efficiency CdTe Ink-Based Photovoltaics. ACS Nano 2014, 8, 9063–9072.


Chemical Polishing Of CdTe And CdZnTe In Iodine-Methanol Etching


