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Comparison of low power, wide tuning range 5 GHz quadrature phase LC CMOS VCO with different devices for resonant circuit

by

Jo Yi Foo

A thesis submitted to the graduate faculty in partial fulfillment of the requirements for the degree of

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Program of Study Committee:
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This is to certify that the master’s thesis of

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has met the thesis requirements of Iowa State University
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ABSTRACT

Three low power 5 GHz LC cross-couple quadrature VCO with different resonant circuits were designed and fabricated in a standard 0.18μm single-poly, six metal layer mixed-signal CMOS process. Combination pairs of an active inductor, spiral inductor, junction varactor and MOScap are used to make the resonant circuit of the quadrature VCO in order to have the best possible performance circuit. Active inductor used in the design is a simple common-source amplifier structure with a PMOS feedback while the passive inductor used is a spiral inductor design using two of the highest level of metal in the process. Junction varactors used in the resonant circuit made use of the capacitance of NWELL and P-implant. All three VCO's have the same topology structure, which is the LC cross-coupled structure. This architecture is used in the design because of the simplicity while the cross-coupled featured will minimize the phase noise of the oscillator. Output drivers and predrivers are design to drive the VCO to a 50 ohm load. Phase noise, power dissipation, output power, spectrum accuracy and quadrature phase error are looked for and tested both in the simulation and on chip. Results of all three different types of resonant circuit VCO's are compared and discuss. All the circuits were fabricated through the MOSIS Educational Program.
1.0 INTRODUCTION

Recent growth in the wireless telecommunication area has lead to the rising need of RF circuits that are low power, low noise and embedded system on chip (SOC). As the wireless telecommunication technology becomes more and more advanced, transceiver and receiver system blocks are becoming more and more complicated to design for SOC. Most of the receivers and transceivers used in a wireless system nowadays utilize quadrature (I/Q) signals generation. Hence, this has become one of the most challenging issues for designing receivers and transceivers circuit blocks since most of the RF circuits available are either single-ended or differential. In the need to provide a solution to this issue, an increasing interest is shown in the design of quadrature phase generation circuit. [1] A quadrature phase signal VCO in the gigahertz range becomes very attractive to the wireless telecommunication world, especially for systems that use zero-IF topologies.

This project focuses on the design and test of several blocks of a quadrature phase voltage control oscillator that uses the cross-coupled LC oscillator topologies but utilizes different kind of devices for its resonant tank. Three different types of resonant tank devices are used: 1) Active inductor and MOScap, 2) MOScap and spiral inductor, and 3) Junction varactor and spiral inductor. A cross-coupled LC oscillator topology was chosen because it has very few transistors, is easy to implement and is differential in nature, thus making it easier to generate quadrature signals. Moreover, this topology consumes lower power, which is very suitable for transceiver and receivers system used in the wireless telecommunication system. Another advantage of this architecture is the easy computation of the LC resonant tank that determines the fundamental frequency of the oscillator. Moreover, by supplying the correct configuration of the resonant tank, the LC topologies will bandpass the fundamental
frequency in the range of frequencies that the VCO is designed for and hence, reducing harmonic distortion.

This project also focuses on the importance of design for test in the sense of impedance matching with test equipment and parasitic capacitance from wafer probing. Hence, the output driver and pre-driver are designed with consideration of the issues of testing. The circuits' blocks design are in the 5 GHz range and are suitable for use in 802.11a and IEEE 802.11b WLAN system. The design was fabricated through MOSIS's Educational Program using TSMC 0.18µm process. This thesis covers circuit analysis, post layout simulated results, lab measurement, and a conclusion.

1.1 LITERATURE REVIEW

Since the 90's, people have shown interest in fully-integrated CMOS quadrature phase oscillators. However, not many people work in depth on quadrature phase oscillators since it can be replaced by two differential oscillators added together with delays. However, with the increasing demands for a smaller SOC and the rising interest in wireless telecommunication technology, the importance of quadrature phase VCO’s starts to take precedence. Most of the integrated quadrature phase oscillators designed at around the 1 GHz range before the current process technology existed used discrete inductors instead of spiral on chip inductors for their VCO resonance circuit [15]. However as submicron process technology becomes more and more advanced, the use of a spiral inductor become more common. With the use of a spiral inductor on chip, the center frequency of the current designed quadrature VCO starts to increase to meet the demand for Bluetooth, and IEEE802.11 b specification.
Different kinds of structures of quadrature phase VCO's have been investigated, such as quadrature coupled VCO (this work), polyphase I-Q VCO scheme, and VCO + frequency divider scheme [5]. Block diagrams of both the polyphase I-Q VCO and the VCO+ frequency divider scheme VCO can been seen in Fig. 1. [5].

![Block diagram of (a) Polyphase VCO topology; (b) Frequency divider VCO topology](image)

Both structures shown in Fig. 1 are more commonly used for quadrature signal generation and show better performance than LC coupled quadrature VCO [5]. However, it can be concluded that at higher frequencies, LC coupled quadrature VCO's are easier to design and give better performance. In [1] and [2] a fully integrated quadrature VCO of around 2 – 5 GHz is presented. In both paper discussions, quadrature phase VCO topology is used for the LC oscillator. Both VCO’s presented have a good phase noise with low power. The VCO designed for this project makes use of the LC topologies at 5 GHz using CMOS technology.
2.0 BASIC RESONANT CIRCUIT

One of the most important parts of an LC VCO is the LC resonant tank. The resonant tank is the basic configuration to control the oscillation frequency of an LC oscillator. The basic tank configuration of an LC oscillator is as seen in Fig. 2. From Fig. 2, L represents the inductance of the tank while C represents the capacitance. Both \( R_L \) and \( R_C \) are the parasitic of the inductance and capacitance respectively.

![Figure 2. Basic LC resonant tank](image)

Looking at the formation of the resonant tank, the impedance of the circuit can be described as

\[
Y = -G + \frac{1}{jwL} + jwC = -G + j(wC - \frac{1}{wL}) \tag{1}
\]

From the analysis of (1) can be seen that at DC, the inductor will be shorted out and the impedance becomes capacitive while at high frequency, the capacitor will be shorted out and the impedance becomes inductive. [11] Hence, the resonance frequency exists when the reactance of the impedance becomes zero as shown in (2)
\[ wL - \frac{1}{wC} = 0 \Rightarrow f_c = \frac{1}{2\pi} \sqrt{\frac{1}{LC}} \] (2)

Resonance frequency is also referred to as the center frequency of the tank which dominantly controls the main oscillator frequency of the tank and the oscillation frequency for this project. In order for the resonance tank to resonate without any loss coming from parasitic, the parasitic resistance and capacitance coming from both the inductor and resistor need to be compensated. Therefore, the calculation of \( C \) in (2) needs to include and take into consideration all the parasitic capacitance in the resonant circuit. As for the compensation for parasitic resistance, a negative resistance, \(-R\) is formed in the tank in order to cancel out both of the parasitic resistances. However, in a real form, negative resistance does not exist. Hence, there is a need to form a negative resistance some other way.
3.0 CROSS-COUPLE QUADRATURE PHASE OSCILLATOR DESIGN

3.1 CROSS-COUPLE SCHEME

For this project, a negative resistance is formed by cross-coupling transistors that are connected to the resonant tank. In Fig. 3, one of the differential oscillators used in the quadrature phase oscillator design is shown.

By cross-connecting the output to the input of the oscillator, negative resistance that has the same conductance as the transistor’s transconductance ($g_m$) is created. As can be seen from (3), $g_m$ depends solely on the square root of the bias current. Since resistance is then the inverse of $g_m$, negative resistance becomes the inverse of the square root of the bias current.
$g_m = \sqrt{2\mu C_{ox} I_D \frac{W}{L}}$ (3)

3.2 QUADRATURE PHASE VCO DESIGN

The proposed quadrature LC VCO architecture is implemented by cross-coupling two identical differential LC oscillators as shown in Fig. 4. [1]-[2] The differential LC oscillator topologies use the same as the structure used in Fig. 3.

When two identical differentials VCO are connected to each other, both oscillator phase delays are forced to synchronize with each other. However, with the cross-connected connection between the outputs and inputs of the first oscillator to the second oscillator, the difference in phase delay of both oscillators becomes 90-degrees to each other. [2]

Three quadrature phase VCO's are designed for this project. All three VCO's make use of the same architecture, which is the cross-coupled LC structure. However, all three VCO’s make use of different components for the resonant circuit:- 1) The first VCO uses a passive spiral inductor and junction varactor, 2) the second VCO uses a passive spiral inductor and MOScap and 3) the third VCO uses an active inductor and MOScap. Different components for the
resonant circuit are used to investigate the best performance that a low power quadrature phase VCO can achieve. The basic circuit structure used for all VCOs can be seen in Fig. 5. For all the different schematic structures of the VCO’s, refer to Appendix A.

![Figure 5. Basic cross-couple LC quadrature phase VCO schematic](image)

Each of the three combinations of components of the resonant circuits has its advantage and disadvantage. The first combination using a passive spiral inductor and junction varactor has a high Q factor even though the passive inductor takes up a lot of chip area. The second combination of passive spiral inductor and MOScap has a high Q factor too but it takes up even more chip area in comparison to the first combination. However, the second combination of resonant tank also has more parameters to manipulate and change when compared to the first combination. The third combination of MOScap and active inductor consumes the least chip area but has the widest tuning range. However, one of the major disadvantages of the third combination is that the use of both active devices results in a low Q factor.
4.0 DEVICES USED IN RESONANCE CIRCUIT

4.1 JUNCTION VARACTOR VS. MOSCAP

4.1.1 JUNCTION VARACTOR

Junction varactors are used in the VCO component design because of its small chip area, power consumption and ease of design. Moreover, a junction varactor model and layout used can be generated from the process technology library used for this project. A junction varactor is basically the same thing as a junction p-n diode connected in reverse bias. Hence, the capacitance for the varactor is from across the P+ active area in the N-Well. Its equivalent circuit model can be seen in Fig. 6.

From the circuit, D is the diode created from P+ and N-Well, \( C_p \) is the parasitic capacitance, and \( C_{sub1} \) and \( C_{sub2} \) are substrate capacitances while \( R_{sub} \) is substrate resistance.
Capacitance from the junction varactor can be calculated by using the general varactor equation as seen in (4) where $C_j$ is the junction capacitance when there is no bias voltage applied to the varactor. $V_R$ and $V_J$ are reverse bias voltage and junction voltage respectively while $K$ is the capacitance grading coefficient and $C_P$ is the parallel capacitance.

$$C_V = \frac{C_j}{K} + C_P \left(1 + \frac{V_R}{V_J}\right) \quad (4)$$

From (4), it can be seen that capacitance on the junction varactor varies with the reverse voltage applied.

### 4.1.2 MOSCAP

Another type of tunable option for a capacitor used for the VCO is a MOScap. A MOScap is formed by connecting both the drain and source of a NMOS transistor together to create one port while the gate forms the other port of the capacitor. The parasitic gate to source and gate to drain capacitances are then taken advantages of by varying the voltage going through the shorted drain and source connection. The equivalent circuit of a MOScap is seen in Fig. 7.
The capacitance of the MOScap is calculated by looking at the current going through the device in reference to voltage and time as in (4)

$$C = I \frac{\partial t}{\partial V}$$  \hspace{1cm} (5)

In order to calculate the capacitance from the circuit model, a ramp voltage is provided to the gate port of the capacitor and the current in reference to time going through the MOScap is measured. Since both the drain and source of the NMOS are tied together, the transistor is always in saturation mode as long as the gate voltage is not more than the voltage going through the tied connection.
Hence, the capacitance of the MOScap can be varied by the control voltage fed to the tied connection and also from the width and length of the transistor according to (6)

\[ I_d = \mu C_{ox} \frac{W}{2L} (V_{gs} - V_t)^2 \]  \hspace{1cm} (6)

**4.1.3 CONCLUSION OF JUNCTION VARACTOR VS. MOSCAP**

Through looking at both different structures of variable capacitance, i.e., MOScap and junction varactor, it can be concluded that both have their own advantages and disadvantages. Ultimately, by using the junction varactor, less chip area is consumed but at the expense of a narrower tuning range compared to a MOScap, which provides more tuning range at the design stage. This is because a junction varactor is created solely from a P-N material while MOScap is a component which gave us more options of varying its physical value. A junction varactor also has a higher Q-factor compared to a MOScap because a MOScap is an active component while a junction varactor is a passive component which has less loss. However, when comparing the ease of capacitance computation, the MOScap capacitance is easier to compute compared to a junction varactor.

**4.2 SPIRAL INDUCTOR VS. ACTIVE INDUCTOR**

**4.2.1 SPIRAL INDUCTOR**

Passive spiral inductors are used in the VCO component design because spiral inductor have a high Q factor, which will let the VCO have a better phase noise performance. Passive spiral
inductors are implemented using the two highest metal levels available from the process technology file. An equivalent lumped model of the spiral inductor used can be seen in Fig. 8.

![Figure 8. Equivalent spiral inductor model](image)

In Fig. 8, $L_s$ is the series inductance, $R_s$ is the series resistance of the metal layer used to form the inductor, $C_s$ is the capacitance between the spiral turn and the center of the inductor, $C_{ox1}$ and $C_{ox2}$ are the oxide capacitance, $R_{sub1}$ and $R_{sub2}$ are the substrate resistances and $C_{sub1}$ and $C_{sub2}$ are substrate capacitances respectively. Even though passive spiral inductors have a high Q factor, they take up a lot of chip area and are very complicated to design. Three different inductance values of spiral inductors are available from the process technology files. Layouts of the spiral inductor used for this project are generated from the process.
4.2.2 ACTIVE INDUCTOR

Another option of inductor that can be used in the VCO tank design is an active inductor. The definition of an active inductor in this project meant that the inductance from the inductor is generated from active circuits. The proposed active inductor design used a simple common source connected NMOS transistor with resistive feedback. This method of active inductor design mainly makes use of the impedance generated from the closed-loop connected circuit to form its inductance. When an NMOS transistor is common source connected and uses closed-loop feedback with a resistive feedback, high impedance is generated based on the value of the feedback component. Hence, in order to get a wider degree of freedom to vary the feedback resistance values, a PMOS transistor is used instead of a real resistor. The proposed active inductor schematic can be seen as in Fig. 9.

![Active Inductor Schematic](image-url)

**Figure 9.** Active inductor schematic
When using a PMOS transistor as a feedback, inductance of the active circuit can be varied and is not fixed to a certain value. This is because the inductance value can be varied by varying the control voltage to the gate of the PMOS device. Also, center frequency peaking obtained by the inductor can be varied since the impedance of the PMOS device changes according to the applied control voltage. By doing small-signal analysis of the active inductor, the output impedance of the circuit is derived. The small-signal analysis of the active inductor is as seen in Fig. 10(a). [4]

Figure 10. (a) Small signal model of active inductor; (b) Real inductor model
In the small-signal model, resistor $R_F$ is the feedback resistance that is represented by the PMOS transistor in Fig. 9. When the PMOS transistor in Fig. 8 is in the active region, then the resistance can be calculated by looking at (7).

\[
    r_{ds} = \frac{2L}{\lambda \mu_p C_{ox} W (V_{intra} - V_t - V_{tp})} = R_F \tag{7}
\]

From (7), can be seen that the resistance of the PMOS transistor can be controlled by its width, length, and also control voltage feed to the gate.

Hence, again looking at the small-signal model of Fig. 10(a), the output impedance of the active inductor can be calculated based on (8).

\[
    Z_{out} = \frac{1 + SR_F (C_{gs} + C_{gs})}{g_m + S^2 C_{gs} C_{gs} R_F + S[C_{gs} + C_{gs} g m R_F]} \tag{8}
\]

By looking at the output impedance equation of the active inductor in (8), it can be seen that $R_F$ plays an important role in the changes of the total impedance. The small-signal model of the active inductor is then compared with a real inductor model. Through the analysis of the real inductor model, the output impedance can be calculated as (9).

\[
    Z_{ind} = \frac{1 + SL}{R_p + \frac{S^2 C_p L}{R_p} + S C_p} \tag{9}
\]

By comparing the output impedance of both the small-signal model and those of the real inductor model, it can be observed that they are similar.

Therefore, it can be concluded that the parameters in the inductor model can be replaced by the circuit parameters in the active inductor. By doing this, the relationship
between the parameters in the active inductor and passive inductor is as seen in (10.1) through (10.3). It is noted that from (10.3) the inductance is inversely proportional to the transconductance of the NMOS transistor, while the feedback resistance, $R_F$ is directly proportional to the inductance.

\[
R_p = \frac{1}{gm} \quad (10.1)
\]
\[
C_P = C_{gs} + C_{gd} gm R_F \quad (10.2)
\]
\[
L = \frac{R_F (C_{gs} + C_{gd})}{gm} \quad (10.3)
\]

This relationship shows that the inductance of the active inductor can be controlled by the transconductance of the NMOS transistor and $R_F$, which is generated by the width, length and control gate voltage of the PMOS transistor as seen in (7). By doing an AC analysis of the active inductor used in this project, the reactance is as seen in Fig 11.

![Figure 11. Active inductor reactance](image)
4.2.3 CONCLUSION OF SPIRAL INDUCTOR VS. ACTIVE INDUCTOR

After looking through both design of the active and passive spiral inductor, it can be concluded that each has its own advantage and disadvantage. One of the main advantages of the spiral passive inductor is its high-Q factor in comparison with the active inductor, which have a really low Q factor. However, the geometric layout area of the active inductor is just one-tenth of the geometric layout of the spiral inductor with the same value of inductance. Hence, in a big system where chip area is very limited for each circuit block, using an active inductor in a VCO design will free up a lot of chip area for the other circuit blocks. Another advantage for using an active inductor in the VCO is that its frequency tuning range is increased if used with a varying capacitor in a tank since both tank components can be varied in comparison with using a passive inductor.
5.0 OUTPUT DRIVER AND PRE-DRIVER DESIGN

5.1 OUTPUT DRIVER DESIGN

All of the three cores VCO are designed to drive a high impedance output load in order to retain a high peak to peak voltage swing and low power. However, most of the high frequency test equipment available in the market currently is designed and matched to a fifty ohm load. Hence, in order to reduce signal reflection, impedance mismatch, and to get the most possible accurate results when testing the VCO, output drivers that drive a fifty ohm load are needed. For this project, a unity voltage gain output driver is designed. A unity voltage gain output driver is designed in order to retain and get back as much as possible of the original voltage swing from the core VCO without adding any significant noise or gain to the peak to peak output voltage swing.

There are currently a lot of different structures and architecture of output drivers in the literature. However, for this project, a CML or current mode logic topology output driver is chosen. This structure is chosen because it is differential in nature, easy to design and makes use of a passive resistor load instead of active load. Noise figure of the circuits are minimized when a passive load is used instead of active load. Hence, the total noise figure of the VCO would not be significantly affected or increased by the noise figure from the output driver. Since all the three core VCO’s designed have a quadrature output, by having a differential output driver it will reduce output error phase mismatch of the VCO when testing it. Moreover, differential circuits are easy to design since the left and right topologies are symmetry to each other. Hence, the total amount of transistors used is also reduced and thus lower the total power of the whole circuits.
The CML output driver used in this project is as seen in Fig. 12. The way CML circuit work is basically steering the current, \( I_d \) coming in from the previous circuit that is connected to its input gate to either of one of the transistors based on the input. The output of the CML then swings between \( V_{dd} \) and \( V_{dd} - \Delta V \) where \( \Delta V \) is voltage drop through the resistive load, hence giving the form of, current, \( I_d \), multiplied by the resistive fifty ohm load, \( R \). A current mirror or any current sources are not used in the design in order to have a lower current sinking and also a direct path to ground. Also, by eliminating the use of any current source, power dissipation of the output driver is greatly reduced.

Figure 12. Output driver schematic
However, the output driver is left to steer a very high biasing current since it is trying to drive a low impedance output coming from a high impedance input. Thus, very large transistors are needed in order not to burn the whole circuit out. However, when very large transistors are used, then the total circuit power will be increased. In order to solve this problem, pre driver stages are added in between the core VCO and the output driver to help the output driver in managing and spreading out the high current.

5.2 PRE-DRIVER DESIGN

For this project, pre-driver stages are needed in order to help the output driver in steering a very high biasing current when trying to drive a low impedance output while maintaining the original output voltage swing coming out from the core VCO. The pre-driver stages make use of common-source amplifier topologies. This structure is chosen for this project because of the ease in designing it and minimal usage of transistors which will help minimize noise. However, unlike the output driver, pre-driver stages make use of an active load instead of passive load. Instead of having a resistor as the load, pre-driver stages use an active inductor as its load.

The main reason pre-driver stages use an active inductor is in order to have inductor peaking at the design frequency. In order to maintain the original output signal swing coming out from the core VCO, pre-driver stages need to have wide bandwidth so that none of the signal is lost or clipped off. A resistive load will not provide as wide a bandwidth as an inductive load. Also, by having high bandwidth at the pre-driver stages, it will ensure that the VCO peak to peak output amplitude will not be lost and minimize any ISI in the output of the whole circuit.
In order to meet the criteria of this project, three stages of pre-drivers are needed between the core VCO and the output driver. Each stage of the pre-driver stages is designed to steer about the same amount of currents in order to maximize the best performance. The first stage of the pre-driver has the smallest size of transistors in order to have a small input capacitance. In the second stage of the pre-driver, transistors sizes are increased about twice the sizes of the first stage while the third stage of the pre-driver transistors sizes are again increased about twice thereof the second stage of the pre-driver in order to have a large driving capability to lower the impedance. The size increases of the transistors at each stage of the driver kept the current and impedance reduction stable and constant through the whole circuits. The schematic of the pre-driver stages can be seen in Fig. 13. Unity gain at 5GHz with reasonable bandwidth is able to be achieved with three pre-driver stages and an output driver. The schematic of the pre-driver stages connected to the output driver can be seen in Appendix B.
Figure 13. Three stages of pre-driver
6.0 LAYOUT

Geometrical layout is one of the most important parts of the project. Even with a prefect design, the geometrical layout may have significant mismatch and if not given enough attention, then the whole chip would not be working. Hence, for this project, geometrical layout is given the utmost attention. When laying out the design, one of the most important rules is that all of the current density rules for the process used are followed closely. This is to ensure that the chip would not burn up when current is flows through the entire metal path in the design. Hence, each and every metal path in the design needs to have enough width to handle the amount of current that is going to be flow through the path. However, if the metal path width is too wide, then too much parasitic capacitance will be added to the whole chip and this change the whole circuit impedance and design.

Hence, another important issue of layout that needs to have close attention is the parasitic that is going to be associated with the design. A parasitic that is formed between each metal layer when laying it out can drastically change the end result of the circuit. Thus, when an initial calculation at the design stage is done, a parasitic calculation based on the process used is included and taken into account. Another important aspect of geometrical layout that needs to be taken into consideration is electro static discharge or better known as ESD. Human touch, test probe and the surrounding air can cause static discharge and hence burn the chip out during the testing process. Hence, when there is direct connection from a test pad to the gate of the transistor, ESD protection circuit blocks are placed to prevent static charge. For this project, ESD protection circuit blocks used are from [4]. The schematic of all the ESD protection circuit blocks used can be seen in Appendix C. In order to further
maximize the performance of the chip, a ground plane is created evenly around the core circuits to minimize any interference such as EMI (electromagnetic interference).

Another important aspect of physical layout that needs close attention paid to it is device mismatch. When device mismatch occurs, then circuit behavior will be influenced and change. Hence, in order to reduce the possibility of device mismatch, common-centroid, multi-fingered, and serpentine techniques are used when dealing with large size devices. Also, when these techniques are applied in circuit layout, noise figure of the circuit can be minimized. In order to further minimize noise, such as switching noise, a bypass capacitor is placed in between a power and ground connection. By having a bypass capacitor from the power supply to ground, the noise current coming from the switching of voltage that is going to the circuits will go through the bypass capacitor instead of the power buss. The bypass capacitor calculation is based on equation (5).

The three chip layout can be seen in Appendix D. The whole chip area for the active inductor and MOScap VCO is 760 µm x 760 µm, which includes a quadrature VCO, six pre-drivers, two output drivers to drive the quadrature output and the pads. The other two VCO's with spiral inductors have the same chip area of 1645 µm x 752 µm. Even though the chip area for the VCO with a junction varactor and spiral inductor is supposed to be smaller than the VCO with a MOScap and spiral inductor, the spiral inductor area is too large and dominates the total chip area. The core VCO with an active inductor and a MOScap tuning chip area without including the output driver and pre driver is 128 µm x 150 µm. The core VCO's for the other two VCO has the same chip area of 518 µm x 752 µm.
7.0 RESULTS

7.1 TESTING

All three VCO were simulated and fabricated in the 0.18 um mixed-signal, six metal layers, and single poly process technology. The power supply used for all VCO's is 1.8 V. Results from the VCO's are compared and discussed with each other. Both of the VCO's which have a spiral inductor as part of their tuning tank did not have any real lab results and hence, the results discussed for both VCO's are post-layout simulation results. However, VCO's with an active inductor discussed in this project are actual results from lab testing.

Lab testing was done on all three VCO's. A spectrum analyzer, network analyzer, and oscilloscope were used to test the VCO. A spectrum analyzer is used to check for the tuning range of the frequency while a network analyzer is used to test for negative resistance of the VCO. A real time oscilloscope is used to check for phase errors between the quadrature signals. RF cascade probes are used to probe the chip under a microscope. A top level block diagram of the VCO under test can be seen in Fig. 14.
A DC block is used in order to prevent voltage coming out from VCO from burning out the test equipment. When testing is done, an ionic fan and electrostatic band is used to prevent static discharge from the air, human touch, and probe tester touched to burn out the chip.

### 7.2 RESULTS DISCUSSION

All of the three VCO spectrums are looked at and output power and center frequency is observed and recorded. The spectrums of the VCO can be seen in Fig. 15.
Figure 15.1. Spectrum of VCO with spiral inductor and junction varactor as resonant circuit

Figure 15.2. Spectrum of VCO with spiral inductor and MOScap as resonant circuit
As tuning voltage is changed, spectrums of the VCO’s are shifted to its respected frequency consequently. From the observation of the spectrum, the tuning range of all the VCO’s versus frequencies are compared among each other as can be seen in Fig.16. Individual graphs of each of the VCO tuning ranges versus frequency can be seen in Appendix E. From Fig. 16, it can be seen that the trace with an active inductor and a MOScap have the highest range of frequency variation compared to the other two VCO’s. The trace with a junction varactor and a spiral inductor as part of the resonance circuit has the lowest range of frequency variation. Also, it is noticed that for the trace with a junction varactor, frequency decreases as tuning voltage is increased as opposed to the other two traces where frequency increase with tuning voltage. This is due to the fact that junction varactor is in the reverse bias mode.
Figure 16. Frequency versus tuning voltage of all three VCO

A summary of the tuning range versus frequency of all the VCO's can be seen in Table 1. From observing the summarization results of Table 1, it can be concluded that the VCO with an active inductor and a MOScap resonance circuit has the widest tuning range variation.

<table>
<thead>
<tr>
<th>VCO Configuration</th>
<th>Tuning Range (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active Inductor and MOScap</td>
<td>494</td>
</tr>
<tr>
<td>Spiral Inductor and junction varactor</td>
<td>300</td>
</tr>
<tr>
<td>Spiral Inductor and MOScap</td>
<td>330</td>
</tr>
</tbody>
</table>

The VCO with an active inductor and a MOScap has the widest tuning range because both the inductor and MOScap can be varied. The trace of the tuning voltage versus frequency of the VCO with an active inductor and a MOScap shown in Fig. 16 is when the...
tuning voltage for both devices has the same voltage. That particular VCO was tested with several combinations of capacitor tuning voltage and inductor tuning voltage and the it gave the best performance when both tuning voltages are set to the same value. The trace of the other combination tuning voltage versus frequency can be seen in Appendix E.

Phase noise results for all the VCO are based on simulation as can be seen in Fig 17.

Figure 17.1 Phase noise for VCO with spiral inductor and junction varactor
Figure 17.2 Phase noise for VCO with spiral inductor and MOScap

Figure 17.3 Phase noise for VCO with active inductor and MOScap
Based on the three graphs of phase noise for all three VCO shown in Fig. 15, Table 2 gives a brief summary of the results.

<table>
<thead>
<tr>
<th></th>
<th>Phase Noise (dB/Hz) @ 1MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active Inductor and MOScap</td>
<td>-74.6</td>
</tr>
<tr>
<td>Spiral Inductor and junction varactor</td>
<td>-98.4</td>
</tr>
<tr>
<td>Spiral Inductor and MOScap</td>
<td>-87.3</td>
</tr>
</tbody>
</table>

The phase noise of the VCO with an active inductor and a MOScap has the worst phase noise of all the three VCO’s, while the VCO with a spiral inductor and a junction varactor has the best phase noise. This is because the VCO with an active inductor as its resonant circuit have a low Q-factor and hence there is a lot of loss compared to the VCO with a spiral Inductor.

In order to check for quadrature signal phase error of VCO, the DUT (device under test) is probed and connected to a real time 3GHz oscilloscope. Before resuming testing, the oscilloscope is tested for initial phase signal error by inputting an ideal sin wave signal from a signal generator to it. The error generated from this calibration setup was about a 10 degree phase error. Hence, the actual real signal phase error of the VCO when a DUT is connected to oscilloscope is the result measured minus 10 degree. The quadrature signal phase error of all VCO’s is checked and can be seen in Fig. 18.1 and Fig. 18.2.
Figure 18.1. Transient response of VCO with active inductor and MOScap

Figure 18.2. Transient response of VCO with spiral inductor and junction varactor
From Fig. 18.2 and 18.3, it is noted that the VCO's have no signal phase error between its quadrature VCO. This is because both VCO's transient responses are not tested on chip and instead the results are from post layout simulation. However, Fig. 18.1 shows an actual measured result. The signal phase error is around 7-degree at 4.21 GHz. The signal is measured at around 4 GHz even though the VCO has center frequency of 5 GHz because the real-time oscilloscope only provides accurate results up to 3 GHz. So, even by measuring at around 4 GHz one pushes the limit of accuracy of the oscilloscope.

Table 3 summarizes the results of all the three quadrature VCO's. Looking at Table 3, and comparing the results of all three VCO's, it can be seen that the VCO with an active inductor and a MOScap as the resonant circuit has the highest power dissipation. However, it is noted that the results for the other two VCO's are simulation based while the results for the VCO with an active inductor is measured based.
### Table 3. Summary of results

<table>
<thead>
<tr>
<th>Results</th>
<th>Simulated Junction Varactor and spiral inductor (VCO 1)</th>
<th>Simulated MOScap and spiral inductor (VCO 2)</th>
<th>Simulated Active inductor and MOScap (VCO 3)</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>1.8 V</td>
<td>1.8 V</td>
<td>1.8 V</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Current (core)</td>
<td>5.3 mA</td>
<td>5.4 mA</td>
<td>3.815 mA</td>
<td>7 mA</td>
</tr>
<tr>
<td>Center Frequency</td>
<td>5.025 GHz</td>
<td>4.945 GHz</td>
<td>5.0 GHz</td>
<td>5.09 GHz</td>
</tr>
<tr>
<td>Tuning range</td>
<td>300 MHz</td>
<td>330 MHz</td>
<td>350 MHz</td>
<td>494 MHz</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>9.54 mW</td>
<td>9.72 mW</td>
<td>6.86 mW</td>
<td>12.6 mW</td>
</tr>
<tr>
<td>Output Power</td>
<td>-6.12 dBm</td>
<td>-6.16 dBm</td>
<td>-2.956 dBm</td>
<td>-31.33 dBm</td>
</tr>
<tr>
<td>Phase noise (@1MHz)</td>
<td>-98.4 dBC/Hz</td>
<td>-87.3 dBC/Hz</td>
<td>-74.6 dBC/Hz</td>
<td>N/A</td>
</tr>
<tr>
<td>Phase Error</td>
<td>0 degree</td>
<td>0 degree</td>
<td>0 degree</td>
<td>~ 4 - 10 degree</td>
</tr>
</tbody>
</table>

Hence, a possible cause of higher power dissipation for VCO 3 might be process variation during the fabrication stage since simulation results shows power dissipation about the same as the other two VCO's. However, VCO 3 still has a low power dissipation of just 12.6mW. Again, looking at the output power of all VCO’s can be seen that VCO 3 has a really low amplitude and small signal peak from the noise floor. Signal loss of VCO 3 at the output might have been caused by a larger parasitic capacitance compare to what is compensated for at the driver stages.

Even though VCO 3 have the worst output power and phase noise, this VCO has the widest tuning range of almost 500 MHz with acceptable low power dissipation.
VCO 3 also shows a quite clean quadrature signal that is almost free of phase errors. Hence, from the observations of the results of all three VCO, it can be concluded that VCO 3 have the best performance for this project of a low power, quadrature phase VCO.

7.3 CHIP #1 FAILURE ANALYSIS

This chip # 1 consists of VCO 1 and VCO 2 and of two chips fabricated, chip #1 did not work as designed when measured in the lab and probe tested. However, no results can be obtained from both circuits. There are several possible reasons for the chip failure of both VCO’s such as:-

- Spiral inductor and junction varactor
- ESD
- Coupling among the inductor

The spiral inductor and junction varactor used in this project use device models provided from the process library. Hence, the geometric layout of both devices is also available from the process library. However, the spiral inductor and junction varactor used is only limited to certain sizes. Both devices were never tested at the desired frequency of this project and the workability of both devices was never confirmed. Also, when putting two VCO in a limited chip area with a large spiral inductor, isolation of all inductors might not be enough thus causing coupling among the spiral inductors. When coupling occurs among the inductors, mutual inductance will cause discrepancy at the resonance circuit of the VCO. Another possible reason for the failure of the chip might be cause by the ESD circuit. Even though
ESD protection circuit blocks are used, they were of smaller capacitance than the one used for the chip that consists of VCO 3.
8.0 CONCLUSION

Two separate fabrication runs of chip which consist of three VCO's with different resonant structures, pre-drivers, output drivers, and ESD protection blocks were fabricated. The first chip was not able to yield any result when measured and tested in the lab. However, the failure of the first chip lead to a better understanding on the importance of layout and an ESD protection circuit block. Hence, the second chip was successfully designed and tested in the lab. The idea of designing a quadrature phase VCO comes because of the unavailability and limited numbers of this particular kind of circuit in the market when demand becomes higher in the current wireless telecommunication technology. This paper started off with discussing the basic resonant structure design used for most LC VCO's that can be found in the market. It was then followed by a step-by-step solution of the design of a cross-couple quadrature phase VCO from schematic through layout level. In between, a discussion on the various active and passive devices used for the resonant circuit of the VCO was conducted. In order to be able to test the VCO using test equipments matched to fifty ohm, the design of pre-drivers and output drivers with a wide bandwidth are discussed from transistor level up to layout. Lab measurements of the second chip on the VCO with active inductor and MOScap showed a working circuit with a wide tuning range of around 500 MHz with a center frequency of 5 GHz and a low power dissipation of 12.6 mW.
APPENDIX A: VCO SCHEMATIC

A1. LC QUADRATURE PHASE VCO WITH JUNCTION VARACTOR AND SPIRAL INDUCTOR SCHEMATIC
A2. LC QUADRATURE PHASE VCO WITH MOSCAP AND SPIRAL INDUCTOR SCHEMATIC
A3. LC QUADRATURE PHASE VCO WITH MOSCAP AND ACTIVE INDUCTOR SCHEMATIC
APPENDIX B: PRE-DRIVER AND OUTPUT DRIVER SCHEMATIC
APPENDIX C: ESD PROTECTION CIRCUIT BLOCKS

C1. ESD PROTECTION BLOCK FOR GROUND PIN

C2. ESD PROTECTION BLOCK FOR DC INPUT PIN
C3. ESD PROTECTION BLOCK FOR VDD PIN
APPENDIX D: CHIP LAYOUT AND PHOTOGRAPH

D1. TOP LEVEL LAYOUT OF VCO WITH SPIRAL INDUCTOR AND JUNCTION VARACTOR
D2. TOP LEVEL LAYOUT OF VCO WITH SPIRAL INDUCTOR AND MOSCAP
D3. TOP LEVEL LAYOUT OF VCO WITH ACTIVE INDUCTOR AND MOSCAP
D4. WHOLE CHIP LAYOUT OF D1. AND D2.
D5. CHIP PICTURE OF VCO WITH ACTIVE INDUCTOR AND MOSCAP AS RESONANT CIRCUIT, DRIVERS, ESD PROTECTION BLOCK AND PADS
D6. CHIP PICTURE OF VCO WITH ACTIVE INDUCTOR AND MOSCAP AS RESONANT CIRCUIT, AND DRIVERS
APPENDIX E: FREQUENCY VS. TUNING VOLTAGE PLOTS

E1. FREQUENCY VERSUS TUNING VOLTAGE OF VCO WITH JUNCTION VARACTOR AND SPIRAL INDUCTOR AS RESONANT CIRCUIT

Frequency vs. Tuning voltage

![Graph showing the frequency vs. tuning voltage plot. The frequency decreases as the tuning voltage increases.](image-url)
E2. FREQUENCY VERSUS TUNING VOLTAGE OF VCO WITH MOSCAP AND SPIRAL INDUCTOR AS RESONANT CIRCUIT
E3. FREQUENCY VERSUS TUNING VOLTAGE OF VCO WITH ACTIVE INDUCTOR AND MOSCAP AS RESONANT CIRCUIT

- $V_{\text{capture}}$ is when capacitor tuning voltage is varied while setting inductor voltage to zero.
- $V_{\text{indtune}}$ is when inductor tuning voltage is varied while setting capacitor voltage to zero
- $V_{\text{cap}} = V_{\text{ind}}$ is when both capacitor and inductor tuning voltage is varied at the same voltage.
BIBLIOGRAPHY


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