Design of a digital signal processing system on chip for an eddy current probe

Brian J. Reed
Iowa State University

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Design of a digital signal processing system on chip for an eddy current probe

by

Brian J. Reed

A thesis submitted to the graduate faculty
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

Major: Electrical Engineering

Program of Study Committee:
Robert J. Weber, Major Professor
Mani Mina
Xiaoli Tan

Iowa State University
Ames, Iowa
2006

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This is to certify that the master’s thesis of

Brian J. Reed

has met the thesis requirements of Iowa State University
DEDICATION

This thesis is dedicated to my parents, Jon and Gayle Reed. Without their constant love and support I would not be where I am and who I am today.

I am also grateful for the love and helpfulness of my brother Matt, the rest of my family, and my friends Phil Staver, Eric Denney, Alex Morris, Jenny Lindberg, Ryan Rock, Corey Yearous, Chris Rieck, Sven Soell, Justus Gries, Imad Abbadi, Sharon Huertas-Cesky, and Mike Cesky.
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<td>M</td>
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ABSTRACT

In 1965 Gordon Moore, co-founder of Intel, observed that the number of transistors per square inch on integrated circuits had doubled every year since the integrated circuit was invented. Moore predicted that this trend would continue for the foreseeable future. In subsequent years, the pace slowed down, but data density has doubled approximately every 18 months, which is the current definition of Moore’s Law. The Semiconductor Industry Association roadmap derived from Moore’s Law promotes continuation of the decrease in minimum feature size and wafer size increase as the bases for the semiconductor industry’s successful future. This continuation of the decrease in minimum feature size and increase in wafer size has a number of important implications. One such important implication is that there will be an increase in chip manufacturing cost. This increase in die manufacturing cost has caused chip designers to investigate the implementation of single chip systems instead of the traditional design of multiple chip systems. The benefit of having a single chip system is that it can provide the same performance yet consume less space and power than multiple chip systems, which in turn cut manufacturing cost. The research conducted describes the design and implementation of an integrated circuit digital signal processing system for an eddy current probe. For this project a digital signal processing system that removes noisy signal components and amplifies the signal produced by an eddy current probe was designed. The purpose of this system is to have the ability to detect cracks in a material and to output that information to an ADC, which then is used to provide digital information to a computer for interpolation. In order to create a digital signal processing system capable of this, multiple building blocks are needed. This includes the design of a low pass filter, a variable gain amplifier which incorporates an operational amplifier and digital-to-analog converter, a current bias cell, and a shift register. An analysis and discussion of the design and fabricated integrated circuit in a TSMC 0.18 micron process is presented.
1 INTRODUCTION

The propulsion system of an aircraft, military or commercial, has always been considered a major aircraft subsystem. As performance requirements become more demanding as technology evolves, the design and integration of these systems has become more complex. The complexities of these systems pose unique technical and integration challenges to the designer and manufacturer. These challenges are especially true in military aircraft, where ever-increasing tactical mission requirements and an early sustained focus on affordability have driven the development and application of new technologies to achieve those challenges. Since those first developments, increasingly more-demanding missions and performance requirements have driven continual advances, not only in engine technology itself but also in the tools used to develop and apply that technology to new systems. This project takes advantage of one such tool, an eddy current probe, to create a device that is used for on wing inspections of a jet engine that is shut down to perform routine maintenance. In an eddy current probe, electrical currents are generated in a conductive material by an induced alternating magnetic field. The electrical currents are called eddy currents because they flow in circles on and just below the surface of the material. Interruptions in the flow of eddy currents, caused by imperfections, dimensional changes, or changes in the material’s conductive and permeability properties, can be detected with the proper equipment [1]. In the paper “Wireless Eddy Current Probe for Engine Health Monitoring,” a prototype digital processing system with wireless communication designed with discrete components that uses an eddy current probe to detect cracks in turbine blades was successfully demonstrated [2]. The next stage of this project is to take that prototype and integrate it into a single chip that will fit inside of a jet engine through borescope holes used for inspections. The borescope holes have a diameter of 1/2 inch to 5/8 of an inch depending on whether it is a military or commercial engine. This limits the size of the overall device. The completed system requires other circuitry to produce a functional system, thus the design of the digital signaling processing system circuitry is only discussed in this thesis. The digital signaling processing system circuitry covers the design and implementation on chip of a low pass filter, shift register, potentiometer, operational amplifier, and digital-to-analog
converter. Also discussed in this thesis are the considerations that went into the overall system design and the measured results of that system.

1.1 General Overview

This thesis will only focus on the design and development of the digital signal processing architecture, Figure 1.1, and the implementation of the various cells required to complete the design.

![Digital signal processing architecture diagram](image)

Figure 1.1: Digital signal processing architecture

Section 2 focuses on the design of the low pass filter used to remove noise from the eddy current probe signal. In Section 3, the shift register which is used to control the different gain amplifier settings is discussed. The gain amplifier, discussed in Section 4, uses variable amplification to amplify the signal from the eddy current probe which detects interruptions in the flow of eddy currents from both small and large cracks. The gain amplifier is a critical device that incorporates a potentiometer, operational amplifier, and digital-to-analog converter discussed in Sections 5, 6, 7 respectively. Section 8 covers the overall design of the system, while Section 9 focuses on the measured results that are produced from the fabricated chip.
2 LOW PASS FILTER DESIGN

2.1 Introduction

The low pass filter is used to remove any signal component from the eddy current probe over 10 kHz that might be present due to interference from other signals and testing equipment, or on the chip.

2.2 Basic Operation

Based on the specifications for the project a fourth-order Butterworth filter design was chosen because Butterworth filters do not ripple in the pass band or stop band as other filters tend to have. The magnitude of the transfer function for a Butterworth filter is

\[ |H(j\omega)| = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_c}\right)^{2n}}} \]  \hspace{1cm} (2.1)

where \( n \) is the order of the filter and \( \omega_c \) is the cutoff frequency. By definition, the cutoff frequency is where the magnitude experiences a 3 dB drop off or where

\[ |H(j\omega)| = \frac{1}{\sqrt{2}} \]  \hspace{1cm} (2.2)

The important aspects of this type of filter are shown in Figure 2.1 where it is shown that the filter does not ripple in the pass band or stop band as other filters tend to, and that the larger \( n \), the sharper the cutoff.
Figure 2.1: Important aspects of a Butterworth filter

A Butterworth filter contains only poles in its transfer function which can be written as

\[ H(s) = \frac{1}{S^n + a_n S^{n-1} + \ldots + a_1 S + 1} \] (2.3)

In designing the low pass filter for this project, an \( n \) of four was chosen because it yields acceptable stop band roll off while keeping size to a reasonable area. The next step is to use this transfer function and to implement a real circuit. From [3] the circuit for a 2nd order Butterworth filter is shown in Figure 2.2.

Figure 2.2: A 2nd order Butterworth low pass filter

Assuming that the operational amplifier is ideal, the transfer function for Figure 2.2 can be found as shown in Appendix A and given by:
After determining the transfer function for a 2\textsuperscript{nd} order Butterworth the transfer function for a 4\textsuperscript{th} Order Butterworth can be obtained by cascading two 2\textsuperscript{nd} order filters together as shown in Figure 2.3.

\[ V_o = \left( \frac{G_1 G_3}{s^2 C_2 C_4 + s C_4 (G_1 + G_3) + C_4 G_3} \right) V_{IN} \quad (2.4) \]

The resulting transfer function for a 4\textsuperscript{th} order Butterworth low pass filter then can be written as a cascade of two 2\textsuperscript{nd} order Butterworth transfer functions

\[ V_o = \left( \frac{G_1 G_3}{G_1 G_4 + G_1 G_3 + G_3 G_4 + G_4 G_4} \right) \left( \frac{G_5 G_7}{G_5 G_8 + G_5 G_7 + G_7 G_8 + G_8 G_8} \right) V_{IN} \quad (2.5) \]

\[ G_1 = \frac{1}{R} \quad G_2 = s C_2 \quad G_3 = \frac{1}{R} \quad G_4 = s C_4 \]

\[ G_5 = \frac{1}{R} \quad G_6 = s C_6 \quad G_7 = \frac{1}{R} \quad G_8 = s C_8 \quad (2.6) \]

\[ V_o = \left( \frac{G_1 G_3}{s^2 C_2 C_4 + s C_4 (G_1 + G_3) + C_4 G_3} \right) \left( \frac{G_5 G_7}{s^2 C_6 C_8 + s C_8 (G_5 + G_7) + C_8 G_7} \right) V_{IN} \quad (2.7) \]
Using Table 1(a) in "A Basic Introduction to Filters- Active, Passive, and Switched-Capacitor" by Kerry Lacanette the denominator coefficients of equation 2.3 of \( n \) equal to four are found to be [4]:

\[
a_0 = 1 \quad a_1 = 2.613126 \quad a_2 = 3.414214 \quad a_3 = 2.613126
\]  

(2.8)

Finally, this determines the final transfer function to be

\[
H(s) = \frac{1}{s^4 + 2.613126 \cdot s^3 + 3.414214 \cdot s^2 + 2.613126 \cdot s + 1} \tag{2.9}
\]

which can be separated into two 2\textsuperscript{nd} order Butterworth transfer functions given as

\[
H(s) = \left( \frac{1}{s^2 + 0.765367 \cdot s + 1} \right) \left( \frac{1}{s^2 + 1.847765 \cdot s + 1} \right) \tag{2.10}
\]

Using the transfer function from 2.5 above the following can be determined from equation 2.9.

\[
\therefore \quad G_1 G_3 = 1 \quad G_5 G_7 = 1
\]  

(2.11)

\[
\therefore \quad C_2 C_4 = 1 \quad C_6 C_8 = 1
\]  

(2.12)

\[
\therefore \quad 2C_4 = 0.765367 \quad 2C_8 = 1.847765
\]  

(2.13)

Knowing 2.10 - 2.12 the components of the 4\textsuperscript{th} order low pass Butterworth can be chosen.
The normalized component values that create a 4th order low pass Butterworth filter with a cutoff frequency of 1 rad/s are shown in Table 2.1. To change the circuit's frequency response, the ratio of reactances to resistances must be maintained at a different frequency. For a roll-off of 10 kHz rather than 1 rad/s, the capacitor values must be scaled using the frequency scaling concept shown below. As this shows, the capacitor's reactance does not reach the original (normalized) value until the higher frequency.

Table 2.1: Normalized component values of a 4th order Butterworth low pass filter

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>R₁</td>
<td>1 Ω</td>
</tr>
<tr>
<td>R₂</td>
<td>1 Ω</td>
</tr>
<tr>
<td>R₅</td>
<td>1 Ω</td>
</tr>
<tr>
<td>R₇</td>
<td>1 Ω</td>
</tr>
<tr>
<td>C₂</td>
<td>2.61313 F</td>
</tr>
<tr>
<td>C₄</td>
<td>0.38268 F</td>
</tr>
</tbody>
</table>
Table 2.1 (continued)

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_6$</td>
<td>1.08239 F</td>
</tr>
<tr>
<td>$C_8$</td>
<td>0.92388 F</td>
</tr>
</tbody>
</table>

2.2 Frequency Scaling

Frequency scaling is the process by which a filter’s frequency characteristic is changed by changing the reactive component values of the original filter. In order to change the frequency characteristic, the original ratio of reactances to resistances must be maintained at the different frequency. This is accomplished through the use of a frequency scaling factor or FSF. Equations 2.21 – 2.27 shows how the components value for a filter with a roll off of 1 rad/s are changed to give a filter with a roll off of 10 kHz.

\[
FSF = \frac{F_{\text{NEW}}}{F_{\text{OLD}}} \tag{2.21}
\]

\[
R' = R \tag{2.22}
\]

\[
C' = \frac{C}{FSF} \tag{2.23}
\]

\[
FSF = \frac{2\pi(10 \text{ kHz})}{1 \text{ rad/s}} = 62831.85307 \tag{2.24}
\]

\[
\frac{C_2}{FSF} = \frac{2.61313}{62831.85307} = 4.15893E-05 \tag{2.25}
\]

\[
\frac{C_4}{FSF} = \frac{0.38268}{62831.85307} = 6.09054E-06 \tag{2.26}
\]

\[
\frac{C_6}{FSF} = \frac{1.08239}{62831.85307} = 1.72268E-05 \tag{2.27}
\]

\[
\frac{C_8}{FSF} = \frac{0.92388}{62831.85307} = 1.4704E-05 \tag{2.28}
\]
Thus a 4th order low pass Butterworth filter with a 10 kHz cutoff frequency has the components values shown in Table 2.2. However, the capacitor component values are not easily realized on chip without using a lot of area. In order to keep the capacitor area small the concept of impedance scaling is used. This means that the resistor values will be increased to decrease capacitance values, maintaining the ratio of reactances to resistances. Capacitors of picofarad values are easily integrable on chip so a new resistance of 10 MΩ was chosen to produce the appropriate scaling.

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1</td>
<td>1 Ω</td>
</tr>
<tr>
<td>R2</td>
<td>1 Ω</td>
</tr>
<tr>
<td>R5</td>
<td>1 Ω</td>
</tr>
<tr>
<td>R7</td>
<td>1 Ω</td>
</tr>
<tr>
<td>C2</td>
<td>4.1589E-05 F</td>
</tr>
<tr>
<td>C4</td>
<td>6.0905E-06 F</td>
</tr>
<tr>
<td>C6</td>
<td>1.7226E-05 F</td>
</tr>
<tr>
<td>C8</td>
<td>1.4704E-05 F</td>
</tr>
</tbody>
</table>

2.3 Impedance Scaling

Impedance scaling is the process by which a filter’s frequency characteristic is kept the same but the component values of the original filter are changed. Sometimes when designing filters, final component values of resistor elements and capacitor elements are not easily found so impedance scaling is used to obtain different component values. In order to change component values, but not change the frequency characteristic, the original ratio of reactance to resistances must be maintained.
This is accomplished through the use of an impedance scaling factor or ZSF. Equations 2.28 – 2.36 shows how the components value giving in Table 2.2 for a filter are changed to values more easily realized on chip.

\[
ZSF = \frac{Z_{\text{NEW}}}{Z_{\text{OLD}}} \\
R' = R \cdot ZSF \\
C' = \frac{C}{ZSF} \\
ZSF = \frac{10 \ \text{MΩ}}{1 \ \text{Ω}} = 10^6 \\
R' = 1 \cdot 10^6 = 10^6 \\
C_2' = \frac{C_2}{ZSF} = \frac{4.15893 \times 10^{-5}}{10^6} = 4.15893 \text{ pF} \\
C_4' = \frac{C_4}{ZSF} = \frac{6.09054 \times 10^{-6}}{10^6} = 0.609054 \text{ pF} \\
C_6' = \frac{C_6}{ZSF} = \frac{1.72268 \times 10^{-5}}{10^6} = 1.72268 \text{ pF} \\
C_8' = \frac{C_8}{ZSF} = \frac{1.4704 \times 10^{-5}}{10^6} = 1.4704 \text{ pF}
\]
2.4 Final Components and Realization

After frequency scaling and impedance scaling the final component values for the 4th order low pass Butterworth filter are the following:

Table 2.3: Final component values of the low pass filter with a 10 kHz cutoff

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_1 = R_2 = R_5 = R_7$</td>
<td>10 MΩ</td>
</tr>
<tr>
<td>$C_2$</td>
<td>4.15893 pF</td>
</tr>
<tr>
<td>$C_4$</td>
<td>0.609054 pF</td>
</tr>
<tr>
<td>$C_6$</td>
<td>1.72268 pF</td>
</tr>
<tr>
<td>$C_8$</td>
<td>1.4704 pF</td>
</tr>
</tbody>
</table>

2.5 Switch-Capacitor Resistor

To implement a 10 MΩ resistor on chip requires a lot of area. Not only due the resistors take up large area, but they are also highly non-linear and have tolerances that are undesirable. In order to implement the four 10 MΩ resistors on chip required by the low pass filter the properties of a resistor need to be simulated. To do this all that is needed are a couple of transmission gates and a capacitor both which are easily realized on chip to form a switch-capacitor circuit. In the switched-capacitor circuit shown in Figure 2.4, the transmission gates $T_1$ and $T_2$ are alternately closed.

![Figure 2.4: A switched-capacitor circuit](image)
As a result the capacitor is charged alternately to $V_1$ and $V_2$. Now, in order to change
the capacitors voltage from $V_1$ to $V_2$, a charge (coulomb) must flow from the capacitor
according to equation 2.37.

$$\Delta q = \Delta V \cdot C = (V_2 - V_1) \cdot C \quad (2.37)$$

The same charge flows through $T_1$ and $T_2$ in sharp pulses each time one of the
switches is closed. If these switches are opened and closed at a regular time interval $\Delta t$ an
average current flows. This average current can be defined by the charged moved $\Delta q$
divided by the time interval $\Delta t$.

$$i = \frac{\Delta q}{\Delta t} = \frac{(V_2 - V_1) \cdot C}{\Delta t} \quad (2.38)$$

Comparing this equation to ohms law

$$i = \frac{V_2 - V_1}{R} \quad (2.39)$$

allows a simulated resistance to be deduced given by:

$$R = \frac{\Delta t}{C} \quad (2.40)$$

Thus switching the voltage across the capacitor moves a charge proportional to the
voltage difference allowing a resistor to be formed with components that are easily
realized on chip.
3 SHIFT REGISTER

3.1 Introduction

The shift register is used to provide the appropriate digital signals to the decoders of the potentiometer and digital-to-analog converter so that only two serial signal wires have to be used instead of sixty four parallel signal wires. The control bits do not need to be kept constant when the power is turned off so a basic flip-flop circuit can be used to store bits.

3.2 Flip-flops

A flip-flop circuit has two outputs, one for the normal value and one for the complement value of the stored bit. Binary information can enter a flip-flop in a variety of ways and gives rise to different types of flip-flops.

3.2.1 Basic Flip-flop Circuit

A flip-flop circuit can be constructed from two NOR gates or two NAND gates which are shown in Figure 3.1 and Figure 3.2 respectively. Each flip-flop has two outputs, Q and Q', and two inputs, set and reset. The outputs Q and Q' are complements of each other and are referred to as the normal and complement outputs, respectively. This type of flip-flop is referred to as an SR flip-flop or SR latch. The flip-flop in Figure 3.1 has two useful states. When Q = ‘1’ and Q' = ‘0’, it is in the set state and then when Q = ‘0’ and Q' = ‘1’, it is in the reset state. The binary state of the flip-flop is taken to be the value of the normal output. When a ‘1’ is applied to both the set and reset inputs of the flip-flop in Figure 3.1, both Q and Q' outputs go to ‘0’. This condition violates the fact that both outputs are complements of each other. In normal operation this condition must be avoided by making sure that ‘1’s are not applied to both inputs simultaneously.
3.2.2 Edge triggered flip-flop

Another type of flip-flop is an edge-triggered flip-flop. In an edge-triggered flip-flop when the clock pulse input exceeds a specific threshold level, the inputs are locked out and the flip-flop is not affected by further changes in the inputs until the clock pulse returns to ‘0’ and another pulse occurs. Some edge-triggered flip-flops cause a transition on the positive edge of the clock pulse (positive-edge-triggered), and others on the negative edge of the pulse (negative-edge-triggered). The logic diagram of a D-type positive-edge-triggered flip-flop is shown in Figure 3.3.
3.3 Overall topology

For the shift register, the D-type positive-edge triggered flip-flop in Figure 3.3 was chosen because the flip-flop is not affected by further changes in the inputs until the clock pulse returns to '0'. Due to the fact that each gain amplifier requires eight bits of control for its DAC and eight bits of control for its potentiometer the shift register was designed in blocks of eight flip-flops as shown in Figure 3.4.
As shown in Figure 3.4 the output Q of each D-type positive-edge triggered flip-flop is tied to the D-input of the next flip-flop. This connection between the output Q and the input D also becomes the output pin for each of the eight different control bits. On the positive-edge of the clock, data is set on the output Q or b₀ of the shift register while the previous indeterminate value on b₀ is shifted into the next flip-flop. On the next positive-edge of the clock the data in flip-flop number one is shifted into flip-flop number two and outputted at b₂ while new data is shifted in and outputted on b₀. This procedure repeats until the eight bits needed for control are shifted through to the appropriate output.
4 GAIN AMPLIFIER

4.1 Introduction

One of the major requirements for the digital signal processing system is to have the ability to amplify the signal from the eddy current probe. Depending on the size of the crack, the amount of amplification required varies leading to the design of a variable gain amplifier. At the same time, because the offset voltage of the eddy current probe signal changes, the gain amplifier also has to have the ability to add variable DC bias to the input signal to center its output voltage signal at the center of the full power supply voltage range available.

4.2 Basic operation

In order to create a variable gain amplifier, four basic building blocks are needed consisting of a potentiometer, operational amplifier, digital-to-analog converter, and shift register. The potentiometer and operational amplifier are used to create the variable gain required by the project while the digital-to-analog converter is used to adjust the offset voltage of the eddy current probe signal by providing different DC bias voltages. The shift register is used to provide the appropriate digital signals to the decoders of the potentiometer and digital-to-analog converter so that only two serial signal wires have to be used instead of sixty-four parallel signal wires for control. To amplify the eddy current probe signal, the operational amplifier is placed in an inverting configuration as shown in Figure 4.1.
The gain of the amplifier is given by [5] as

\[ A_v = \frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1} \quad (4.1) \]

To ensure that cracks of various sizes can be detected, the gain of the amplifier needs to be adjustable from a gain of one to a gain of two hundred and fifty-six. If the resistance of \( R_1 \) is kept constant at a value of 1 kΩ then the resistance of \( R_2 \) needs to be adjustable from a resistance of 1 kΩ to a resistance of 256 kΩ. The requirement of \( R_2 \) to vary from a resistance of 1 kΩ to a resistance of 256 kΩ leads to the use of a potentiometer. A potentiometer is an electronic component which has a user-adjustable resistance. Usually, this is a three-terminal resistor with a sliding contact in the center [6]. The potentiometer replaces the feedback resistor \( R_2 \) in Figure 4.1 as shown in Figure 4.2 creating a variable gain amplifier which has an adjustable gain from one to two hundred and fifty-six.
In order to adjust the offset voltage of the eddy current probe, the voltage output of the digital-to-analog converter is tied into the positive terminal of the operational amplifier as shown in Figure 4.3.

When the digital-to-analog converter is tied to the positive terminal of the inverting operational amplifier configuration the voltage, input to voltage output relationship changes according to the following equation:

$$V_{out} = \frac{R_2}{R_1} (V_{IN} - V_{DAC}) + V_{DAC}$$  \hspace{1cm} (4.2)$$

which is derived in Appendix B.
The last consideration of the inverting configuration of the gain amplifier is making sure that the negative input is biased properly at 1.65 V. In order to achieve 1.65 V at the negative input of the operational amplifier, a resistor divider between the supply voltage rails is set up using two 10 kΩ resistors. The voltage of 1.65 V is then fed into the negative terminal of the operational amplifier through a 1 kΩ resistor that is in parallel with the 1 kΩ resistor that feeds in the input signal resulting in the circuit shown in Figure 4.4.

![Gain amplifier circuit](image)

Figure 4.4: Gain amplifier circuit

When the digital-to-analog converter is tied to the positive terminal of the operational amplifier the addition of a DC bias voltage to the negative terminal causes the voltage input to voltage output relationship to change to

\[
V_{out} = -\frac{R_2}{R_1}(V_{IN} + 1.65 - 2V_{DAC}) + V_{DAC}
\]  

(4.3)
which is derived in Appendix C. Depending on the values of $V_{IN}$, $R_2$ and $V_{DAC}$, the output voltage can be adjusted up and down to achieve the desired center voltage at 1.65 V on the output of the gain amplifier with the appropriate gain needed. The last component of the gain amplifier is the shift register. Two 8-bit shift registers are used to covert the serial digital control provided from an external source to sixteen parallel digital control signals. The first eight of the signals are used to control the tap position of the potentiometer while the last eight are used to control the output voltage of the digital-to-analog converter.
5 POTENTIOMETER

5.1 Introduction

A potentiometer is an electronic component which has a user-adjustable resistance. Usually, this resistance is created by a three-terminal resistor with a sliding contact in the center which is referred to as the tap point [6]. Since the potentiometer is a three-terminal resistor with sliding contact it allows the resistance of the feedback resistor in the inverting operation amplifier configuration to change thus providing the variable gain needed to appropriately detect interruptions in the eddy current for small and big cracks.

5.2 Basic operation

Since the gain of the operational amplifier needs to be adjustable from a gain of one to a gain of two hundred and fifty-six, the potentiometer was designed to have two hundred and fifty-six tap positions. The two hundred and fifty-six tap positions are implemented through the use of two hundred and fifty-six transmission gates and two hundred and fifty-six resistors. Each of the two hundred and fifty-six transmission gates is fed a control signal from a decoder which only turns on one transmission gate and turns off all the other transmission gates. The transmission gate that is turned on creates a resistance path from the terminal that is connected to the negative terminal of the operational amplifier to the terminal of the potentiometer that is connected to the output of the operational amplifier. The third terminal of the potentiometer is connected to ground. All of the other transmission gates are turned off presenting an open circuit which does not allow current to flow. This allows the control of the tap position that is connected to the output of the operational amplifier which in turns allows for the resistance of the feedback path to vary from 1 kΩ to 256 kΩ producing the desired gains.
5.2.1 Transmission gate

A transmission gate is an electronic element made by the parallel combination of transistors with the input at the gate of one transistor (NMOS) being complementary to the input at the gate of the other (PMOS) as shown in Figure 5.1. Current can flow through this element in either direction. Depending on whether or not there is voltage on the gate of the transistors the input to output is either a low-resistance path or a high-resistance path. When the gate input to the NMOS transistor is '0', and the complementary gate input to the PMOS transistor is '1', both transistors are turned off resulting typically in a resistance of greater than 5 MΩ. However when the gate input to the NMOS transistor is '1' and its complementary gate input to the PMOS transistor is '0', both transistors are turned on resulting in a typical resistance of 100 Ω that passes any signal '1' or '0' equally well without any signal degradation [7].

![Figure 5.1: A transmission gate](image)

In order to minimize the area of the potentiometer, each transmission gate was designed to have a conducting resistance of 500 Ω. The resistance of an individual transistor, assuming it is in the non-saturation region, is given by [8].

\[ r_{on} = \frac{1}{\frac{\partial i_D}{\partial V_{DS}}} = \frac{L}{\mu C_{ox} W (V_{GS} - V_T - V_{DS})} \] (5.1)
According to equation 5.1, the conducting resistance of a transistor is inversely proportional to the width of the transistor. By designing the conducting resistance of the transmission gate to be 500 Ω the width of the transistors is reduced, thus the total area of the transmission gate is kept small.

### 5.2.2 Resistor string

The resistor string consists of one 500 Ω resistor and two hundred and fifty-five 1 kΩ resistors in series. The first resistor is designed to be 500 Ω because the transmission gate at each tap point is sized to have a conducting resistance of 500 Ω. The resistance of R₁ in Figure 4.1 was designed to be 1 kΩ. In order to achieve a gain of one to two hundred and fifty-six, the resistance of R₂ needs to be increased in increments of 1 kΩ. The path of resistance that the signal at each tap point travels, is through the resistor and then the transmission gate. For the first tap point, since the transmission gate is 500 Ω, the first resistor only needs to be 500 Ω in value to achieve a total resistance of 1 kΩ. For the second tap point, the total resistance needs to be 2 kΩ to achieve a gain of two. The signal through the feedback path goes through the 500 Ω resistor, then through a 1 kΩ resistor and then, finally, through a 500 Ω transmission gate which equals a total resistance of 2 kΩ. This is why the first resistor is designed to be 500 Ω and the rest of the resistors are 1 kΩ.
5.2.3 Potentiometer decoder

In order to control the tap position of the potentiometer, the control signal that is fed to each of the two hundred and fifty-six transmission gates has to be produced. Since it is not practical to use two hundred and fifty-six parallel control signals to produce the required signals, an 8-to-256 decoder was designed. This decoder, shown in Appendix D, allows the potentiometer tap position to be controlled from the eight bits that it is fed from the shift register. The decoder is made from one 4-to-16 decoder which is described in Appendix E and sixteen 4-to-16 enabled decoders described in Appendix F. The lower 4-bits of the potentiometer decoder are fed directly into the first 4-bits of each 4-to-16 enabled decoder, while the upper 4-bits of the potentiometer decoder are fed into the 4-to-16 decoder. The 4-to-16 decoder decodes the upper 4-bits into sixteen different signals, which of fifteen are ‘0’ and one is ‘1’. Each of these sixteen signals then are tied to the enable input of a different 4-to-16 enabled decoder. The one 4-to-16 enabled decoder that receives a ‘1’ at its enable input in then allowed to decode the lower 4-bits which were directly tied to it into sixteen different signals, which of fifteen are ‘0’ and one is ‘1’. The remaining fifteen 4-to-16 enabled decoders receive a ‘0’ at their enable input which causes sixteen ‘0s’ to be produced. This means that the eight control bits of the potentiometer are decoded into two hundred and fifty-five ‘0s’ and one ‘1’ which turns on one transmission gate, or tap position of the potentiometer.
6 OPERATIONAL AMPLIFIER

6.1 Introduction

To provide proper variable amplification to detect interruptions in the eddy current an inverting operational amplifier configuration with a variable feedback resistance was chosen. In order to use this configuration, an operational amplifier with significant open loop gain and frequency bandwidth is needed. This section describes the design of the operational amplifier used in the gain amplifier architecture.

6.2 Input stage

Over the last several years, due to the lowering of supply voltages, a number of rail-to-rail architectures have been proposed. In each of these rail-to-rail architectures, the key problem in designing an amplifier lies in designing an input stage that maintains constant transconductance ($g_m$) throughout the rail-to-rail input common mode range so that the unity-gain bandwidth, phase margin, and slew rate of the amplifier are kept constant. In this research, an input stage with rail-to-rail common mode range and constant transconductance was designed entirely out of CMOS transistors. This input stage was based upon a novel input stage architecture reported in “Design of a Silicon ASIC Chip for Crystal Oscillator Oven Circuitry” by Vijaya Rentala [9]. The two PMOS differential pairs M0-M3 shown in Figure 6.1 are used to achieve rail-to-rail input common mode range by conducting in two different voltage ranges.
The differential pair, $M_2$ and $M_3$, conducts only for a limited range of the input common mode voltage range that is close to the positive rail while the differential pair $M_0$ and $M_1$ conducts for most of the input common mode voltage range. To hold the transconductance constant through both ranges of operation, constant current is maintained through the use of a current switch $M_5$ whose range of operation is set by a voltage bias named $V_{\text{control}}$. When the input common mode voltage is near the positive rail, the tail current $I_{\text{tail}}$ is steered through the differential pair, $M_2$ and $M_3$, by shifting up the input common mode voltage to a higher value to make the differential pair active. The level shifter ($M_6$-$M_9$) is used for this purpose. In order to determine the correct amount of voltage shift needed for the input common mode voltage, the gate-to-source voltage ($V_{GS}$) of $M_6$ and $M_7$ has to satisfy the following condition:

$$V_{GS} \geq V_{Th\_M2} + V_{DSat\_M5} + V_{DSat\_M4}$$  \hspace{1cm} (6.1)
The input common mode voltage that turns on both differential pairs is set by $V_{\text{control}}$, which has a maximum value equal to $V_{\text{DD}} - V_{\text{Th,M4}} + V_{\text{DSsat,M4}}$. At this common mode voltage, the gate voltages of $M_2$ and $M_3$ are equal to $V_{\text{Th,M4}} + V_{\text{DSsat,M4}} + V_{\text{Th,M2}} + V_{\text{DSsat,M5}} + V_{\text{DSsat,M4}}$. $V_{\text{Th,M4}} + V_{\text{DSsat,M4}}$ is included in the gate voltage of $M_2$ and $M_3$ because the level shifters $M_6$-$M_9$ shift the gate voltage down by the amount of $V_{\text{Th,M4}} + V_{\text{DSsat,M4}}$ allowing $M_2$ and $M_3$ to conduct current near the $V_{\text{DD}}$ rail thus creating a constant $g_m$. Since $M_8$ and $M_9$ have to remain in saturation, the minimum supply voltage can be determined as

$$V_{\text{DD min}} = |V_{\text{Th,M0}}| + V_{\text{DSsat,M4}} + |V_{\text{Th,M2}}| + |V_{\text{DSsat,M5}}| + V_{\text{DSsat,M4}} + V_{\text{DSsat,N18}}$$  \hspace{1cm} (6.2)

For typical values of $V_{\text{Th}}$ (0.5 V) and $V_{\text{DSsat}}$ (0.2 V) a minimum supply voltage of about 1.8 V can be achieved which is well below the process supply voltage of 3.3 V. To operate the circuit with a supply voltage of 3.3 V and not be sensitive to process variation $V_{\text{control}}$ is required to track changes in the supply voltage and temperature. In order to track changes in the supply voltage and temperature the biasing stage in Figure 4.2 was designed. Using the 40 μA current source reference explained in section 6, two current mirror structures ($M_{14}$ - $M_{16}$) were implemented. Transistor $M_{16}$ is used to bias the gate voltage of level shifter transistors $M_6$ and $M_7$ in Figure 6.1. At the same time transistors, $M_{14}$ - $M_{15}$ are used to bias the tail current transistor $M_4$ in Figure 4.1 and to provide the current to bias $V_{\text{control}}$. Transistors $M_{12}$ and $M_{10}$ - $M_{11}$ are diode connected transistors sized to provide a 2 V drop on the gate of $M_{12}$ or to set $V_{\text{control}}$ equal to 2 V. By using the diode connected transistors, $V_{\text{control}}$ will change in the same direction as the threshold voltages of the input transistors keeping the voltage required to turn on transistor switch $M_5$ in Figure 6.1 at the appropriate value.
6.3 Folded cascode stage

The folded cascode stage with the input stage forms a single stage folded cascode operational amplifier. The basic idea of the folded cascode stage is to apply cascode transistors to the input differential pair using transistors opposite in type from those used in the input stage. This allows the output of the input and cascode stage to be at the same bias-voltage levels as the input signals. Using the folded cascode stage shown in Figure 6.3 provides a very high gain due to its high output impedance even though it is a single stage amplifier.
In order to provide high output impedance, transistors M₁₉ - M₂₄ were sized to conduct 43 μA while M₁₇ - M₁₈ were sized to conduct 66 μA. M₁₇ - M₁₈ are sized to handle 23 μA more current because the input stage provides 23 μA on top of the 43 μA biasing of the rest of the cascode stage to these two transistors. Given Equation 6.4, below the width / length ratio of the transistors can be determined assuming various $V_{GS}$, $V_{DS}$ and $V_{Th}$ values. Table 6.1 shows the $V_{GS}$, $V_{DS}$, $I_{DS}$, and the width / length ratios of all of the transistors in the folded cascode stage.

\[
I_{DS} = \frac{\mu_n C_{ox} W}{2L} \left( V_{gs} - V_{Th} \right)^2 \left( 1 + \lambda \cdot V_{DS} \right)
\]  \hspace{1cm} (6.3)

\[
\frac{W}{L} = \frac{2I_{DS}}{\mu_n C_{ox} \left( V_{gs} - V_{Th} \right)^2 \left( 1 + \lambda \cdot V_{DS} \right)}
\]  \hspace{1cm} (6.4)
Table 6.1: Folded cascode transistor parameters

<table>
<thead>
<tr>
<th>Transistor</th>
<th>$I_{DS} \ (\mu A)$</th>
<th>$V_{GS} \ (V)$</th>
<th>$V_{DS} \ (V)$</th>
<th>$V_{TH} \ (V)$</th>
<th>Width (µM)</th>
<th>Length (µM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_{17}$</td>
<td>66</td>
<td>0.9223</td>
<td>0.1057</td>
<td>0.8087</td>
<td>26.4</td>
<td>0.7</td>
</tr>
<tr>
<td>$M_{18}$</td>
<td>66</td>
<td>0.9223</td>
<td>0.1057</td>
<td>0.8087</td>
<td>26.4</td>
<td>0.7</td>
</tr>
<tr>
<td>$M_{19}$</td>
<td>43.6</td>
<td>0.9253</td>
<td>0.8167</td>
<td>0.8579</td>
<td>26.4</td>
<td>0.7</td>
</tr>
<tr>
<td>$M_{20}$</td>
<td>43.6</td>
<td>0.9243</td>
<td>0.8167</td>
<td>0.8579</td>
<td>26.4</td>
<td>0.7</td>
</tr>
<tr>
<td>$M_{21}$</td>
<td>43.6</td>
<td>-0.8531</td>
<td>-0.7152</td>
<td>-0.7574</td>
<td>104</td>
<td>0.7</td>
</tr>
<tr>
<td>$M_{22}$</td>
<td>43.6</td>
<td>-0.8531</td>
<td>-0.7152</td>
<td>-0.7574</td>
<td>104</td>
<td>0.7</td>
</tr>
<tr>
<td>$M_{23}$</td>
<td>43.6</td>
<td>-0.8145</td>
<td>-0.0993</td>
<td>-0.7065</td>
<td>104</td>
<td>0.7</td>
</tr>
<tr>
<td>$M_{24}$</td>
<td>43.6</td>
<td>-0.8145</td>
<td>-0.0993</td>
<td>-0.7065</td>
<td>104</td>
<td>0.7</td>
</tr>
</tbody>
</table>

6.4 Operational amplifier gain

The gain of the operational amplifier is determined by the product of the input transconductance and the output impedance.

$$A_v = g_{m1} \cdot Z_L$$ (6.5)

Here, $g_{m1}$ is the transconductance of transistors $M_0$ and $M_1$ in the input differential pair in Figure 6.1 and $Z_L$ is the impedance to ground on the output node. The output impedance consists of the parallel combination of the output load capacitance, the impedance of any additional circuit stage, and the impedance of transistors $M_{18}$, $M_{20}$, $M_{22}$, and $M_{24}$ [9]. The output impedance $Z_L$ is given by the following [8]:

$$Z_L = \frac{1}{g_{mM_{20}} r_{dsM_{20}} r_{dsM_{11}} || g_{mM_{22}} r_{dsM_{22}} (r_{dsM_{11}} || r_{dsM_{24}})}$$ (6.6)
Knowing that

\[ g_m = \sqrt{\frac{2\mu C_w L}{W} I_D} \]  \hspace{1cm} (6.7)

and that

\[ r_{ds} \equiv \frac{1}{I_D} \lambda \] \hspace{1cm} (6.8)

the output impedance and the gain of the operational amplifier can be calculated using Table 6.1 above. Table 6.2 shows the calculated values for the operational amplifier.

**Table 6.2: Calculated operational amplifier parameters**

<table>
<thead>
<tr>
<th>Transistor</th>
<th>( g_m )</th>
<th>( r_{ds} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>0.000418</td>
<td>4487.464269</td>
</tr>
<tr>
<td>M20</td>
<td>0.001065</td>
<td>2293.141443</td>
</tr>
<tr>
<td>M22</td>
<td>0.000963</td>
<td>2293.141443</td>
</tr>
<tr>
<td>M24</td>
<td>0.000963</td>
<td>2293.141443</td>
</tr>
</tbody>
</table>

**6.5 Frequency response**

The frequency response of the folded cascode operational amplifier is determined primarily by the output pole, which is given as

\[ P_{out} = \frac{-1}{C_{out} / |Z_L|} \] \hspace{1cm} (6.9)
where $C_{\text{out}}$ is all the capacitance connected from the output of the operational amplifier to ground [8]. Since there is only one dominate pole, the gain-bandwidth (GB) of the operational amplifier is given as

$$GB = \frac{g_{\text{ml}}}{C_L}$$  \hspace{1cm} (6.10)

where $C_L$ is approximately 1 pF based on the capacitance of the output pad the operational amplifier is required to drive. Then from the fact that $g_{\text{ml}}$ is equal to 0.000418 from Table 6.2 above the GB of the operational amplifier is calculated as 418 MHz which is more than satisfactory for the gain amplifier.

### 6.6 Class-AB output stage

In order to efficiently use the power supply range, an output stage should combine a high maximum output current with a low quiescent current. To provide a high maximum output current, a class-B biasing output stage can be used. A class-B output stage is biased so that collector current is cut off during one-half of the input signal. When a signal is applied for one half the cycle, the output transistor will be biased on and current will flow. During the other half of the cycle, the output transistor is biased off and the current will be cut off. For class B operation, drain current will flow for approximately 180 degrees (half), of the input signal. [10]. The drawback of class-B biasing is that it introduces a large cross-over distortion. To minimize the distortion, a class-A biasing output stage can be used. Class-A outputs are biased so that variations in input signal polarities occur within the limits of the cutoff and saturation of a transistor. Biasing an output in this manner places the dc operating point between cutoff and saturation and allows drain current to flow during the complete cycle (360 degrees) of the input signal, providing an output which is a replica of the input (Internet Source #1).
To achieve a compromise between distortion and high output current, the output stage needs to be biased between class-A and class-B leading to the solution of a class-AB output stage. Class-AB outputs are biased so that the drain current is cutoff for a portion of one alternation of the input signal. Therefore, current will flow for more than 180 degrees but less than 360 degrees of the input signal. As compared to the class-A amplifier, the dc operating point for the class AB amplifier is closer to cutoff. A classic configuration of a class-AB output stage is shown in Figure 6.4 which consists of two common-source connected output transistors, \( (M_{31} \text{ and } M_{32}) \), that are driven by two-in-phase signal currents, \( I_{in1} \) and \( I_{in2} \).

![Figure 6.4: A classic configuration of a class-AB output stage](image)

The control of the class-AB amplifier is formed by transistors \( M_{25} \) and \( M_{26} \), while the stacked diode transistors of \( M_{29} - M_{30} \text{ and } M_{27} - M_{28} \) bias the gates of the class-AB transistors \( M_{32} \text{ and } M_{31} \) respectively. The floating class-AB control transistors, the stacked diode connected transistors, and the output transistors set up two translinear loops \( M_{26}, M_{27}, M_{28}, M_{31} \text{ and } M_{25}, M_{29}, M_{30}, M_{32} \), which determine the quiescent current in the output transistors [9].
The class-AB action is performed by keeping the voltage between the gates of the output transistors constant. According to the thesis “Design Of A Silicon ASIC Chip For Crystal Oscillator Circuitry” by Vijaya Rentala, if the in-phase signal current sources $I_{in1}$ and $I_{in2}$ are pushed into the class-AB output stage, then the current of $M_{25}$ will increase while the current in $M_{26}$ will decrease by the same amount. This causes the gate voltage of transistors $M_{32}$ and $M_{31}$ to move up causing the output stage to pull current from the output node. This action continues until the current through $M_{25}$ is equal to $I_{b1}$ [9]. When the current of $M_{25}$ is equal to $I_{b1}$ the current of $M_{31}$ is kept at minimum value that is set with the width over length ratio of $M_{26}$ and $M_{25}$ while the current through $M_{32}$ is still allowed to increase. When the input current sources $I_{in1}$ and $I_{in2}$ are pulled instead of pushed from the class-AB output stage, the above can be repeated except that the current in $M_{26}$ will increase while the current in $M_{25}$ will decrease. The major drawback with using the class-AB control is that the quiescent current of $M_{31}$ and $M_{32}$ depends on the voltage supply variations [9]. A voltage supply dependent variation of the quiescent current occurs because the supply voltage variation is directly placed across the output impedance of $M_{25}$ and $M_{26}$ by the gate to source voltages of $M_{31}$ and $M_{32}$ [9].

6.7 Overall design of the operational amplifier

The rail-to-rail input stage, folded cascode stage, and the class-AB output stage have previously been described. In this section, the overall design of the operation amplifier is described. Traditionally, the way to design a two-stage operational amplifier is to place the input stage, folded cascode stage, and the class-AB stage in cascade. However, when this is done two significant drawbacks occur. First, the overall gain of the operational amplifier decreases because the bias currents $I_{b1}$ and $I_{b2}$ are in parallel with the cascode transistors $M_{20}$ and $M_{22}$ of the folded cascode stage. Secondly, the folded cascode transistors $M_{20}$ and $M_{22}$ along with the bias currents of the class-AB control $M_{25}$ and $M_{26}$, contribute to the noise and offset of the amplifier [9].
A way to reduce the noise and offset effect of the bias currents of the class-AB control transistors is to move them into the folded cascode stage as shown in Appendix G. By shifting the class-AB control transistors into the folded cascode stage, they now are biased by the current of the folded cascode transistors instead of the bias currents $I_{b1}$ and $I_{b2}$, eliminating the noise and offset caused by them. The last concern of the operational amplifier is due to the addition of the class-AB output stage creating a situation where there is no longer one dominate pole presented by the folded cascode stage. To overcome this, the operational amplifier is compensated using the conventional Miller compensation technique. The capacitors $C_{M1}$ and $C_{M2}$ around the output transistors $M_{31}$ and $M_{32}$ in Appendix G split apart the poles of the operational amplifier, ensuring a 20 dB per decade roll off of the amplitude. The Miller compensation technique adjusts the output pole to a frequency given by [9]:

$$w_{out} = \frac{g_{m-out}}{C_L}$$  \hspace{1cm} (6.11)

where $g_{m-out}$ is the transconductance of the output transistors and $C_L$ is the capacitance of the load [9].
7 DIGITAL-TO-ANALOG CONVERTER

7.1 Introduction

One of the most important functions in signal processing is the conversion between analog and digital signals and vice versa. The conversion between analog and digital signals is accomplished through the use of either an analog-to-digital converter (ADC) or a digital-to-analog converter (DAC). For the gain amplifier discussed above the design of a DAC was required to provide an analog voltage for centering of the eddy current probe signal in the middle of the voltage supply range. A DAC with a voltage output can be characterized by the block diagram in Figure 7.1. In this block diagram \( b_0 - b_{N-1} \) are digital ‘1’ s or ‘0’ s provided by an external reference and \( V_{out} \) is the analog voltage that varies depending on the digital signal. Typically the following holds true for a DAC.

\[
V_{OUT} = K \cdot V_{REF} \cdot D
\]

(7.1)

\[
D = \frac{b_0}{2^1} + \frac{b_1}{2^2} + \frac{b_2}{2^3} + \cdots + \frac{b_{N-1}}{2^N}
\]

(7.2)

where \( K \) is some scaling factor and \( V_{REF} \) is the reference voltage desired at \( V_{out} \) when \( b_0 - b_{N-1} \) are all digital ‘1’ s.

![Figure 7.1: Block diagram of a DAC](image)
7.2 Digital-to-Analog converter structures

Since one of the most important functions in signal processing is the conversion between analog and digital signals and vice versa, several different DAC architectures have been developed over the years. Each of these architectures has its advantages and disadvantages which had to be considered for the design of the DAC for the gain amplifier.

7.2.1 Binary-weighted resistor DAC

In Figure 7.2, the basic architecture for a binary-weighted resistor DAC is shown. The key advantages to this architecture is that it is insensitive to parasitic capacitance and it is fast which makes it desirable for use in the gain amplifier. However, it requires a large spread in resistor values and lots of chip area which can lead to poor matching between the various resistors. Therefore, if the number of bits of the DAC is large, precision resistors or trimming would be required to achieve the degree of accuracy needed for the gain amplifier [11].

Figure 7.2: A binary weighted DAC implementation (4 bit)
7.2.2 R-2R DAC

Another option is the use of an R-2R DAC architecture which is shown in Figure 7.3. The R-2R DAC architecture is typically chosen over the binary-weighted DAC because the R-2R architecture eliminates the large component spread associated with binary-weighted DACs [11].

![Figure 7.3: An R-2R DAC implementation (4 bit)](image)

The resistance seen to the right of any of the vertical 2R resistors is always 2R which causes the current to be reduced by a factor of 2 as the current flows from the left most vertical 2R to the right most vertical 2R thus the current $I_N$ flowing through switch $d_N$ is given by:

$$I_1 = \frac{V_{\text{REF}}}{16R}, \quad I_2 = \frac{V_{\text{REF}}}{8R}, \quad I_3 = \frac{V_{\text{REF}}}{4R}, \quad I_4 = \frac{V_{\text{REF}}}{2R}$$

(7.3)

This current flows into the negative terminal of the operational amplifier which is referred to as the summing node and creates an output voltage given by:
Some of the key advantages and disadvantages of the R-2R DAC are that it is only as accurate as the matching of the resistors. As the number of digital bits increases the reference voltages generated by the resistor string are much closer and the resistor matching requirements are increased. Also R-2R DACs have no load driving ability so if the DAC output has an appreciable current draw, the current is siphoned off of the negative terminal of the operational amplifier because it is non-ideal thus causing the reference voltages to be inaccurate. The fact that the R-2R DAC has no load driving ability makes this architecture undesirable for use in the gain amplifier.

7.2.3 Current Steering Flash DAC

The current steering flash DAC is an architecture that was developed to overcome the no load driving ability of the R-2R DAC. An N bit current steering flash DAC uses N, 2^N, or more matched circuit elements to create N, 2^N, or more reference currents as shown in Figure 7.4.

\[
V_{OUT} = -K \cdot \left( \frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \ldots + \frac{b_{N-1}}{2^N} \right) \cdot V_{REF}
\]  

(7.4)
A major advantage of the current steering flash DAC is its high current drive, high speed, and monotonic output voltage. The disadvantages of the current steering flash DAC is that glitches in the analog output voltage are created when the switches do not operate at the exact same instance, and there is stringent current source matching requirement as the number of digital bits increase. At the same time the current sources have finite output impedance that drive the analog voltage so as the DAC output varies over its full-scale range, different impedances are connected to the output changing the load resistance and introducing non-linearity. If the disadvantages of the current sources can be overcome the current steering flash DAC architecture would fit the requirements needed for use in the gain amplifier.

7.3 Current source structures

Since the current steering flash DAC architecture has stringent current source matching requirements the right current source structure has to be designed. A current sink and current source are components whose current is independent of the voltage across their terminals. In a current sink and current source the current flows from the positive node to the negative node through the sink or source. The major difference between a current sink and current source is that a current sink typically has the negative node at Vss and the current source has the positive node at Vdd. Figure 7.5 shows the NMOS transistor implementation of a current sink.

![Figure 7.5: A NMOS transistor implementation of a current sink](image)
Typically the gate is set at whatever voltage is needed to create the desired value of current and the FET is not operated in the non-saturation region because it does not make a good current source in this region. For the current sink in Figure 7.5 to perform properly

\[ V_{OUT} \geq V_{GG} - V_i \]  

(7.5)

Given Equation 7.5 and that the gate to source voltage of the current sink is held constant the current-voltage characteristic of the current sink can be drawn as shown in Figure 7.6 thus showing why a current sink is not operated in the non-saturation region.

If the source and bulk are connected to the same potential the small-signal output resistance is given by:

\[ r_{out} = \frac{1 + \frac{\lambda V_{DS}}{\lambda I_D}}{\lambda I_D} \approx \frac{1}{\lambda I_D} \]  

(7.6)

As shown in Figure 7.5 a NMOS transistor is used to create a current sink because the source of a NMOS transistor is typically tied to the lowest potential which current sinks too. In order to provide a current source the current needs to flow into the source of a transistor that is connected to the highest potential which is why PMOS transistors are used to implement current sources. Figure 7.7 shows a PMOS transistor implementation of a current source.
Again if the gate to source voltage is held constant the current-voltage characteristic of the current source can be drawn as shown in Figure 7.8.

Like before, the small-signal output resistance of the current source is given by Equation 7.6. The source-drain voltage must be larger than $V_{\text{MIN}}$ in Figure 7.8 for the current source to work properly and only works for values of $V_{\text{OUT}}$ given by:

$$V_{\text{OUT}} \leq V_{\text{GG}} + |V_t|$$  \hspace{1cm} (7.7)

The reason why current sinks and sources of Figures 7.5 and 7.7 are so popular is due to their simplicity. Even though they are simple there are two areas in which their performance may need to be improved for certain applications. One improvement is to increase the small-signal output resistance which results in less current fluctuation over the range of $V_{\text{OUT}}$ values.
The second improvement is to reduce the value of $V_{\text{MIN}}$ allowing a larger range of $V_{\text{OUT}}$ over which the current sink/source works properly. In current steering flash DACs the main concern is to improve the small-signal output resistance to reduce current fluctuation thus improving resolution. One way to implement an improvement in small-signal output resistance is to use the transistor architecture shown in Figure 7.9.

![Figure 7.9: Circuit for increasing $r_{\text{out}}$ of a current sink](image)

Is this architecture, the output resistance ($r_{\text{ds1}}$) of current sink $M_1$ is increased by the common-gate voltage gain of $M_2$ which is shown in Appendix H. The small-signal output resistance of the current sink $M_1$ in Figure 7.9 is increased by a factor of $g_{\text{m2}}r_{\text{ds2}}$.

### 7.4 Overall design

To implement the DAC needed to provide the centering analog voltage to the gain amplifier the current steering flash architecture was chosen due to its high current drive and monotonic characteristic. To overcome the finite output impedance inherent in a current steering flash architecture, it was decided to sum the current into an operational amplifier. By using an operational amplifier the finite output impedance becomes stable and is increased. The question then arises how to combine a current steering DAC architecture with an operational amplifier?
Taking a look at various amplifier configurations and borrowing from the R-2R DAC architecture it was decided to sum the current from the current steering flash architecture through a resistor and then use the amplifier in a non-inverting configuration to produce the required voltage.

### 7.4.1 Current source

The first step in designing the DAC needed for this project was to determine the current source configuration. In this design, glitches are a major limitation in current steering converters. When the digital input values change it is possible that some of the digital control signals may cause the switch controls to conduct, resulting in glitches in the analog output signal values. For example, if the most significant bit, the eighth bit in this design, changes its value faster or slower than all the other bits it is possible to have a glitch that causes the analog output voltage to be off by almost half of the upper voltage rail. This problem can be alleviated by the use of thermometer code representation of the binary digital bits. Figure 6.10 shows the decimal-to-binary-to-thermometer code representation [11].

#### Thermometer code

![Figure 7.10: Thermometer code representation of binary bits](image)

Although this coding scheme can result in potentially more complex circuitry, it has many advantages such as guaranteed monotonicity, reduced glitching noise, and linearity. In a thermometer code, the number of ‘1’s in the converted signal represent the decimal value.
So if the decimal representation of the binary value is a four there will be four '1's present in the thermometer code. In a thermometer code based DAC, the switching network consists of \(2^N-1\) switches that have equal resistances and carry equal amounts of currents. The current through these switches is conditionally directed either into the feedback resistor of an operational amplifier or directly to ground. To minimize complexity and area usage it was decided to binary weight the lower four bits and to thermometer encode the upper four bits of the eight bit DAC. By doing this, most of the glitches associated with switching are eliminated and the mismatch in the current sources is spread out but circuit complexity is reduced. The second step in designing the DAC is to decide on the type of current source to use. To increase the small-signal output resistance of the current source a cascode current structure was decided on thus reducing mismatch errors due to voltage changes. The cascode current source along with the transistor switch was designed to supply 16.15 \(\mu\)A with a voltage drop of 6.5 mV across a sink resistor of 400 \(\Omega\). Next the current source and transistor switch in Figure 7.11 was designed to have a 1.65 V drop from the positive rail of the current source to the sink resistor.

![Circuit Diagram](image)

*Figure 7.11: Circuit of the DAC current source and transistor switch*

By doing this the transistor switch can be sized to keep the resistance down to allow more voltage head room for the cascode current source. The resistance of a transistor in the saturation region is given by:
Along with the increased voltage head room, in order to ensure that there are no major glitches, a dual sink resistor scheme was decided on. In this dual sink resistor scheme two sinking resistors of 400 $\Omega$ were tied to two different switching transistors which were tied to the same current source. These different switching transistors were tied to complementary control signals so that only one switch conducts at a time. One sinking resistor is used as the current summing node into the operational amplifier while the second sinking resistor is directly tied to ground. By using complementing control signals the current source is never sinking into an open circuit thus reducing current source mismatch. The overall circuit implementation of the eight bit DAC is shown in Appendix I.

### 7.4.2 DAC control

The next step in designing the DAC is to implement the control structure for the binary-weighted lower four bits and the thermometer weighted upper four bits. To implement the control structure for the binary weighted lower four bits, all that has to be done is that the control signals $B_0 - B_4$ are complemented and feed through to the appropriate transistor switch. To implement the control structure for the thermometer weighted upper four bits a four-to-sixteen decoder and fifteen OR-gates were used. The main principle behind thermometer code, is that with each increasing binary number there is only one thermometer bit that changes. This logically means that if the upper thermometer bit is a one then all the thermometer bits below it must also be a one. Figure 7.12 shows the circuit implementation of the DAC controller.
The four-to-sixteen decoder converts the four upper bits of the DAC to a digital ‘1’ at one of the sixteen outputs and to a digital ‘0’ at the rest of the outputs. Each of the decoder’s outputs are tied into input A of an OR gate except for output Y15. At the same time input B of each OR gate is tied to the Y output of the OR gate above it allowing a digital one to cascade down through the sixteen control signals. For example if B0 = ‘1’, B1 = ‘1’, B2 = ‘1’, and B3 = ‘1’ then decoder output Y0-Y14 = ‘0’ and Y15 = ‘1’. Y15 is then feed into input A of OR gate 15. Since Y14 = ‘0’ input B of OR gate 15 is ‘0’. Table 7.1 shows the truth table of an OR gate.

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
From the truth table if $A = \text{‘1’}$ and $B = \text{‘0’}$ then $Y = \text{‘1’}$. This ‘1’ is then feed into input $A$ of OR gate 14 whose input $B$ is tied to $Y_{13}$ of the decoder which is ‘0’. Again this produces a ‘1’ at the output of the OR gate. This continues to happen all the way through the rest of the OR gates producing ‘1’s on all the thermometer control bits. Now if $B_0 = \text{‘0’}$, $B_1 = \text{‘1’}$, $B_2 = \text{‘1’}$, and $B_3 = \text{‘1’}$ then $Y_{14} = \text{‘1’}$ and $Y_0$-$Y_{13}$, $Y_{15} = \text{‘0’}$. Therefore input $A = \text{‘0’}$ and input $B = \text{‘0’}$ of OR gate 15 which according to Table 7.1 produces a ‘0’ at the output. For OR gate 14 input $A = \text{‘1’}$ and input $B = \text{‘0’}$ so a ‘1’ is produced at the output which cascades down the rest of the OR gates. So the DAC control structure produces the appropriate thermometer code with just fifteen OR gates and one four-to-sixteen decoder.
8 SYSTEM DESIGN

8.1 Introduction

In the previous chapters the individual components of the digital signal processing (DSP) system were discussed and explained. Each of the components discussed are not novel to the world of electrical engineering, but the way in which the components were designed together is the novelty behind this work. In the design of the DSP system the power consumption, physical layout, and physical considerations were all challenging and new.

8.2 Power consideration

The overall implementation of the digital signal processing system is going to be battery operated so power consumption is a major concern. Since the operational amplifier is used in the low pass filter, digital-to-analog converter, and gain amplifier, its power usage has a major impact on the overall power consumption of the chip. The desire to decrease the power consumption of the operational amplifier leads to an engineering tradeoff. In the design of the gain amplifier the operational amplifier is placed in an inverting feedback configuration. The nature of this feedback configuration requires the operational amplifier to have a certain open loop gain so that finite gain problems do not occur. In the design of the operational amplifier, the amount of current used directly affects the amplifier’s power consumption and open loop gain. If the current of the operational amplifier is increased, the open loop gain of the amplifier is also increased, but the power consumption is also increased. At the same time the bandwidth of the amplifier is decreased due to the larger capacitance of the larger transistors needed to handle the current.
If the current of the operational amplifier is decreased the power consumption and open loop gain is decreased while the bandwidth of the amplifier is increased due to smaller device sizes. In order to achieve a desirable balance between open loop gain, bandwidth, and current an operational amplifier with the architecture described above in chapter 6 was designed with a bias current of 20 µA. After this was done the open loop gain and bandwidth of the amplifier was simulated. Next the amplifier was placed into a test bed schematic as shown in Figure 8.1.

![Gain amplifier test bed schematic](image)

Figure 8.1: Gain amplifier test bed schematic

The purpose of the test bed schematic is to simulate the gain amplifier in its most demanding performance condition. The most demand on the performance of the amplifier is when the input signal has an amplitude of 1/255 V, a frequency of 10 kHz, and a feedback resistance of 255 kΩ. After placing the amplifier in the test bed shown in Figure 8.1 the response of the circuit was simulated. Figure 8.2 shows an example of what the output is expected to look like.
Figure 8.2: Output of the test bed schematic in Figure 8.1

From the simulations of the amplifier, it was estimated that at a frequency of 10 kHz that the operational amplifier needs to have an open loop gain of around 70 dB to function properly. Knowing that an open loop gain of around 70 dB at 10 kHz was required, the amplifier was redesigned with a tail current of 50 μA. After its completion, the simulation of open loop gain and bandwidth showed that at 10 kHz it had around 85 dB of open loop gain and limited bandwidth. Due to the limited bandwidth and the excessive open loop gain at 10 kHz, the amplifier was redesigned to have a tail current of 40 μA to save on power consumption. Figure 8.3 shows the open loop gain and bandwidth of the amplifier with a tail current of 40 μA.
Since the open loop gain at 10 kHz came out to be around 70 dB while the gain bandwidth was around 100 MHz, the tail current of 40 μA design was kept. The total average power consumption of the operational amplifier was determined to be approximately 3.5 mW.

### 8.3 Physical considerations

A circuit defined and functioning properly at the schematic level can fail if it is not physically designed correctly. Physical design of integrated circuits is affected by matching of components, parasitic components, noise, wire resistance, and circuit biasing. This section will focus on physical layout techniques for the design of the entire system as well as the biasing scheme used for the various components.
8.3.1 Physical Layout

The correct layout of the low pass filter, operational amplifier, potentiometer, and DAC circuitry is crucial in having a functional system. There are several areas that must be given adequate attention to have a successful fabricated design. These areas include:

- Routing of critical paths through the placement of cells
- Coupling of sensitive lines
- Design for testability
- Electromigration of metal due to current
- Parasitic capacitance and wire resistance
- Device matching for critical components

Most of these issues can be overcome with the careful placement of the cells and their interconnections through floor planning. Floor planning is the design of the physical aspects of a system taking into account its geometrical limitations. The floor planning and physical design of the digital signaling processing system (DSP) was done in a top down fashion. In Figure 8.4 a block diagram of the floor plan of the DSP system shows the order in which the physical design of the system was completed.

![Block diagram of the floor plan for the DSP system](image)
To begin with, two hundred and fifty six resistors were physically laid out to minimize space in the X-direction. Next the transmission gates of the potentiometer were then physically placed below the resistors in the same X-dimension. The next major component was the 4-to-16 enabled decoder used to control the transmission gates in the potentiometer. In the physical layout of the 4-to-16 enabled decoder, the major consideration in its design was to keep the X-dimension of the decoder the same dimension as sixteen resistors and transmission gates. This allows the sixteen control signals from the decoder to be lined up with the inputs of the sixteen transmission gates. Since there are two hundred and fifty six transmission gates, this allows sixteen enabled decoders to be placed physically close to each in a repetitive manner. In the process of designing the layout of the 4-to-16 enabled decoder it was discovered that there wasn’t enough room to fit the physical X-dimension of sixteen resistors and transmission gates. So after some rearranging, four out of the five 2-to-4 decoders that make up the 4-to-16 enabled decoder fit within the X-dimension of the sixteen resistors and transmission gates. These four 2-to-4 decoders are the ones that the sixteen control signals come from. This meant that the last 2-to-4 decoder needed to placed below and to the left of the other four 2-to-4 enabled decoders creating an L-configuration style layout. This L-configuration leaves a considerable amount of chip area open between the sixteen 4-to-16 enabled decoder layouts.

In order to utilize the open area of the L-configuration of the 2-to-4 enabled decoder, the physical layout of an individual DQ flip flop of the shift register was designed to fit in this area. Even though this helps utilize the empty area, it brings up the concern of excessive delay between flip flops in the shift register. To overcome this, two inverter buffers were placed on the end of the each DQ flip flop in the shift register to drive the signal and minimize delay. The last physical layout of the potentiometer to be designed was the 4-to-16 decoder. Since the 4-to-16 decoder is similar to the 4-to-16 enabled decoder, except for one gate, the layout of the 4-to-16 enabled decoder was reused. However, to save chip area in the Y-dimension the fifth 2-to-4 decoder creating the L-configuration was moved and placed to the left of the other gates in the layout.
Following the physical layout of the potentiometer and its control the operational amplifier was designed next. In the design of the physical layout of the operational amplifier two things were kept in consideration. The first was to minimize area as much as possible because the physical layout of the operational amplifier is used in the implementation of the digital-to-analog converter and low pass filter. The second consideration was the placement of the PMOS and NMOS transistors in relation to the power supply. In order to make sure the transistors have a solid body contact in relation to the power supply the PMOS transistors were grouped together on top of the layout near the Vdd power supply rail, while the NMOS transistors were grouped together on the bottom of the layout near the Gnd power supply rail.

The next component to be physically laid out was the DAC. To minimize process variation and current source mismatch, the layout technique of common centroid was used. Common-centroid layout refers to a layout style in which a set of devices has a common center point. Figure 8.5 shows an example of common-centroid layout [12].

![Common-centroid layout example](image)

Figure 8.5: An example of common-centroid layouts

Common-centroid layout techniques are widely used to create circuits that are process independent with respect to device width and length for transistors and other component values. In the case of the DAC, the current sources and transmission gates were laid out in a horizontal line very similar to the common centroid layout in Figure 8.5. After placing the transistors physically, the wiring to steer the current to the summing resistor was laid out. In the design of the wires of the DAC, electromigration has to be taken into account.
Electromigration is the transport of material caused by the gradual movement of the ions in a conductor due to the momentum transfer between conducting electrons and diffusing metal atoms. Over time this transporting of material causes the metal to thin and open thus the metal path becomes non-conductive, thus making a chip essentially useless. In order to ensure that this doesn't happen, there are rules in the DRC manual that need to be followed that designate the amount of current density per micron width a metal layer can handle before having electromigration occur. After completing the wiring for the DAC, the control logic for the transmission gates was placed to the left of the current source structure and the operation amplifier was placed to the right of the current sources. The only consideration in this choice of design was to minimize chip area and to keep signal wiring as short as possible. The last individual component to be physically laid out was the low pass filter. After designing the individual capacitors for the switch resistor design used in the filter, all that was done to complete the filter layout was to position the capacitors as tightly as possible around the layout of the operational amplifier. In relation to the rest of the DSP layout, both filters were rotated ninety degrees and placed next to the layout of the potentiometer, gain amplifiers, DAC, and shift register. This was done to minimize area in the X-dimension and to keep wiring length short.

After floor planning and layout through the use of the layout vs. schematic (LVS) tool, each physical design is checked against its schematic. After this verification, the critical performance characteristics of the layout, such as wire resistance, transistor size, and capacitance, are extracted. Each component is then simulated using the extracted information. Components that did not meet certain criteria are modified to improve performance. The main causes for degraded performance of a cell are parasitic capacitance, wire resistance, and mismatch being larger than expected. Schematic simulations do not account for the parasitic capacitances unless they are physically put into the schematic view. At the same time, process variations in fabricating circuits on a wafer can account for performance degradation too. Problems arise from device mismatches and variation of widths that change component performance. In each fabrication process, following the design rule check (DRC) manual minimizes all the above problems.
8.4 Design for test

Due to issues with interconnect errors, parasitic components, wire resistance, and process variations associated with systems, the physical layout does not match the schematic exactly. This means, despite all the layout techniques and precautions taken, once the design is sent for fabrication, it is nearly impossible to fix any mistakes that have resulted from layout errors. This is especially problematic if the layout contains no provisions for external test points used to isolate problems. Therefore, in this design, several test points were placed throughout the system so that measuring the performance of the individual components is possible. In this digital signaling processing system there were four main tests to verify system function. These tests focused on the inputs and outputs (I/O) of the low pass filter, digital-to-analog converter (DAC), gain amplifier, and shift register by wiring the I/O to external pins. By having external pins as connections, the individual components can be tested and the entire system still wired together through the used of a milled PCB board. In the case of the low pass filter, the input non-overlapping clock used for the switch capacitor resistors, the signal input to the filter, and the output of the filter were wired to three different external pins. In the case of the gain amplifiers the signal input and DAC offset voltage input to both the first amplifier and the second amplifier were wired to the four different external pins. The reason for this is that the design of the DAC is very sensitive to process variation causing the voltage offset function of the gain amplifier to be in question. By having the DAC output of each gain amplifier wired to an external pin, the functionality of each can be evaluated. If each DAC functions as expected then, it can still be wired to the external pin of the offset voltage input of the gain amplifier. If all, one, or several of the DAC’s don’t function properly, an external voltage source can be wired to the offset voltage input instead allowing the DSP system to still function. For the shift register, the clock input, signal input, and shift register output were wired to a pad pin. This allows the verification of the functionality of the shift register.
By designing the DSP for test, the functionality of the individual components that make up the entire system can be tested and verified. At the same time if issues with interconnect errors, parasitic components, wire resistance, and process variations cause system error, the problem can be narrowed down and isolated. For example, if the low pass filter failed due to interconnect problems at the external pin an off the shelf low pass filter could be used to test the functionality of the entire DSP.

8.5 System biasing

To provide proper bias to all of the circuits, a bias source is needed. Due to the environment in which this chip is going to be used, this source needs to be independent of process variations and temperature fluctuations. This section describes the design of the bias source and how all of the circuits on the chip are biased with it.

8.5.1 Current Biasing Cell

Proper biasing of the internal circuits is critical to the performance and operation of a chip. The bias cell shown in Figure 8.6 is a classic architecture of a current source. In this architecture, the p-type transistors $M_2$ and $M_4$ form a current mirror with a gain of $S_2/S_4$ and the n-type transistors $M_1$ and $M_3$ form a second current mirror with a gain of $S_3/S_1$ where $S_1$, $S_2$, $S_3$, and $S_4$ are the width to length ratios of the transistors.

![Current bias source](image)

**Figure 8.6: Current bias source**
If the resistor is neglected, the two current mirrors become interconnected in a closed loop that has a corresponding gain that is the product of the two individual gains. By design, this loop gain is chosen to be higher than one so that the current in both branches increases until equilibrium is reached, when the gain is reduced to one by the voltage drop across the resistor. If $M_1$ and $M_3$ operate in weak inversion and are in the same p-type well, then $V_{S3} = V_R$ and $V_{G3} = V_{G1}$ by [13]:

$$V_R = U_T \ln \left( \frac{S_3}{S_1} \cdot \frac{S_2}{S_4} \right)$$  \hspace{1cm} (8.1)

where $U_T = kT / q$. The reference current proportional to $V_R / R_{nwell}$ is extracted by the current mirror $M_4$ and $M_5$. The fact that $V_R$ is proportional to $U_T$ and that $U_T = kT / q$ makes this current source a proportional to absolute temperature (PTAT) source. By combining a PTAT with a source that is inversely proportional to absolute temperature, the creation of a current reference that is independent of temperature can be accomplished. The drawback to that type of current reference is the circuitry used to combine the two sources becomes complex and consumes a large amount of chip area. However, the reference current in the PTAT is proportional to $V_R / R_{nwell}$; so through the use of an nwell resistor, which possesses a high temperature coefficient and proper design of the ratio of the width to length ratios of the transistors, the current can be kept constant over temperature. The current bias cell in Figure 8.6 was designed for a 10 µA biasing current in transistors $M_1$-$M_4$ in order to produce a 40 µA biasing current through current mirror transistor $M_5$, which is required to bias the other circuits on the chip. In order to check performance of the bias cell, the circuit was simulated over a temperature range from -40°C to +80°C. For this temperature range, the 40 µA bias current only varied 2.9 µA as shown by Figure 8.7.
8.5.2 Biasing fail safe voltage

The current reference above is required to provide a stable current source independent of temperature, supply voltage and load to the entire system. However, there are several main sources of error that cause a current source to deviate from its nominal value. Examples of such main sources are process tolerances, IR-drop, noise, and/or current mirroring mismatch associated with a chip-wide reference current distribution. Simulations results like that of Figure 8.7, help determine the current source deviation from nominal values but it doesn’t give the designer a precise knowledge of which part of the circuit is more sensitive to process tolerances. This fact combined with the fact that the reference current cell provides bias to the entire system requires the design of a system fail safe voltage. The purpose of the fail safe voltage is to force a voltage at a certain point in the current reference so that the current can be adjusted depending on the system response. To incorporate a system fail safe into the DSP system a test point was designed into the current reference cell at the drain of transistor M5 in Figure 8.6 above.
This fail safe pin for each current source in the DSP system is tied to an external pad pin. This allows a voltage to be forced on the drain of transistor M5 and on any transistor tied to M5. If a voltage is forced at this test point the current response of both transistors M5 and the one tied to it will change allowing adjustments. However, if no voltage is forced on the pin the voltage will bias to its designed value. This way if there are IR drops, noise, and/or current mismatches the operation of the system can still be ensured.
9 MEASUREMENT RESULTS

9.1 Introduction

In order to ensure that the overall digital signal processing circuit for the eddy current probe would work properly the individual blocks of the system were tested separately and characterized.

9.2 Shift Register Results

The primary function of the shift register was to convert a serial sequence of sixty-four control signals to a parallel sequence of sixty-four control signals. To test the performance of the shift register a random sequence of was shifted into the register and out of the register for testing. For example, if a bit pattern of ‘0111’ is shifted into the shift register using four clock cycles after sixty more clock cycles a ‘1’ should be present on the last output of the shift register. If three more clock cycles are pulsed and the voltage on the last output of the shift register captured a pattern of ‘011’ should be seen. In order to capture the pattern a logic analyzer must be used. To test the fabricated shift register, a HP 16500C logic analysis system was used by capturing the clock of the shift register, input of the shift register, and output of the shift register as shown in Figure 9.1.
In Figure 9.1, from top to bottom, the first white line is the captured clock, the second white line is the input to the shift register, and the third white line is the output of the shift register. In this test a bit pattern of ‘00000111000001110000011100000111’ was shifted into the register twice because if the bit pattern is shifted in only once the logic pattern will be only held on the sixty-four parallel outputs so in order to see what pattern is stored, sixty-four more bits have to be shifted in. From Figure 9.1, one can see that the pattern shifted into the shift register matches the pattern shifted out of the register with a slight time mismatch, because the pattern has to be shifted in twice, proving that the shift register works as designed.

### 9.3 Gain amplifier results

The primary function of the gain amplifier is to provide a variable gain from one to two hundred and fifty-six to an input signal with a frequency up to 10 kHz. In order to measure the amount of gain the gain amplifier provides at different tap positions and frequencies, a Schlumberger 1260 impedance/gain-phase analyzer was used. To begin with, the actual voltage gain of the gain amplifier at all two hundred and fifty-six tap positions was measured.
For this measurement the input signal was set with amplitude of 5 mV\textsubscript{rms}, DC bias of 1.65 V, and a frequency of 1 kHz. In Figure 9.2 the results from the measurement are plotted against the ideal gain of the gain amplifier. As the desired gain of the amplifier increases the actual gain begins to drop off from the ideal gain expected. The difference between the ideal gain and actual gain is due to resistor mismatch and transmission gate mismatch in the potentiometer. As described in section 5, the potentiometer consists of several 1 k\textOmega\ in series with transmission gates at the tap positions. Mismatch in the resistance value of the transmission gates and resistors due to process variation cause the total resistance to be less than what is expected to create a high enough closed loop gain causing the difference in curves in Figure 9.2.

![Graph of Gain vs. Potentiometer Position](image)

Figure 9.2: Gain of the amplifier at different tap values

The response of the gain amplifier over different frequencies was then measured. For this the tap position of the gain amplifier was first set at a gain of ten while the input signal was set with an amplitude of 5 mV\textsubscript{rms}, a DC bias of 1.65 V, and a variable frequency from 1 Hz to 1 MHz. As the frequency was swept from 1 Hz to 1 MHz the gain of the gain amplifier was recorded. Following this the measurement was repeated with the same conditions except that the tap position was set at a gain of 100. The results from the measurement at the two different tap positions are shown in Figure 9.3.
At frequencies below 10 Hz, the gain amplifier has trouble producing the desired amount of gain due to improper DC biasing at the inputs of the gain amplifier. However, at the higher frequencies the gain amplifier performs as expected. The major thing to take away from Figure 9.3 is the fact both gain curves have the same shape or magnitude response until a frequency above 10 kHz. At the frequencies above 10 kHz the operational amplifier used in the gain amplifier structure does not have enough open loop at the higher frequencies needed for the higher feedback resistance. The fact that the curves do match up till the 10 kHz mark means that the gain amplifier reacts the same to different frequencies at different gains as it was designed to do.

9.4 Low pass filter results

The primary function of the low pass filter is to filter out any signal from the eddy current probe above 10 kHz at any input amplitude and DC bias. In order to see if the low pass filter functions properly, the magnitude response of the filter over frequency was measured.
For this measurement the input amplitude of the filter was set to 1 Vpp with a DC bias of 1.65 V and then the frequency was varied from 1 Hz to 1 MHz. As shown in Figure 9.4, at frequencies below 10 Hz the magnitude of the filter is below -3 dB, while from 10 Hz to 10 kHz the magnitude of the filter is around 0 dB, and then at 10 kHz the magnitude goes back to -3 dB and begins to roll-off as expected. In the testing of the low pass filter a DC blocking capacitor was used to protect the test equipment. This DC blocking capacitor is in a series combination with the real impedance of the low pass filter which creates a low frequency pole. The magnitude response shown in Figure 9.4 indicates this series capacitance as well as the designed 10 kHz cutoff.

![Figure 9.4: Magnitude response of the low pass filter](image)

To see how the low pass filter performs at different DC bias voltages, the input signal to the filter was set to an amplitude of 1 Vpp with a frequency of 5 kHz while the DC bias voltage was swept from 0 V to 3.3 V. This same measurement was then repeated with a frequency of 10 kHz. As shown in Figure 9.5 over the range of about 0.1 V to 3.2 V the low pass filter performs as expected, because at 5 kHz the magnitude is approximately -0.7 dB, while at 10 kHz it is the expected value of -3 dB.
To test how the low pass filter performs to different input signal amplitudes the input signal DC bias was set to 1.65 V at frequency of 5 kHz while the amplitude was varied from 0.1 $V_{pp}$ to 2.1 $V_{pp}$ while the magnitude was recorded. The same measurement was then repeated for a frequency of 10 kHz. As shown in Figure 9.6 from an input amplitude of around 0.1 $V_{pp}$ to 1.65 $V_{pp}$ the filter performs as expected, because the magnitude of the 5 kHz signal is around -0.7 dB and the magnitude of the 10 kHz is at -3 dB like in Figure 9.5. Above the input amplitude of 1.65 $V_{pp}$ the low pass filter begins to not perform as expected due to the fact that the DC bias of 1.65 V and 1.65 $V_{pp}$ input signal causes the operational amplifier of the filter to saturate.
Figure 9.6: Low pass filter magnitude response to input amplitude

9.5 Digital-to-Analog converter results

The primary function of the digital-to-analog converter is to produce an analog voltage to be used as a DC bias offset to the gain amplifier. In order to characterize its performance the analog output versus digital input was measured as shown in Figure 9.7. From Figure 9.7 at a digital decimal input of two hundred and fifty-five the analog output only reaches about 1.0 V which is 2.3 V below the designed value. After further investigation into why the output is 2.3 V below the designed value, it was found that the resistances of the wire to the summing resistor in the DAC were not taken into account during the design of the DAC. Each current source has a wire with different length that the current travels to sink into the summing resistor of 400 Ω. This error in resistance causes a voltage drop of more than the designed value of 6.2mV causing voltage errors in the biasing of the current sources causing output voltage errors.
Since the DAC is integrated on chip, nothing could be done to fix the wire resistance discussed above to produce the right voltages needed to provide the DC bias to the gain amplifier internally. However, a resistor divider network can be connected to the output of the DAC as shown in Figure 9.8 to create a DC bias offset.

Figure 9.7: Analog output of the digital-to-analog converter

Figure 9.8: A DAC with a resistor divider network
The DC bias offset moves the center of the DAC to a higher voltage while still allowing the DAC to have the same voltage swing as before. Figure 9.9 shows how the addition of a resistor network on the output of the DAC can be used to change the voltage range allowing it to still be used in the overall design.

Figure 9.9: Comparison of a DAC without and with a resistor divider network
10 CONCLUSION

10.1 Summary of work

With the successful demonstration of the prototype digital processing system with wireless communication by Mike Reid, Ben Graubard, Robert Weber, and Julie Dickerson, the next phase of the project was to implement a system on chip [2]. The work presented in this document describes the implementation of a digital signal processing system on a fabricated chip. A detailed analysis on the design of the individual components required to create the digital signal processing system along with a description of how those individual components were implemented together to form a novel DSP system is shown. After the DSP system was fabricated in a TSMC 0.18-µm process a complete analysis was of that DSP system was completed. Measured results of the low pass filter, shift register, and gain amplifier indicate that these individual blocks perform as expected. However, measured results of the DAC indicated a low voltage output range problem caused by wire resistance. A resistor divider network was used to create a DC offset bias to overcome this problem. This DC offset bias adjusts the output voltage range of the DAC allowing it to still be used in the overall system. After exhaustive testing of the individual system blocks the entire system was wired together and tested successfully.

10.2 Main contributions to this work

While I was conducting this research from May 2003 to May 2005 there were no digital processing systems on chip for an eddy current probe available in the market. Therefore, a custom made system was required to meet design specifications. To produce a system meeting the specifications of the project required me to investigate the design of a low pass filter, shift register, gain amplifier, a DAC, and how these components could be combined together. Even though the investigations into the individual components of the DSP system were not novel the way the components were combined was.
After designing the individual components the overall systems had to be designed. The design required the overall power consumption, physical layout, testability, and system biasing of the DSP system to be taken into account. The overall power consumption consideration required an engineering tradeoff to be made between power used and the open loop gain of the amplifier. The physical layout consideration required the implementation of the individual components through the use of floor planning and layout techniques. The testability consideration required the design of test points throughout the DSP system so that the overall system performance could be analyzed and problems fixed if they arise. The last consideration in the design of the DSP systems was that of the system biasing. This consideration required the design of a temperature insensitive biasing cell and fail safe voltage in case the biasing cell malfunctions. The work presented in this thesis focused on the results of my investigations into these individual components for the digital signal processing system and the performance of the integrated circuit implementation.
APPENDIX A: PROOF OF EQUATION 2.4

Assuming the op-amp is ideal then the following holds true

\[ V_n = V_p = V_o \quad (A.1) \]
\[ I_n = I_p = 0 \quad (A.2) \]

At the node where \( R_1 \) and \( R_2 \) connect (node A) sum the currents out of the node using conductance:

\[ G_1 = \frac{1}{R_1}, \quad G_2 = sC_2, \quad G_3 = \frac{1}{R_2}, \quad G_4 = sC_4 \quad (A.3) \]

\[ (V_A - V_{in})G_1 + (V_A - V_p)G_3 + (V_A - V_n)G_2 = 0 \quad (A.4) \]

At node \( V_p \) sum the currents out of the node using conductance:

\[ V_pG_4 + (V_p - V_A)G_3 = 0 \quad (A.5) \]

Solve (G.5) for \( V_A \):

\[ V_pG_4 + V_pG_3 - V_AG_3 = 0 \quad (A.6) \]
\[ V_AG_3 = V_pG_4 + V_pG_3 \quad (A.7) \]
\[ V_A = V_p \frac{G_4}{G_3} + V_p \quad (A.8) \]

Now plug \( V_A \) back into Equation A.4 above:

\[
\left( V_p \frac{G_4}{G_3} + V_p \right) G_1 - V_{in} G_1 + \left( V_p \frac{G_4}{G_3} + V_p \right) G_3 - V_p G_3 + \left( V_p \frac{G_4}{G_3} + V_p \right) G_2 - V_n G_2 = 0 \quad (A.9)
\]

\[
V_p \frac{G_4 G_1}{G_3} + V_p G_1 - V_{in} G_1 + V_p G_4 + V_p G_3 - V_p G_3 + V_p \frac{G_4 G_2}{G_3} + V_p G_2 - V_n G_2 = 0 \quad (A.10)
\]

\[
V_o \frac{G_4 G_1}{G_3} + V_o G_1 - V_{in} G_1 + V_o G_4 + V_o \frac{G_4 G_2}{G_3} = 0 \quad (A.11)
\]

Solve for \( V_o \):

\[
V_o \left( \frac{G_4 G_1}{G_3} + G_1 + G_4 + \frac{G_4 G_2}{G_3} \right) = V_{in} G_1 \quad (A.12)
\]

\[
V_o \left( \frac{G_4}{G_3} + 1 + \frac{G_4}{G_1} + \frac{G_4 G_2}{G_3 G_1} \right) = V_{in} \quad (A.13)
\]

\[
V_o \left( \frac{G_1 G_4 + G_1 G_3 + G_2 G_4 + G_2 G_3}{G_1 G_3} \right) = V_{in} \quad (A.14)
\]

\[
V_o = \left( \frac{G_1 G_3}{G_1 G_4 + G_1 G_3 + G_2 G_4 + G_2 G_3} \right) V_{in} \quad (A.15)
\]

\[
V_o = \left( \frac{G_1 G_3}{s C_4 G_1 + G_1 G_3 + s C_4 G_3 + s C_2 s C_4} \right) V_{in} \quad (A.16)
\]

\[
V_o = \left( \frac{G_1 G_3}{s^2 C_2 C_4 + s C_4 (G_1 + G_3) + C_1 G_3} \right) V_{in} \quad (A.17)
\]
APPENDIX B: PROOF OF EQUATION 4.2

\[ V_n = V_p \]  \hspace{1cm} (B.1)

\[ I_n = I_p = 0 \]  \hspace{1cm} (B.2)

\[ \frac{V_n - V_{in}}{R_1} + \frac{V_n - V_{Out}}{R_2} = 0 \]  \hspace{1cm} (B.3)

\[ V_n = V_p = V_{DAC} \]  \hspace{1cm} (B.4)

\[ \frac{V_{DAC} - V_{in}}{R_1} + \frac{V_{DAC} - V_{Out}}{R_2} = 0 \]  \hspace{1cm} (B.5)

\[ \frac{V_{DAC} - V_{Out}}{R_2} = \frac{V_{in} - V_{DAC}}{R_1} \]  \hspace{1cm} (B.6)

\[ V_{DAC} - V_{Out} = \frac{R_2}{R_1} (V_{in} - V_{DAC}) \]  \hspace{1cm} (B.7)

\[ -V_{Out} = \frac{R_2}{R_1} (V_{in} - V_{DAC}) - V_{DAC} \]  \hspace{1cm} (B.8)

\[ V_{Out} = -\frac{R_2}{R_1} (V_{in} - V_{DAC}) + V_{DAC} \]  \hspace{1cm} (B.9)
APPENDIX C: PROOF OF EQUATION 4.3

\[ V_n = V_p \]  \hspace{1cm} (C.1)

\[ I_n = I_p = 0 \]  \hspace{1cm} (C.2)

\[ \frac{V_n - V_{in}}{R_1} + \frac{V_n - 1.65}{R_1} + \frac{V_n - V_{Out}}{R_2} = 0 \]  \hspace{1cm} (C.3)

\[ V_n = V_p = V_{DAC} \]  \hspace{1cm} (C.4)

\[ \frac{V_{DAC} - V_{in}}{R_1} + \frac{V_{DAC} - 1.65}{R_1} + \frac{V_{DAC} - V_{Out}}{R_2} = 0 \]  \hspace{1cm} (C.5)

\[ \frac{V_{DAC} - V_{Out}}{R_2} = \frac{V_{in} - V_{DAC}}{R_1} + \frac{1.65 - V_{DAC}}{R_1} \]  \hspace{1cm} (C.6)

\[ V_{DAC} - V_{Out} = \frac{R_2}{R_1} (V_{in} - V_{DAC} + 1.65 - V_{DAC}) \]  \hspace{1cm} (C.7)

\[ -V_{Out} = -V_{DAC} + \frac{R_2}{R_1} (V_{in} + 1.65 - 2 \cdot V_{DAC}) \]  \hspace{1cm} (C.8)

\[ V_{Out} = V_{DAC} - \frac{R_2}{R_1} (V_{in} + 1.65 - 2 \cdot V_{DAC}) \]  \hspace{1cm} (C.9)

\[ V_{Out} = -\frac{R_2}{R_1} (V_{in} + 1.65 - 2 \cdot V_{DAC}) + V_{DAC} \]  \hspace{1cm} (C.10)
APPENDIX D: POTENTIOMETER DECODER SCHEMATIC
APPENDIX E: 4-TO-16 DECODER SCHEMATIC
APPENDIX F: 4-TO-16 ENABLED DECODER SCHEMATIC
APPENDIX G: OPERATIONAL AMPLIFIER SCHEMATIC
Using the small-signal model above and keeping in mind that in small-signal models that voltage sources become shorts or wires, the gate of M₁ and M₂ become shorted to ground thus

\[ V_{gs2} = V_{bs2} = -V_1 \]  \hspace{1cm} (H.8)

\[ V_{gs1} = 0 \]  \hspace{1cm} (H.9)

If the currents out of node \( i_{out} \) in the small-signal model are summed using Kirchoffs current law then the following can be written

\[ -i_{out} + g_m V_{g2}V_{gs1} + g_m V_{bs2}V_{bs2} + V_{out} - V_1 = 0 \]  \hspace{1cm} (H.10)

Substituting (8.8) and (8.9) into (8.10)

\[ -i_{out} - g_m V_1 - g_m V_{bs2}V_1 + \frac{V_{out} - V_1}{r_{ds2}} = 0 \]  \hspace{1cm} (H.11)
Since

\[ V_1 = i_{out} r_{ds1} \]  \hspace{1cm} (H.12)

\[-i_{out} - g_{m2} i_{out} r_{ds1} - g_{mbs2} i_{out} r_{ds1} + \frac{V_{out} - i_{out} r_{ds1}}{r_{ds2}} = 0 \]  \hspace{1cm} (H.13)

\[ \frac{V_{out} - i_{out} r_{ds1}}{r_{ds2}} = i_{out} + g_{m2} i_{out} r_{ds1} + g_{mbs2} i_{out} r_{ds1} \]  \hspace{1cm} (H.14)

\[ V_{out} - i_{out} r_{ds1} = i_{out} r_{ds2} + g_{m2} i_{out} r_{ds1} r_{ds2} + g_{mbs2} i_{out} r_{ds1} r_{ds2} \]  \hspace{1cm} (H.15)

\[ V_{out} = i_{out} r_{ds1} + i_{out} r_{ds2} + g_{m2} i_{out} r_{ds1} r_{ds2} + g_{mbs2} i_{out} r_{ds1} r_{ds2} \]  \hspace{1cm} (H.16)

\[ V_{out} = i_{out} (r_{ds1} + r_{ds2} + g_{m2} r_{ds1} r_{ds2} + g_{mbs2} r_{ds1} r_{ds2}) \]  \hspace{1cm} (H.17)

\[ r_{out} = \frac{V_{out}}{i_{out}} = r_{ds1} + r_{ds2} + g_{m2} r_{ds1} r_{ds2} + g_{mbs2} r_{ds1} r_{ds2} \]  \hspace{1cm} (H.18)

Given that

\[ g_{m2} r_{ds2} \gg 1 \]  \hspace{1cm} (H.19)

\[ g_{m2} > g_{mbs2} \]  \hspace{1cm} (H.20)

\[ \therefore r_{out} \approx (g_{m2} r_{ds2}) r_{ds1} \]  \hspace{1cm} (H.21)
APPENDIX I: OVERALL SCHEMATIC OF THE 8-BIT DAC
APPENDIX J: BIAS CURRENT SOURCE LAYOUT
APPENDIX K: 4-TO-16 ENABLED DECODER LAYOUT
APPENDIX L: DAC LAYOUT
APPENDIX N: LOW PASS FILTER LAYOUT
APPENDIX O: SHIFT REGISTER LAYOUT
APPENDIX P: DSP SYSTEM LAYOUT
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