Measurement of mobility in nanocrystalline semiconductor materials using space charge limited current

Daniel Paul Stieler

Iowa State University

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Measurement of mobility in nanocrystalline semiconductor materials using space charge limited current

by

Daniel Paul Stieler

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Vikram L. Dalal (Major Professor)
Joseph Shinar
Rana Biswas

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This is to certify that the master's thesis of

Daniel Paul Stieler

has met the thesis requirements of Iowa State University

Signatures have been redacted for privacy
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ABSTRACT

A new technique for measuring mobility of carriers in device-type structures is used to determine the mobility of both electrons and holes in nanocrystalline Si materials. The technique is based on space charge limited current. When the injected space charge exceeds the resident charge, the current is directly related to the mobility. Unlike Hall measurements, this technique allows for a determination of mobility in the direction of transport (vertical or growth direction) in device type structures, deposited on conducting substrates.

The samples that were studied were fabricated primarily using a hot wire deposition technique from mixtures of silane and hydrogen. The crystallinity and grain size were systematically varied by changing the deposition chemistry and growth temperatures. Crystallinity was determined using Raman spectroscopy, and grain sizes were determined using x-ray diffraction techniques. In addition to hot wire samples, a few samples were also made using both ECR-PECVD and VHF-PECVD techniques. For measuring electron mobility, samples of the type n+nn+ were used. Care was taken to minimize series resistance due to contacts or thin oxide layers. Four point probe measurements were used to eliminate spurious series resistance. For measuring hole mobility, samples of the type p+pp+ were used.

The electron mobility was found to vary between 1 and 5 cm$^2$/V-s. In general, the mobility increased with grain size. The mobility also increased with measurement temperatures, indicating that transport across the grain boundaries was the factor limiting the mobility. Mobility also increased with thickness, because the material became more crystalline with increasing thickness. The largest mobility of holes measured was 2.7 cm$^2$/V-s, which is on the same order as the mobility of electrons.
A major advantage of the current technique for measuring mobility is that it can be used for both doped and undoped layers, unlike time of flight technique which can only be used for relatively lightly-doped layers. Another advantage is that we obtain values of mobility in the direction in which transport takes place in solar cell devices.
1. INTRODUCTION

1.1 History

Historically many semiconductor devices have been fabricated on single crystal silicon wafers. Silicon wafers are easy to process and there is an abundance of silicon making it relatively inexpensive. Devices fabricated on silicon wafers use more silicon than necessary, since wafers are ~ 500 µm thick and devices only penetrate a few micrometers into the wafer. For this reason costs could be reduced by depositing devices on foreign substrates using thin film technologies. Using chemical vapor deposition techniques (CVD), thin layers of silicon can be deposited on various types of substrates, such as polyimide, glass, or stainless steel [1].

Nanocrystalline silicon is an important thin film semiconductor material. It has been used in the fabrication of thin film transistors [2] and solar cells [3, 4]. Single crystal solar cells do not degrade and have higher efficiency than thin film amorphous solar cells. To increase the efficiency of thin film solar cells, micromorph cells are being developed [4, 5]. Micromorph solar cells consist of an amorphous and nanocrystalline solar cell in tandem [4, 5]. This configuration yields higher cell efficiency than just amorphous or nanocrystalline cells [4, 5]. Thin film amorphous and nanocrystalline semiconductors have very different optical and electrical properties than crystalline silicon. Nanocrystalline silicon is not a single type of material, but a family of materials with various grain sizes, grain orientations, and interfacial layers. Therefore, systematic research is being done to characterize deposition methods, optical properties, and electrical properties of thin film nanocrystalline semiconductors.
1.2 Objectives of Project

Recently there has been an increased interest in using nanocrystalline silicon to create thin film transistors and photovoltaic devices. To do this effectively it is important to know the electrical properties of the material. One important electrical property is the mobility of carriers. Measuring mobility is not a trivial task. One way to measure the mobility of a semiconductor is to use the Hall Effect. To measure Hall Effect mobility, accurately, requires special sample geometry, an extremely low noise apparatus, and a high powered magnet. To measure Hall Effect mobility, a film must be prepared on an insulating substrate, like glass. Unfortunately, nanocrystalline silicon grown on glass will have different electronic and structural properties than a layer that is grown on an n+ amorphous silicon layer, even if the same growth parameters are used. The intrinsic or i-layer of a thin film p-i-n solar cell is deposited on n+ amorphous silicon; So, it would be valuable to know the mobility of an i-layer grown on an n+ amorphous silicon layer. The objective of this research is to develop a process to determine the mobility of electrons in an n-type material and the mobility of holes in a p-type material by measuring space charge limited current (SCLC). In order to make such a measurement, both fabrication and measurement techniques will need to be examined and refined. Mobility derived from the space charge limited current region of operation of an n-i-n device will yield an effective mobility value of the i-layer in the vertical direction, as shown in Figure 1.2.1. The effective mobility found by measuring SCLC differs from the
more traditional Hall mobility, since the Hall Effect measures mobility in the horizontal direction. Effective mobility measured using SCLC will be the minimum mobility for that nanocrystalline i-layer because mobility will be reduced by oxide, amorphous, and seed layers in the device. Also, if the crystallinity of a film is poor the mobility will be reduced due to an increased number of potential barriers within the material. If the crystal to amorphous ratio measured by the Raman effect is large, then the effective conductivity in the vertical direction of the device will be dominated by the crystal and amorphous phases instead of the grain boundaries, since there are fewer grain boundaries for electrons to pass through [6]. Structural properties of the i-layer can be compared to mobility values to find a relationship between grain size and mobility. An important comparison that can be made is the mobility of a given i-layer structure to the performance of a solar cell containing that same layer.
2. SAMPLE PREPARATION

Intrinsic layers of the samples were prepared using hot wire, or catalyst, chemical vapor deposition (HWCVD), electron-cyclotron resonance chemical vapor deposition (ECRCVD), and very high frequency plasma enhanced chemical vapor deposition (VHF-PECVD). The substrate chosen for the n-i-n devices was stainless steel. Stainless steel is cheap compared to other substrate materials, readily available, and used for fabricating p-i-n solar cells. Both the top and the bottom n+ layers were deposited using electro-cyclotron resonance chemical vapor deposition (ECRCVD) and phosphine (PH₃) was used as the dopant gas for the n+ layers.

2.1 Hot Wire Chemical Vapor Deposition (HWCVD)

Depositions done using hot wire chemical vapor deposition (HWCVD) were done in a combined ECR-HWCVD reactor. A schematic of this reactor is shown in Figure 2.1.1. The intrinsic layer of the device was the only part deposited using the HWCVD method. Filaments for HWCVD depositions were made using .5mm diameter Tantalum wire coiled around a 3/8” diameter rod. A picture of a filament can be seen in Figure 2.1.2. Each deposition was performed with either one or two filaments. The filament to substrate distance was kept large, 13cm, to minimize substrate heating due to the filaments. If the distance between the filaments and substrate is not large the substrate temperature will increase significantly during the deposition [3]. The largest grain sizes, ~56nm, in this work were achieved by
using the HWCVD process at low pressures, ~10mT. The growth process has been described previously by Ring [7], Heintz [8], Hammers [9], and Kuprich [5]. Deposition parameters for the i-layers of devices are located in Appendix A.

![Diagram of HW/ECRCVD reactor](image)

Figure 2.1.1. Schematic of combined HW/ECRCVD reactor

2.3 Electron-Cyclotron Resonance Chemical Vapor Deposition (ECRCVD)

The heavily doped n+ layers and i-layers were deposited using ECRCVD. ECRCVD uses a magnetic field and 2.45GHz microwaves to create a plasma from Hydrogen or Helium gas. When the electrons reach a cyclotronic frequency of 2.45GHz, then the plasma ignites. The plasma leaves the plasma section of the chamber through a restricting orifice, which focuses the plasma on the substrate. The process gases enter the chamber next to the
substrate holder where they are decomposed by the plasma. ECRCVD plasma is very dense and does an excellent job dissociating the processes gases. For more information about ECRCVD see Niu [10].

2.4 Very High Frequency Plasma Enhanced Chemical Vapor Deposition (VHF-PECVD)

Intrinsic layers for both n-i-n and p-i-p devices were deposited using VHF-PECVD. Nanocrystalline silicon depositions were performed at a frequency of 44.5 MHz, RF power of 20-30 watts, and pressures of 50-100 mTorr. To make an i-layer for a p-i-p device, parts per million (ppm) levels of Trimethyl Boron were added to the mixture of silane and hydrogen gas. For more information about the VHF-PECVD and the nanocrystalline silicon growth process see Dalal [11, 12] and Vetterl [13]. For general information about PECVD see Plummer [14].

2.4 Deposition Procedure

To deposit the i-layer (intentionally not-doped layer) of an n-i-n device, a substrate with a predeposited n+ layer is etched in buffered oxide etch, rinsed with deionized water, and placed in methanol, or directly transferred from one reactor to the next with minimum exposure to atmospheric gases. After etching, the sample is transported in methanol to the room with the reactor. Next, the sample is removed from methanol and dried by blowing compressed nitrogen across it. Once the sample is dry it is placed on the substrate heater and a one inch square mask is screwed onto the substrate heater to hold the sample in place and
ensure uniform thermal contact with the heater. After the sample has been fastened to the 
substrate heater it is blown off with compressed nitrogen to remove any particles that may 
have fallen onto it and loaded into the reactor. When the chamber reaches a pressure of 
$3 \times 10^{-6}$ Torr, after many purge cycles with nitrogen gas, the shutter shielding the substrate 
from deposition is verified to be closed and a layer of amorphous silicon is deposited on the 
chamber walls to bury any impurities present on the walls of the reactor. Also while the 
amorphous silicon is depositing on the walls, the temperature of the substrate is ramped up to 
the desired value. Temperature is never ramped up before hydrogen or silane gases are 
flowing in the reactor to ensure there will not be oxidation of the n+ layer. After the chamber 
walls have been coated to bury impurities, hydrogen is introduced into the reactor and the hot 
wire is energized. This process removes the silicides, deposited during the amorphous 
silicon layer, from the filament. Next, the i-layer is deposited on the n+ layer. Once the 
deposition is complete the sample is cooled in hydrogen and silane until it is below 70 
degrees Celsius to reduced chances of oxidation. After cooling the sample is directly 
transferred to the ECRCVD reactor for deposition of the top n+ layer. A direct transfer from 
one reactor to the next is done as quickly as possible to reduce oxidation of the surface and 
collection of moisture in the film [15].

2.6 Contact Formation

Forming a low resistance, ohmic contact is very important. The contact provides an 
electrical connection to the device and allows the extraction of current versus voltage data. If 
the contact is not ohmic or is very resistive the slope of the current versus voltage curve will 
be affected and significant amounts of error can be introduced into the measurement.
2.6.1 Metallization

Two different materials were used for contacts on the n-i-n and p-i-p devices. For the n-i-n devices aluminum was deposited as the top contact layer. The work function of aluminum closely matches the Fermi level of the n+ layer. For the p-i-p devices chromium was deposited as the top contact layer. The work function of chromium matches the Fermi energy of the p+ layer more closely than aluminum. The chromium or aluminum dots were deposited by placing a mask, like the one shown in Figure 2.6.1, on top of the sample prior to the evaporation. To minimize the tapering of the thickness of the metal by the sides of the contacts the mask used is very thin.

When the Aluminum or Chromium is ready to be evaporated it is heated until the desired evaporation rate is reached, as measured by a thickness monitor using a piezoelectric crystal. Once the desire rate has been reached the shutter is opened and the thickness monitor is restarted simultaneously. During the deposition, the deposition rate and the chamber pressure are monitored to ensure they stay within tolerance and a good quality metal layer is deposited. Upon reaching the desired thickness, the voltage is shut off, the chamber is backfilled with nitrogen to atmospheric pressure, and the sample can be removed. Aluminum depositions were done at a rate of ~30 Å/s with a total thickness of ~2500Å, while Chromium depositions were done at a rate of 5 Å/s with a total thickness of ~1000Å. The maximum allowed chamber pressure during the deposition was $4 \times 10^{-6}$ Torr.
2.6.2 Thermal Annealing

After depositing metal contacts it is important to thermally anneal the metal before testing the device. Samples were annealed at 150C for 45-90 minutes. This anneal step allows the metal to punch through any thin oxide layer on the top n+ layer of the device and causes the droplets of evaporated aluminum to combine into a more uniform material.

2.6.3 Electrical Annealing

The final step before measuring the SCLC characteristic of an n-i-n or p-i-p device is to electrically anneal the contact by driving a high current through it. This was done by driving a .3A current through the device for 10-30 minutes. This step further reduces the contact resistance and improves the ohmic properties of the contact. The resistance of the contact was found to decrease considerably after it had been electrically annealed.
3. CHARACTERIZATION METHODS

To characterize the devices the following measurements were performed: UV/VIS/IR Spectroscopy, Raman Spectroscopy, X-Ray Diffraction, and Space Charge Limited Current. Care was taken to use proper technique when performing each measurement, so that the data collected was reasonable.

3.1 UV/VIS/NIR Spectroscopy

To measure the thickness of the various layers and devices a Lambda 19 UV/VIS/IR spectrophotometer made by Perkin Elmer was used. The spectrophotometer was connected to a computer, which allowed easy modification of the measurement parameters and collection of measured data.

Films and devices studied in this work are very thin, so an interference pattern is seen in the reflection and transmission graphs. The interference pattern is caused by the reflection of light off of the front surface and the back surface of the film as shown in Figure 3.1.1. The reflections off of the front and back of the film add together when in phase and subtract when out of phase to create the interference pattern. From this series of peaks and valleys the thickness of the film can be calculated using Equation 3.1.1. In this equation $\lambda_1$ and $\lambda_2$ are consecutive
peaks or troughs, $n_1$ and $n_2$ are the refractive index of the material at those peaks or troughs, and $t$ is the thickness of the film.

\[
    t = \frac{\lambda_1 \cdot \lambda_2}{2 \cdot (n_1 \cdot \lambda_1 + n_2 \cdot \lambda_2)}
\]

Equation 3.1.1

For thickness measurements transmission or reflection were measured from 2500nm to 1000nm. The refractive index does not change quickly over this range of wavelengths making it the best range to perform measurements in. Transmission measurements were used to determine the thickness of a film grown on glass and reflection measurements were used to determine the thickness of a device grown on stainless steel.

3.2 Raman Spectroscopy

Raman spectroscopy is a method used to determine the crystallinity of a film. On n-i-n devices the Raman measurement has to be performed before depositing the top n+ layer, since the laser cannot penetrate through the top n+ layer. The equipment used to perform Raman measurements was an inVia Reflex Raman microscope manufactured by Reinshaw. To perform the Raman measurement a laser impinges on the sample and the photons reflected off of the sample are collected by a CCD. The photons from the laser collide with the sample and are scattered. The majority of the photons are elastically scattered off of the sample. This type of scattering is known as Raleigh scattering and does not give any information. The rest of the photons are inelastically scattered off of the material, this is known as Raman scattering. This inelastic scattering either creates or destroys a phonon in the lattice. Phonons created in the lattice are known as anti-stokes, while phonons destroyed
are known as stokes. Any phonons generated by the Raman scattering process are dissipated in the lattice as heat. Phonons in the lattice vibrate at a characteristic frequency for each material, so as photons are scattered a very sharp peak occurs at the wavenumber corresponding to the phonon's vibratory frequency. For crystalline silicon this wavenumber is 520 cm\(^{-1}\) and for crystalline germanium the wavenumber is 300 cm\(^{-1}\) [10, 16, 17]. If the material is amorphous it has a broad range of phonon modes due to the structural disorder. For amorphous silicon the peak occurs at 485 cm\(^{-1}\) and for amorphous germanium the peak occurs at 278 cm\(^{-1}\) [10, 16, 17]. A Lorentzian function is used to fit the shape of the crystalline peaks and a Gaussian function is used to fit the amorphous peaks. After the data has been collected and the peaks have been fit, the position and the maximum intensity of each peak are known. The ratio of the maximum intensity of the crystalline peak to the amorphous peak gives a reasonable approximation of the crystalline composition of the film [18, 11]. Figure 3.2.1 shows a typical Raman spectrum for a nanocrystalline silicon film. In this case, the crystalline peak has a maximum intensity of 8113 photons and the amorphous peak has an intensity of 1817 photons, so the film has a crystal: amorphous ratio of 4.47:1. Thus the film is about 82% crystalline.
3.3 X-Ray Diffraction

X-Ray diffraction is used to determine the crystallite size and orientation in nanocrystalline semiconductors. X-Ray diffraction measurements were performed with a Siemens X-Ray diffractometer utilizing a sealed copper anode x-ray tube. This diffractometer was connected to a computer to automate control of the diffractometer and collect data.

Crystalline materials are periodic in nature. When the wavelength of the x-ray beam is equal to the distance between crystal planes Bragg’s law is satisfied, photons are collected by the detector, and a peak is formed on the diffraction pattern. Bragg’s law is shown in Equation 3.3.1. In this equation, $\lambda$ is the wavelength of the x-rays, $d$ is the spacing of the planes in the lattice, and $\theta$ is the angle of incidence of the x-rays on the sample. For a peak at
a given incident angle, \( \theta \), of x-rays there is a specific material and crystal plane, (111); (220); (311), that it corresponds to.

\[ n\lambda = 2d \sin \theta \]
Equation 3.3.1

Once the data has been collected, an x-ray diffraction analysis program called JADE 7.5 is used to deconvolve the x-ray diffractogram. Care must be taken to ensure the baseline is fit properly and the each peak fits the experiment data. The peak deconvolution gives the full width at half max (FWHM), the maximum intensity, the center, and calculates the estimated grain size using Scherer’s formula [19], Equation 3.3.2. In Equation 3.3.2, \( d \) is the grain size, \( \beta \) is the FWHM, \( \theta \) is the incident angle of the x-rays, and \( \lambda \) is the wavelength of the x-rays.

\[ d = \frac{0.9\lambda}{\beta \cos \theta} \]
Equation 3.3.2

In nc-Si:H x-ray peaks occur at \( \sim 28.5 \) degrees and \( \sim 47 \) degrees \( 2\theta \) as seen in Figure 3.3.1. The first peak corresponds to \(<111>\) oriented grains and the second peak corresponds to \(<220>\) oriented grains.

![Figure 3.3.1. Typical x-ray spectrum of nc-Si:H on 7059 Corning glass](image-url)
3.4 Space Charge Limited Current (SCLC)

Insulators and semiconductors experience a phenomenon known as space charge limited current (SCLC) once the number of carriers injected into the sample exceeds the number of traps or resident charge in the sample. SCLC results from the fact that when the injected carrier concentration exceeds the thermal carrier concentration, the electric field in the sample becomes very non-uniform, and the current no longer follows Ohm’s law. The device used to measure SCLC is an n-i-n device as stated previously. The band diagrams for an n-i-n device, both in thermal equilibrium and under electrical bias, are shown in Figure 3.4.1. The n+ layers grown on each side of the i-layer are very heavily doped, thus causing the Fermi level to move into the conduction band. Heavily doping the layers on both sides of the intrinsic layer allows electrons to easily be injected into the intrinsic layer. To study the mobility of holes, the n+ layers of the device would be replaced by p+ layers.

The exact theory of SCLC is rather complicated and extremely difficult to work with, so a simplified theory is used. (For information regarding the exact theory consult Lampert
The simplified theory neglects the diffusion current in the device. This is a reasonably good simplification to make when a device enters SCLC, since there are more carriers injected into the device than free carriers resident in the device. In order for the simplified theory to be valid, the distance between n+ layers of the device, distance L, must be much larger than the sum of the depletion widths, W_c and W_a, inside the i-layer of the device and the contacts must have a low resistivity. To show that the simplified theory is valid assume $V_{SCLC} >> KT/q = V_T$ and that the voltage drop across the device is V. If $V > V_{SCLC}$, then $V >> KT/q$. Looking at the band diagram under a bias voltage for the section of the device from $0 < X < W_c$, the drift current opposes total current flow, so $J = J_{diffusion} - |J_{drift}|$ [20]. The potential minimum occurs at $W_c$. J at a potential minimum is solely due to the diffusion current [20]. For $W_c < X$, both drift and diffusion currents are contributing to the total current. Within the bulk of the device the carrier concentration is assumed not to vary rapidly with position [20]. The equation for diffusion current density is shown in Equation 3.4.1 and the equation for drift current density is shown in Equation 3.4.2.

$$J_{diffusion} = -q * V_T * \mu * \frac{dn}{dx}$$

*Equation 3.4.1*

$$J_{drift} = q * \mu * n * \frac{V}{L}$$

*Equation 3.4.2*

In Equation 3.4.1 and 3.4.2, q is the charge of an electron, $V_T$ is the thermal voltage, $\mu$ is the mobility of electrons, n is the carrier concentration, V is the voltage, L is the distance between n+ layers, and $dn/dx$ is the rate of change of carrier concentration with distance. If $n_{average}/L$ is substituted into Equation 3.4.1 for $dn/dx$, then the result is Equation 3.4.3.

$$J_{diffusion} = -q * V_T * \mu * \frac{n_{average}}{L}$$

*Equation 3.4.3*
If $V >> V_T$ then $J_{\text{drift}} >> J_{\text{diffusion}}$, so $J_{\text{total}}$ is almost entirely due to drift current in the bulk of the material [20]. Since the total current is due almost entirely to drift current the diffusion current can be neglected and the simplified theory is obtained.

The voltage where all traps in the material are filled or the injected charge exceeds the resident charge is known as the trap filled limit voltage or $V_{\text{SCLC}}$. The current versus voltage curve of a semiconductor or insulator has several different regions. At voltages below the trap filled limit voltage, the semiconductor will exhibit an ohmic characteristic dictated by Equation 3.4.4. When the applied voltage is almost entirely absorbed across the bulk of the device Ohm’s law is observed [21]. In this equation $q$ is the charge of an electron, $n_0$ is the carrier concentration, $A$ is the area, $\mu$ is the effective mobility, $t$ is the thickness of the i-layer of the device, and $R$ is the total resistance of the sample.

$$I = \frac{q * n_0 * A * \mu * V}{t} = \frac{V}{R}$$

Equation 3.4.4. Ohm’s Law

The voltage where the current versus voltage characteristic of the semiconductor changes from ohmic to SCLC, $V_{\text{SCLC}}$, occurs when the injected charge is comparable to the thermal charge in the semiconductor and can be calculated using Equation 3.4.5. In this equation $q$ is the charge of an electron, $n_0$ is the carrier concentration, $t$ is the thickness of the i-layer, and $\varepsilon$ is the permittivity of the material.

$$V_{\text{SCLC}} = \frac{q * n_0 * t^2}{\varepsilon}$$

Equation 3.4.5. SCLC transition voltage
Once the trap filled limit has been reached, the sample has entered the space charge limited current region of operation, mathematically shown in Equation 3.4.6. In this equation $\varepsilon$ is the permittivity of the material, $A$ is the area of the contact, $\mu$ is the effective mobility of the material, and $t$ is the thickness of the i-layer.

$$I = \frac{9*\varepsilon*A*\mu}{8*t^3}V^2$$

Equation 3.4.6. SCLC current-voltage characteristic

To determine the mobility and carrier concentration of the i-layer of a device the experimental data must be closely examined. First, the thickness of each layer of the device must be determined carefully, so that an accurate i-layer thickness is found. An error of 10% in the thickness will introduce an error of 25% into the value of the estimated mobility, since mobility changes with $t^3$. Next, the current versus voltage (IV) data for the device is plotted, as shown in Figure 3.4.2. This plot is examined and broken down into two separate regions. The ohmic region is a linear region that starts at 0 volts and continues up to $V_{SCLC}$. $V_{SCLC}$ is found where the IV curve changes from the linear to quadratic region of operation. After $V_{SCLC}$ is reached the IV curve should exhibit a current versus voltage squared ($V^2$) dependence and can be fitted with a second order polynomial. If the IV plot only exhibits a linear region that means that the voltage across the device
during the measurement was not sufficient to put the device into the SCLC region of operation or there is a short circuit across the i-layer of the device. To determine the resistivity of the sample, a line is fit to the linear, ohmic, section of the IV curve. From the slope of this line the resistivity can be determined using Equation 3.4.7. In this equation \( \rho \) is the resistivity, \( A \) is the area of the contact, \( \text{Slope}_{\text{ohmic}} \) is the slope of the ohmic portion of the curve, and \( t \) is the thickness of the i-layer of the sample.

\[
\rho = \frac{A}{\text{Slope}_{\text{ohmic}} \times t}
\]

Equation 3.4.7. Resistivity

To determine the mobility, plot the experimental data, so that current is on the y-axis and voltage squared is on the x-axis, as shown in Figure 3.4.3. Once again there are two portions of this curve, ohmic and SCLC. With the data plotted like this the ohmic region of the curve looks like a square root function and the SCLC portion of the curve is linear. A line is fit to the linear, SCLC, portion of the curve and the slope of this line is used to calculate the effective mobility using Equation 3.4.8. Equation 3.4.8 is derived from Equation 3.4.6, where \( I/V = \text{Slope}_{\text{IV vs V}} \) and the equation is solved for \( \mu \).

![Figure 3.4.3. IV² curve of an n-i-n device](image)
Finally, the carrier concentration of the material can be calculated using two different methods. In the first method, the carrier concentration can be calculated by using Equation 3.4.9. In this equation $n$ is the carrier concentration, $\rho$ is the resistivity, $\mu$ is the mobility, and $q$ is the charge of an electron.

$$n_0 = \frac{1}{q \rho \mu}$$

Equation 3.4.9. Carrier concentration

The second method used to calculate the carrier concentration uses the voltage where the sample transitioned from ohmic operation to SCLC, $V_{SCLC}$. This calculation can be done using Equation 3.4.10, which is simply Equation 3.4.5 solved for $n_0$.

$$n_0 = \frac{q V_{SCLC} t^2}{\varepsilon}$$

Equation 3.4.10. SCLC transition voltage

Carrier concentration is determined using both methods to verify that the experimental data is reasonable and show that the data is self consistent.

In the next chapter considerations for growing devices to collect SCLC data, building an apparatus to measure SCLC, and measurement procedures will be discussed.
4. RESULTS AND DISCUSSIONS

There were two major sections of this project. The first section was to construct an apparatus capable of accurately measuring the mobility of nanocrystalline silicon using SCLC. Two different apparatuses were setup. The first system supplied a DC current to the device and measured the voltage. The second system generated a voltage pulse across the device and a resistor and measured the voltage across the resistor. The second section was to develop a procedure for growing n-i-n and p-i-p devices that yielded a reasonable value for the effective mobility.

4.1 Apparatus

4.1.1 DC Measurement of SCLC

Determining the right set of equipment to perform the SCLC mobility measurements took a few iterations. Initially, there was an apparatus designed for measuring the defect density, using SCLC, of amorphous silicon. This apparatus consisted of a Keithley 617 electrometer and a set of two probes. The internal voltage supply on the electrometer was used to bias the sample and the electrometer measured the current. This equipment did not work for measuring mobility in nanocrystalline silicon using SCLC because it could not measure currents above 2mA. Most devices did not reach $V_{SCLC}$ with a current of this magnitude.

Next, a pair of Keithley 177 DMMs, a Hewlett Packard E3611A power supply, and two probes were used to perform the measurement. Sample biasing was done using the
Hewlett Packard power supply; one Keithley 177 DMM was used to measure the voltage the power supply was supplying; and the other DMM was used to measure the current across the sample. This system allowed SCLC to be reached, since the power supply was capable of supplying a maximum of 3A. A spreadsheet was constructed to determine how much voltage was being dropped across the DMM when measuring any current in any of the ranges. The specification for the Keithley 177 DMMs stated that for a full scale current in each range the meter would drop 20mV. This spreadsheet was used to correct the voltage data to account for the meter effects. Using this system SCLC data could be collected and mobilities could be calculated.

To gain more accuracy in the SCLC measurement, a third system was assembled. This system utilized a Keithley 2400 SourceMeter, which could source the current and measure the voltage across the sample. Initially this was setup to use two probes like the other systems, however to reduce the contact resistance to the stainless steel substrate, which was about .3Ω, a third probe was added. This was the final iteration of the DC measurement system. The sourcemeter was used in four point probe and constant current modes. Constant current mode means the current was chosen and the voltage was measured. Measurements were performed inside of an aluminum box on an aluminum block with a 120V heater attached to the bottom of it and a thermocouple attached to the top of the block next to the sample. This configuration allowed measurements to be made at various temperatures from room temperature, ~23C, to 150C. The source meter was not electrically connected to the sample in a true four point probe configuration. Both the current driving wires and the voltage measuring wires were connected to the sourcemeter using banana connectors. The voltage measuring wires were converted to a BNC connection and then to a triax connection before entering the aluminum measurement enclosure. The current supply wires entered the
aluminum measurement enclosure through a pair of binding posts. Once inside the box the positive leads of the voltage and current wires were connected to the same gold plated telescoping probe, which was lowered onto the top contact of the sample. The negative voltage measuring and current supplying leads were attached to separate gold plated telescoping probes and then lowered onto a portion of the stainless steel substrate close to each other. Before placing the probes onto the substrate, it must be lightly sanded to remove any oxide layer. Using two probes on the stainless steel substrate yielded better results because the resistance between the gold contacts and the stainless steel substrate was between .3 and .6Ω, which introduced a significant amount of error into the IV measurement, especially at high currents. Connecting both the positive voltage and current leads to the top

![Figure 4.1.1. Schematic of system designed to measure SCLC using the DC method](image)
of the same probe eliminates the parasitic resistance of the wires and connectors leading up to the probe. This measurement configuration yielded the most reproducible results. Figure 4.1.1 shows a schematic of the final measurement system.

4.1.2 Pulsed Measurement of SCLC

Measurements made using a DC current have limitations, primarily because the power being dissipated by the device increases the temperature of the device significantly causing the IV curve to deviate from its quadratic nature at high currents. To solve this self-heating problem short duty cycle current pulses were used. The use of current pulses enabled the collection of an IV curve with a maximum current of 1\,A. The maximum current for the DC system before heating effects became noticeable was between .3 and .4\,A. With the ability to drive larger currents, thicker devices or devices with larger dopings can be measured.

The pulsed apparatus was the same as the DC apparatus except for the Keithley 2400 SourceMeter was replaced by an HP 214B Pulse Generator, a 10Ω resistor, and a Tektronix 2430A Digital Oscilloscope, as shown in Figure 4.1.2. Channel one of the oscilloscope was used to measure the voltage across the 10Ω resistor. This voltage was used to calculate the current through the device. Channel two of the oscilloscope was used to measure the output voltage of the pulse generator. Subtracting the voltage from channel one from the voltage from channel two yields the voltage across the device. For this measurement only two probes were used across the sample. Knowing the current through the device and the voltage across the device, the IV curve can be plotted and the mobility can be calculated.
4.2 Device Structure

It is critical that devices for measuring mobility using SCLC be grown very carefully. Figure 4.2.1 shows the device structure of the n-i-n devices. The substrate for all of the devices was stainless steel. On top of the stainless steel was an ECRCVD deposited n+ layer, doped with phosphine. Above the bottom n+ layer, a thin undoped amorphous silicon...
layer is deposited. Immediately after the amorphous silicon layer the gas flow is changed to a very high dilution ratio of hydrogen to silane. This causes rapid nucleation to occur and the grains begin to grow. The layer where rapid nucleation takes place is known as the seed layer. Grains grow in a conical geometry, starting out very small and growing upward and outward in a conical fashion [18, 13]. This makes the top of the layer representative of the largest grain size. Over a period of about 10 minutes the hydrogen flow is decreased slowly to the final hydrogen flow, which will be used for the intrinsic layer deposition. If this type of seed layer is not used the silicon does not crystallize quickly enough and the measured mobility will be dominated by the mobility of the amorphous layer between the n+ layer and the intrinsic nanocrystalline silicon. Vetterl has shown that grading the hydrogen to silane ratio from high dilution to lower dilution can create nanocrystalline layers as thin as 10nm [22]. All of the intrinsic nanocrystalline silicon is unintentionally doped n-type due to impurities, such as oxygen, in the chamber [23]. After deposition of the i-layer, the device is transferred to the ECRCVD reactor to have the top n+ layer grown on it. Special care must be taken when transferring a device between reactors to ensure an oxide layer does not form [15]. These considerations were previously addressed in Section 2.4.
4.3 Results

Using SCLC to calculate the mobility of a nanocrystalline semiconductor yields a mobility value that is the minimum possible mobility for the material [24]. This must be the minimum value since there are many places in the devices that can reduce the effective mobility below the value of the actual mobility in the nanocrystalline silicon layer. The mobility could be affected by a thin oxide layer between either of the n+ layers and the intrinsic layer, as shown in Figure 4.2.1. Oxide layers can form immediately once a sample is removed from the reactor due to moisture in the air and the porosity of large grain nanocrystalline samples [25]. For this reason, Raman measurements were not performed on many of the n-i-n devices and substrates had to be either transferred from one reactor to another as quickly as possible or etched in buffered oxide etch before being loaded into the reactor. To perform Raman measurements an i-layer was deposited, using the same parameters as another n-i-n device, on top of a standard bottom n+ layer and then measured. Problems can be encountered if the thin undoped amorphous silicon layer that is deposited on top of the bottom n+ is too large. If the amorphous layer is too large, the mobility of that layer will dominate and the measured mobility will reflect that of the amorphous silicon. The growth parameters and thicknesses of the undoped amorphous silicon layers are shown in Table 4.3.1.

To crystallize the nanocrystalline silicon layer quickly a seed layer is deposited by starting with a very high hydrogen to silane dilution ratio and rapidly grading the hydrogen down to the deposition quantity over a period of about 10 minutes. The starting dilution ratio for the seed layers was 22.4. At the end of the seed layer the dilution ratio was the ratio used for the deposition of the bulk of the i-layer. If a seed layer is not used the nanocrystalline
number of growth filament
time thickness pressure sih4
of rate temp
filaments (a/s) (min) (um) (mT) (OC) (seem)
2 3.48 1 0.02 5 1915 12.04
2 3.48 3 0.06 5 1915 12.04
1 3.58 1 0.02 5 1915 12.04
1 3.58 3 0.06 5 1915 12.04

Table 4.3.1. Growth parameters and thicknesses of intrinsic a-Si layers

layer does not crystallize quickly enough and amorphous silicon deposited at the start of the deposition can dominate the mobility. Another part of the device that can negatively affect the measured mobility is the top contact. If the contact is not ohmic, then the current flow through the device is significantly lower at small electric fields. Once again this will yield a much lower measured effective mobility. Experiments were done with the top n+ layers and top contact materials to find a combination that reliably provides an ohmic contact to the device. The best contact was made by depositing a thin layer of n+ amorphous silicon, then a thin layer of n+ amorphous germanium (1 in Table 4.3.2), and finally aluminum. Contacts made using a thin layer of n+ amorphous (2 in Table 4.3.2) or nanocrystalline silicon (3 in Table 4.3.2) and aluminum also formed ohmic contacts. Growth parameters for the various n+ layers are shown in Table 4.3.2.
<table>
<thead>
<tr>
<th>Layer</th>
<th>Time (min)</th>
<th>Temp (°C)</th>
<th>Pres (mT)</th>
<th>Power (W)</th>
<th>H₂ (sccm)</th>
<th>GeH₄⁺</th>
<th>SiH₄ (sccm)</th>
<th>PH₃⁺ (sccm)</th>
<th>Thickness (µm)</th>
</tr>
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<tbody>
<tr>
<td>a-Si</td>
<td>5</td>
<td>326</td>
<td>10</td>
<td>6.03</td>
<td>60</td>
<td>0</td>
<td>15.6</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>a-Ge</td>
<td>2</td>
<td>326</td>
<td>10</td>
<td>6.03</td>
<td>60</td>
<td>3.6</td>
<td>0</td>
<td>10</td>
<td>0.07</td>
</tr>
<tr>
<td>a-Si</td>
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<td>326</td>
<td>10</td>
<td>6.2</td>
<td>60</td>
<td>0</td>
<td>15.6</td>
<td>25</td>
<td>0.05</td>
</tr>
<tr>
<td>a-Si</td>
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<td>6.26</td>
<td>60</td>
<td>0</td>
<td>15.6</td>
<td>75</td>
<td></td>
</tr>
<tr>
<td>nc-Si</td>
<td>25</td>
<td>326</td>
<td>5</td>
<td>6.85</td>
<td>100</td>
<td>0</td>
<td>SiH₄⁺</td>
<td>7</td>
<td>0.06</td>
</tr>
</tbody>
</table>

Table 4.3.2. Growth parameters and thicknesses of n⁺ layers

*Balance of gas is H₂

Each device displayed an increase in mobility with increasing temperature, as shown in Figure 4.3.1. This increase in mobility can be attributed to the grain boundaries in the nanocrystalline material. Between grains there are many traps that cause a rise, for an n-type material, in the conduction and valence bands, as shown in Figure 4.3.2. As the temperature increases, the thermionic transfer across the barrier height at each of the grain boundaries improves. This reduction in effective barrier height makes it easier for electrons to cross the barriers and move between grains, thus increasing the mobility. Traps at the grain boundaries play a major role in the effective mobility of the material [26].
For the same reason as mobility, resistivity of the sample decreases with an increase in temperature as shown in Figure 4.3.3. Carrier concentration would increase or decrease slightly with increasing temperature, depending on the sample. In most samples it did not change more than $\pm 3 \times 10^{14}$ with carrier concentrations between $10^{14}$ and $10^{15}$. For measurements that yielded a reasonable value for mobility the carrier concentration calculated using the mobility and resistivity was within a factor of two of the carrier concentration calculated using the transition voltage between ohmic and SCLC operation.
Figure 4.3.3. Resistivity versus temperature

The n-i-n devices that were fabricated had approximately the same grain size for <111> oriented grains, however the size of the <220> oriented grains varied from about 15nm to 50nm. Growth parameters and measured properties of the devices can be found in Appendices A and B respectively. Data collected from this series of n-i-n devices shows that the mobility increases as the <220> grain size increases. Figure 4.3.4 shows the mobility versus <220> grain size at 25°C for the three deposition methods. When examining these figures, remember that the value of mobility derived using the SCLC measurement technique is the minimum value and can be easily reduced by imperfections in the device. The mobility of devices grown using ECRCVD are much higher, .77-2 cm²/V-s for 6-8nm grains, for a given <220> grain size than those grown using HWCVD. This difference in mobility is due to interfacial layers, such as oxide layers, in the devices. As discussed previously, only i-layers were grown using HWCVD, so to deposit the two n+ layers the sample had to be
transferred between reactors. When transferring the sample between reactors there will always be some oxide layer that forms. The n-i-n samples that were grown using just ECRCVD were done in one deposition without being removed from the reactor. This ensures oxide layers will not form between layers, thus increasing the mobility.

![Graph](image)

**Figure 4.3.4.** Mobility of HWCVD devices versus <220> grain size at 25°C measured using the DC method

Mobility of devices also increased as the thickness of the device increased and the grain size was held approximately constant. An increase in mobility with increased sample thickness is reasonable. Since, the amorphous and seed layers deposited on the bottom n+ layer are about the same thickness for each device grown, the nanocrystalline region of the device must be thicker if the overall thickness is greater. If the nanocrystalline region is much thicker than the amorphous region, the measured mobility will be due more to the nanocrystalline region of the device than the amorphous or seed layers. Figure 4.3.5 shows mobility versus layer thickness.
Measurements performed using the pulsed method yielded mobilities that were much smaller than the measured DC mobilities. Figure 4.3.6 shows the measured IV data for a sample using the pulsed measurement technique. Figure 4.3.7 shows the measured IV data for the...
same sample using the DC technique. The data shows that using the pulsed technique allows the sample to be measured at higher currents without deviating from the $V^2$ characteristic. Figure 4.3.8 shows the $IV^2$ curve that deviates from the $V^2$ characteristic caused by what is believed to be sample heating.

To collect more accurate data using the pulsed measurement setup, a couple improvements need to be made to the apparatus. Instead of measuring the voltage dropped across a resistor and calculating the current, the resistor could be removed from the circuit and a current probe could be used to directly measure the current through the device. To reduce the contact resistance and more accurately determine the voltage across the device a differential probe setup could be used on the oscilloscope. This system would allow a measurement to be made with a similar configuration to the DC measurement with one probe on the top contact and two probes on the substrate, one for driving current and one for measuring voltage. By making these improvements to the apparatus a significant amount of parasitic resistance could be removed from the circuit, the current through the device would be known more accurately, and the voltage measured across the device would be more
Figure 4.3.8. Deviation from $V^2$ characteristic caused by sample heating from power dissipation using the DC technique

accurate. Reducing the parasitic resistance is important especially at high currents, where a significant amount of voltage can be dissipated across the parasitic resistances. Making these improvements, especially more accurately measuring voltage and current across the device, would be likely to increase the measured mobility significantly.
5. CONCLUSIONS

The objective of this project was to develop a method for measuring mobility of nanocrystalline semiconductors in the vertical direction of the material, not the lateral direction like Hall Effect measurements yield. To achieve this, a process for fabricating n-i-n devices that yield the mobility of the nanocrystalline layer by measuring SCLC was developed. Once the devices were fabricated, a method for accurately testing each device had to be developed.

In order to make devices that yield a reasonable measured mobility value, care must be taken when preparing the sample. Anytime the sample is transferred from one reactor to another the sample must be either stored in methanol and then etched with Buffered Oxide Etch (BOE) prior to loading or directly unloaded from one reactor and loaded into the next to prevent an oxide layer from forming. As shown by the high measured mobilities of the ECRCVD samples, it is best to deposit all three layers of the device without removing it from the reactor. At the start of the i-layer deposition, the amorphous silicon layer must be kept as thin as possible and the nanocrystalline layer must be rapidly crystallized by using a very high hydrogen to silane dilution ratio and then grading the hydrogen down to the desire flow rate for the deposition. If there is an oxide layer or a thick amorphous layer in the device the mobility measured will be significantly decreased. Also, it is imperative to create ohmic contact to both n+ layers. The stainless steel substrate forms a good ohmic contact with the bottom amorphous silicon n+. To make an ohmic top contact a couple different materials could be used for the n+ layer. The two top n+ layers that worked were an amorphous silicon n+ layer and an amorphous silicon n+ layer with an amorphous germanium n+ layer deposited on top of it. Aluminum was determined to be the best material for making contact...
to the top n+ layer. This study also found that it is critical that the device be annealed at 150°C for at least 45 minutes. In addition to thermal annealing, the device must be annealed by driving a high current across the device until the resistance of the contact is no longer changing, at least 10 minutes.

In addition to proper fabrication methods, it is important to properly test each device and understand where the errors in the measurement can be introduced. Devices thicknesses were carefully measured and i-layer thicknesses were carefully derived from these measurements. SCLC measurements were performed using a three point probe system with 2 probes touching the substrate. Two probes were placed onto the substrate since there was a significant, 0.3Ω, contact resistance between it and the gold plated probes. When analyzing the measured IV curves, care was taken determining the voltage where the device transitions from ohmic to SCLC operation. Also, at higher DC currents, > 0.3 - 0.4A, the device would begin to heat up and the current versus voltage characteristic would diverge from the voltage squared characteristic. To eliminate the effects of heating due to power dissipation within the device, short voltage pulses can be used.

When devices are made and measured carefully using appropriate methods the mobility, carrier concentration, and resistivity of the semiconducting layer can be measured with reasonable accuracy. The results of this study demonstrated that mobility increases with grain size as expected, due to a reduction in the number of grain boundary barriers in the material [27]. For a given grain size the measured effective mobility increases with thickness. As expected for nanocrystalline semiconductors, mobility increases and correspondingly resistivity decreases, with temperature due to lowering of grain boundary barriers.
6. REFERENCES


ACKNOWLEDGEMENTS

Completion of this project took a great deal of effort and I could not have done it without help. I would like to thank everyone for their assistance with this project. First, I would like to thank Dr. Vikram Dalal for his guidance, funding, and the opportunity to perform this research. Next, I would like to thank Dr. Rana Biswas and Dr. Joseph Shinar for being on my committee.

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### APPENDIX A – N-I-N DEPOSITION PARAMETERS

<table>
<thead>
<tr>
<th>Sample</th>
<th>Temperature (°C)</th>
<th>Pres (mT)</th>
<th>Time (min)</th>
<th>Filaments * Tfil (°C)</th>
<th>I(A)</th>
<th># (scm)</th>
<th>H2 (scm)</th>
<th>SiH4 (scm)</th>
<th>a-Si Layer Deposition (min)</th>
<th>Top n+ Layer (Table 4.3.2)</th>
</tr>
</thead>
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<td>3/2004</td>
<td>326</td>
<td>10</td>
<td>170</td>
<td>1920</td>
<td>11.9</td>
<td>1</td>
<td>36</td>
<td>3.2</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>3/2006</td>
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<td>1</td>
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<td>3.2</td>
<td>3</td>
<td>2</td>
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</table>

**Annealed in 1 Torr, H2 and SiH4, 60min@275°C, 30min@300°C, 30min@325°C,**
**30min@350°C, 30min@375°C, 30min@400°C, 30min@425°C**

3/2043: 207 10 180 1920 23.8 2 48 4.3 1 1

**Annealed in 1 Torr, H2 and SiH4, 30min@350°C**

* All Filaments were 40cm long and made of Tantulum

---

### ECRCVD Deposited n-i-n Devices

<table>
<thead>
<tr>
<th>Sample</th>
<th>Temp (°C)</th>
<th>Pres (mT)</th>
<th>Time (min)</th>
<th>Power (W)</th>
<th>TMB**</th>
<th>H2 (scm)</th>
<th>SiH4 (scm)</th>
<th>a-Si Layer Deposition (min)</th>
<th>Top n+ Layer (Table 4.3.2)</th>
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</tbody>
</table>

TMB in graded layer

2/8857: 326 5.4 90 6.83 13 60 2.6 2 1

---

### VHF-PECVD Deposited n-i-n Devices

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<th>Pres (mT)</th>
<th>Time (min)</th>
<th>Power (W)</th>
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<th>H2 (scm)</th>
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<td>40</td>
<td>7.8</td>
<td>10</td>
<td>2</td>
</tr>
</tbody>
</table>

Seed layer doped with PH3 first 10min, then TMB

** TMB – 20 parts per million Trimethyl Boron, balance H2**
## APPENDIX B – N-I-N MEASURED PROPERTIES

<table>
<thead>
<tr>
<th>Sample</th>
<th>Thick (um)</th>
<th>Grains (nm)</th>
<th>Mobility (cm²/(V·s))</th>
<th>Resistivity (Ω·cm)</th>
<th>Carrier Conc. (cm⁻³)</th>
</tr>
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<td></td>
<td></td>
<td>&lt;111&gt;</td>
<td>25C</td>
<td>150C</td>
<td>(Equation 3.4.6)</td>
</tr>
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<td>HWCVD Deposited n-i-n Devices</td>
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APPENDIX C – MATERIAL PROPERTIES AND GROWTH CHEMISTRY OF NANCORystalline Silicon Films Used for Photovoltaic Devices

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Vikram L Dalal*, Jeff Leib*, Kamal Muthukrishnan*, D Stieler*† and Max Noack*†
* Dept. of Electrical and Computer Engr., Iowa State University
† Microelectronics Research Center, Iowa State University
Ames, Iowa 50011

ABSTRACT

We report on the growth chemistry and properties of nanocrystalline Si:H (nc-Si:H) films and devices grown using three different growth techniques – ECR plasma, VHF plasma and hot wire. It is found that the films grown using ECR plasma deposition are predominantly <111> oriented, whereas the orientation depends upon pressure, growth rate and ion bombardment in films grown using VHF plasma. Remote hot wire grown films also show both <111> and <220> orientations. It is also found that all the films are stressed, with both compressive and tensile stress being present in the same film. The stress depends upon the grain size. Stress can explain the shift in Raman peak from its nominal value of 520 cm⁻¹. Devices with good minority carrier diffusion lengths can be fabricated in both <111> and <220> materials. Electron mobilities are in the range of 0.5-1.0 cm²/Ns.

1Primary researcher performing XRD, Raman, and Hall effect measurements
INTRODUCTION

Nano Si:H is an important PV material [1-4]. A variety of techniques can be used to deposit the material. Among these are hot wire [5,6], ECR plasma [7,8] and VHF plasma techniques [1-3]. All three techniques have been shown to yield high quality devices with good fill factors (65-70%) and minority carrier diffusion lengths (>1 micrometer). However, the techniques seem to yield materials with distinctly different structures. In particular, it appears that orientation of the grain is very different between different materials, with the ECR material almost always showing <111> orientation, whereas the VHF plasma can yield materials with either <111> or <220> grains dominating. In this paper, we systematically study the impact of growth chemistry on the properties of materials deposited using various techniques. Both x-ray and Raman spectroscopy will be used to characterize the structure, and a careful examination of the x-ray spectrum will be used to deduce information about the stresses present in the various films. It will be shown that the stress levels are high in films with small grain sizes. We will also investigate the PV properties of these materials by making diagnostic devices in both ECR and VHF materials, the latter with varying grain orientations.

GROWTH CHEMISTRY

The films were grown using silane-hydrogen mixtures using either low pressure, high power ECR plasma [8], or with 45 MHz VHF plasma under varying pressure conditions. We have shown earlier [9] that in VHF growth, the pressure during growth plays a major role in determining whether a film turns crystalline or not. In this work, we further explore
influence of pressure on grain orientation and electronic and structural properties.

In Fig. 1, we show a typical x-ray spectrum for a nc-Si:H film deposited using VHF discharge at 100 mT. Note that there is a significant presence of both <111> and <220> grains. The influence of varying the deposition pressure on grain orientations is shown in Fig. 2. As the pressure increases, with hydrogen/silane ratio remaining constant, both the peak intensity and grain size of <220> grains increases relative to <111> grains. We know from the previous work [9] that higher pressures lead to lower ion flux. At the same time that the grain orientation changes to <220>, the growth rate also increases. See Fig. 3. These are very remarkable results; what they are suggesting is that the natural growth mechanism for the film is <220>, given the large surface energy of a (220) plane. However, when significant hydrogen ion bombardment is present, random nucleation which includes <111> grains, takes place. Thus, excessive hydrogen etching can actually lead to a film with smaller grains! Clearly, the role of hydrogen is very complicated in the growth of nc-Si:H. Too little hydrogen or too low a flux
of H ions leads to amorphous films [9]. On the other hand, too much hydrogen or too much ion bombardment leads to smaller grains and random grain orientations.

In Fig. 4, we show the results of x-ray spectra of films deposited using our remote hot-wire system [10]. In contrast to other groups, our hot filament is far away from the substrate (11 cm), thereby minimizing the influence of hot filament on substrate heating. Once again, both <111> and <220> grains are present! Now there are no ions in the reactor, but from other experiments, it appears that as the hydrogen dilution increases, the ratio of peak intensities of <111> relative to <220> increases, and grain size decreases!

Thus it appears that too many hydrogen radicals or ions cause a random orientation in the film, and also reduce the grain size. These results are very similar to the results for nc-Ge:H films, reported elsewhere in these proceedings [11].
STRESS IN NC-SI:H FILMS

By making a careful x-ray measurement, one finds distinct satellite peaks around both <111> and <220> grains. See Fig. 5. Notice that the satellite peaks are in different directions; for the <111> grain, the peak indicates a tensile stress, and for <220>, a compressive stress. This is a very remarkable result! The same film is under both tension and compression. How can it be? The reason it can be is because of the presence of a thin amorphous tissue at the grain boundaries. The tissue can bond to <111> grain and put it under tension, and a <220> grain, and put it under compression. Clearly, if this is the case, the amount of stress must be a function of grain size; it is. Smaller the grain, larger both tensile and compressive stresses. See Fig. 6.

Fig. 5 Extended x-ray diffraction spectra for a VHF nc-Si:H film, showing the presence of satellite peaks in both <111> (top figure) and <220> (bottom) grains in the same film. The satellite peaks are related to the presence of stress in the film. <111> is tensile, and <220> is compressive.
ELECTRONIC PROPERTIES

We have shown earlier that good PV devices can be made in both ECR and VHF deposited films [8, 12].

Here we report on the electronic properties such as mobility and diffusion lengths. Mobility was measured using a Hall apparatus with a high signal/noise ratio achieved using coupled electrometers and triax cabling. In Fig. 7, we show the Hall mobility for a film with a grain size of 12 nm vs. temperature.

As expected, the mobility increases with temperature; a more surprising result we found was that the carrier concentration also seems to be increasing with temperature.

We ascribe this latter result to the thermal emission of carriers from the deep traps at the grain boundaries, particularly in the a-Si tissue.
We also measured diffusion lengths of minority carriers (holes) in both \(<111>\) and \(<220>\) oriented materials. The diffusion length was measured using the QE vs. voltage and capacitance vs. voltage techniques described earlier [12]. The results for QE vs. depletion width for films with dominant \(<111>\) orientations were reported earlier [12]. Fig. 8 shows the data for relative QE vs. depletion width for a VHF film with a larger \(<220>\) grain than \(<111>\), with a doping density of \(\sim2\times10^{16}/\text{cm}^3\). The hole diffusion length is about 0.37 micrometer, somewhat larger than reported for the \(<111>\) oriented films earlier. This result may be related to larger grain size in this film. Quite clearly, reasonable diffusion lengths can be obtained in both types of materials. The intercept indicates a diffusion length of \(\sim0.36\) micrometer. The film had a doping of \(2-3\times10^{16}/\text{cm}^3\).

On the other hand, when we made films with a much higher degree of crystallinity (much less amorphous phase as determined by the Raman ratios of crystalline and amorphous phases), we discovered that films with very high crystallinity had smaller diffusion lengths (\(\sim0.1-0.2\) micrometer). Clearly, the amorphous tissue plays a role in passivating the grain boundaries.

![Fig. 8 Relative QE vs. depletion width Wd in a p+nn+ device, grown at 100 mTorr pressure in a VHF discharge.](image-url)
CONCLUSIONS

In summary, we have shown that the growth chemistry significantly impacts the structure of the material, including fundamental properties such as grain orientations and growth rates and stress in the film. We have also shown that excessive etching by hydrogen seems to be undesirable, and that it can lead to smaller grains. It appears that the presence of amorphous tissue in the material is necessary for efficient grain boundary passivation.

ACKNOWLEDGEMENTS

This work was partially supported by a grant from NSF and a contract from NREL. We also thank Keqin Han, Durga Panda and Xuejun Niu for help with device fabrication and measurements.
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APPENDIX D – GROWTH CHEMISTRY OF NANOCRYSTALLINE SI:H FILMS

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Vikram L. Dalal, Kamal Muthukrishnan, Daniel Stieler\(^1\) and Max Noack
Dept. of Electrical and Computer Engr. and Microelectronics Research Center
Ames, Iowa 50011, USA

ABSTRACT

We report on the growth of nanocrystalline Si:H films using both plasma CVD and remote hot wire deposition under systematically varied growth conditions. The films were grown from mixtures of silane and hydrogen. It was found that when the films were grown under low pressure VHF plasma growth conditions, the orientation of the film changed as the pressure increased. At the lowest pressures, the films were mainly \(<111>\) oriented, but changed to \(<220>\) orientation as the pressure increased. The grain size increased as the growth temperature increased. When the films were grown using remote hot wire deposition, the orientation depended upon both hydrogen dilution and growth temperature. As the hydrogen dilution increased, the \(<220>\) grain size became smaller. Grain size as large as 36 nm was obtained by controlling the growth conditions in hot wire deposition. As the growth temperature increased, the size of \(<220>\) grains increased. Growth rates also increased with increasing temperature. The data can be explained by invoking a growth model which

\(^1\)Primary Researcher performing XRD and Raman measurements
recognizes that the natural growth direction for Si is $<220>$, since the surface energy is highest for (220) plane. Random nucleation leads to $<111>$ grains. Bonded H is believed to inhibit the growth of $<220>$ grains.

INTRODUCTION

Nanocrystalline Si:H [nc-Si:H] is an important electronic and optical material, widely used for solar cells, image sensors and thin film transistors [1-5]. There are several methods for depositing nc-Si:H, among the most popular being PECVD, either at 13.5 MHz or at higher frequencies (40-100 MHz) [1], ECR plasma CVD [6,7], and hot wire deposition [8,9]. Most of the groups in the world use VHF plasma deposition, since it produces a plasma with lower energy ions. The films are typically grown under high hydrogen dilution (20:1 or greater), with lower dilutions leading to mixed phase or amorphous materials [1]. Most of the films deposited using VHF plasma have predominantly $<220>$ orientation, though under very high hydrogen dilution, the film structure changes to primarily $<111>$ orientation [1]. Typical grain sizes are in the 10-15 nm range. The films typically show a strong Raman peak at 520 cm$^{-1}$, with an amorphous shoulder in the 480 cm$^{-1}$ range.

In recent work [10], we have shown that the crystallinity of the film is a strong function of pressure in a VHF plasma reactor operated at 45 MHz. We showed there that the films grown primarily at low pressures (50 mTorr) required much less hydrogen for crystallization than films grown under higher pressure conditions. In this paper, we extend that work to examine the crystallinity and grain orientation as functions of pressure in the reactor, growth temperature and hydrogen dilutions. We also examine films grown using a remote hot wire deposition technique, where the hot filament is 11 cm away from the
substrate, and therefore, substrate heating from the filament is minimized [11]. This is an important consideration, since we will show that increasing the temperature of the substrate can have significant impact on both grain orientation and grain size.

**EXPERIMENTAL TECHNIQUES**

The PECVD films were grown using a 45 MHz plasma in a simple diode reactor. Most of the results reported here are for films grown on stainless steel substrates so as to correspond to device work. All the films had a thin (~100 nm) a-Si tissue layer grown first, so as to allow for a reproducible template to grow the nanocrystalline films. The total film thicknesses were in the range of 1000 nm. The films were grown from mixtures of silane and hydrogen. The films were grown under reactor pressure in the range between 25 mTorr to 500 mTorr. The hot wire films were grown using a single Ta filament heated to 2100 °C.

The films were characterized for their structure using Raman spectroscopy using a Renishaw Raman microscope using the 488 nm line from an Ar laser at low power so as to not heat up the sample. The samples were also measured for grain size using x-ray diffraction and applying Scherer’s formula.

**RESULTS ON PECVD DEPOSITED FILMS**

In Fig. 1, we show the results from Raman spectroscopy of a typical PECVD nc-Si:H film grown with a growth temperature of 280 C and deposition pressure of 50 mTorr. The results show a sharp peak at 520 cm⁻¹ and a small amorphous shoulder at 485 cm⁻¹. The results show a relatively high ratio (4:1) between crystalline and amorphous films. In Fig. 2,
we show the x-ray spectrum for this film. Both $<111>$ and $<220>$ peaks are seen to exist. In Fig.3, we plot the ratio of $<220>/<111>$ intensities as a function of pressure. In Fig.4, we plot the grain sizes deduced from x-ray diffraction as a function of deposition pressure. It is seen that as the pressure increases, under otherwise identical growth conditions, $<220>$ grain size increases, while $<111>$ decreases, and the ratio of $<220>$ intensity to $<111>$ intensity also increases. Thus, the primary orientation of the film is changing from $<111>$ to $<220>$ as the pressure increases.
In Fig. 5, we plot the grain size as a function of growth temperature, showing an increasing grain size with temperature.

RESULTS ON HOT WIRE DEPOSITED FILMS

In Fig. 6, we show the x-ray diffraction spectrum for nc-Si:H films deposited using the remote hot wire system described above. The films were grown at a pressure of 5 mTorr, corresponding to a (pd) product of 55 mTorr-cm. Once again, both <111> and <220> features are evident in the film. In Fig. 7, we plot the grain size as a function of hydrogen dilution. It is seen that as the hydrogen dilution increases, there is a pronounced decrease in <220> grain size and a smaller increase in <111> grain size. In Fig. 8, we show what happens when the growth temperature is increased. It is seen that the <220> grain grows with increasing temperature, but the size of <111> grain does not change much. In Fig. 9, we show what happens to the different grain sizes and intensities as the deposition pressure changes. It is seen that as the pressure increases, the <220> grain size and the relative ratios
of intensities increases, at least up to 20 mT. The increase in grain size is quite pronounced at the lowest pressures (pd products). At 30 mTorr, the grain size for <220> suddenly decreases. We noticed on this sample from Raman spectra that the Raman ratio of crystalline to amorphous peaks also decreased at this pressure, so perhaps the material is not as crystalline at these highest (pd) products. We need further investigation of this higher (pd) product range before we can draw definitive conclusions about what is happening at the highest pressures investigated.
Note that when we used multiple filaments to grow the films, we obtained much larger grain sizes, as large as 36 nm. We are still continuing this work in detail, and therefore will not report the details here.

DISCUSSION OF RESULTS

From both PECVD data and hot wire data, we see that as the growth temperature increases, the size of the <220> grain increases. From both data sets, we also see that increasing pressure seems to lead to increasing grain sizes. We also see from hot wire data that the high hydrogen dilutions lead to lower <220> grain sizes.

These are remarkable results, which are providing valuable insight into the growth mechanisms of nc-Si:H films. From thermodynamic considerations, one can deduce that the preferred grain orientation should be <220>, since the (220) plane has a higher surface energy than the (111) plane in Si. The <111> Grain probably arises from random nucleation. When conditions are thermodynamically favorable, e.g. when temperatures are higher, the <220> grain begins to grow more rapidly. Thus one gets both a larger grain size and a preferred <220> orientation. If temperatures are low, there is significant bonded H in the lattice, and this bonded H inhibits the natural growth of <220> grain, but allows the randomly nucleated <111> to grow. At the lowest pressures, the higher H ion and/or radical flux impinging on the substrate inhibits the growth of <220> in both systems.

If the above reasoning is true, one should find some very interesting results when one studies the growth of nc-Ge:H. Ge-H is a much weaker bond than Si-H. Therefore, at a given growth temperature (e.g. 250 C), the nc-Ge:H film should be dominated by the <220> grain, and the grain size should be much larger than in nc-Si:H. That is exactly what we find
Therefore, we conclude that this model for the growth of nc-Si:H films appears to be consistent with all the experimental data for both Si and Ge films.

CONCLUSIONS

In summary, we have shown that the deposition conditions in both PECVD and hot wire growth have significant influence on the fundamental structure of the films. The natural growth direction for the films appears to be <220>, and bonded H (and perhaps, excessive ion bombardment) appear to inhibit the growth of <220> grains. By controlling growth conditions, one can obtain larger grains. The largest grain size obtained was 36 nm at a growth temperature of 280 °C.

ACKNOWLEDGEMENTS

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APPENDIX E – ELECTRON MOBILITY IN NANOCRYSTALLINE SILICON DEVICES

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Daniel Stieler*1, Vikram L Dalal*#, Kamal Muthukrishnan*, Max Noack+ and Eric Schares*

*Dept. of Electrical Engineering and Microelectronics Research Center
+ Microelectronics Research Center
Iowa State University
Ames, Iowa 50014
#corresponding author: email: vdalal@iastate.edu

ABSTRACT

Electron mobility in the growth direction was measured using space charge limited current techniques in device-type n-In nanocrystalline Si:H and nanocrystalline Ge:H structures. The films were grown on stainless steel foil using either hot wire or remote plasma enhanced chemical vapor deposition (CVD) techniques. Grain size and crystallinity were measured using x-ray and Raman spectroscopy. The size of grains in films was adjusted by changing the deposition conditions. It was found that large <220> grain sizes (~ 56 nm) could be obtained using the hot wire deposition technique, and the conductivity mobility at room temperature was measured to be 5.4 cm²/V-s in films with such large grains. The plasma-grown films had smaller grains and smaller mobilities. The mobility was

1 Primary Researcher and Co-author.
found to increase with increasing grain size and with increasing temperature.

Nanocrystalline Silicon (nc-Si:H) is an important material for photovoltaic devices and thin film transistors (TFT)\textsuperscript{1-4}. An important property for device applications is the carrier mobility. Generally, the mobility is measured using Hall effect techniques\textsuperscript{5}, or in thin film transistor devices, using the transistor current vs. gate voltage techniques\textsuperscript{2}. Mobility measured using either Hall effect or TFT devices measures a transverse mobility. Also, TFT devices yield values of mobility in a surface channel, which may not be representative of the bulk layer. The mobility in TFT devices may also be representative of the bet mobility, since in a material in which crystallinity is changing with thickness, the electrons may get channeled into the lowest gap state, viz, the most crystalline layer. In contrast, the performance of photovoltaic devices is dependent upon mobility in the bulk layer in the vertical or growth direction and the electrons and holes have to travel through materials with varying crystallinity. Note also that for both TFT and Hall effect measurements, the materials are grown on insulating (e.g. glass) substrates. In contrast, the photovoltaic devices are grown on conducting (e.g. steel or tin oxide) substrates\textsuperscript{1,6}. It is known that the substrate can have a significant influence on the morphology and structure of the subsequent film, and that the transport properties (e.g. diffusion lengths of holes) in the transverse direction may be very different from the properties in the growth direction\textsuperscript{7}. Therefore, it would be useful to measure the bulk conductivity mobility of carriers in the vertical or growth direction in device-type structures which are deposited on the same substrate as devices using the same growth techniques as used for photovoltaic devices. Recently, hole mobility in nc-Si:H devices were measured using time of flight techniques\textsuperscript{8}. In this paper, we report on a measurement of electron mobility in nanocrystalline Si:H device type structures using a different technique.
The technique used for the measurement was space charge limited current (SCLC). The device structure was \( n^+nn^+ \) type, with space charge injection limited to electrons. It is known from the theory of SCLC\(^9\) that once the current is controlled by the space charge, the current density is given by \( J = 1.12 \epsilon \mu V^2/L^3 \), where \( V \) is the applied voltage, \( L \) is the length of the \( n \) type layer, \( \mu \) is the mobility and \( \epsilon \) is the dielectric constant. Since we know all the other parameters, the mobility can be calculated by plotting \( J \) vs. \( V^2 \).

The samples were grown using either a remote hot wire deposition technique\(^{10}\) or plasma growth techniques using either electron-resonance (ECR) plasma\(^{11}\) or VHF diode plasma\(^1\). Most of the devices in this work were made using the remote hot wire technique. Remote hot wire refers to the fact that unlike most hot wire depositions, in our system, the hot Ta filament is \(~12 \text{ cm} \) away from the substrate, thereby reducing significantly the radiant heating effect of the filament upon the substrate. In our system, the measured substrate temperature changes by only about 10-20 °C during growth. The ECR plasma CVD growth system has been described previously\(^{11}\). All the devices were of \( n^+nn^+ \) type on stainless steel substrates, with \( n^+ \) layers being amorphous Si. Top contacts were evaporated Al films, which were annealed at 170 °C for 30 min to form good ohmic contacts. In addition, a high current was passed before the measurement to allow Al to diffuse through any surface oxide layer. The bottom \( n^+ \) layer was 0.25 micrometer thick, whereas the top \( n^+ \) layer was 0.06 micrometer thick. The bottom layer was deliberately kept thicker so as to induce crystallinity in the nanocrystalline layer grown on it and to prevent shorts. The thickness of the nanocrystalline \( n \) layer (which was not intentionally doped but was nevertheless doped \( n \) type because of the inevitable presence of oxygen\(^{12}\)) was varied between 0.5 micrometer and 1.8 micrometer, with most measurements done on films with \( n \) layer thicknesses of \(~1.2-1.5 \) micrometer. Care was taken to induce rapid crystallinity in the nanocrystalline layer by
using a very high hydrogen dilution during the initial stages of growth of this layer and then rapidly (over ~ 5m minutes) grading the hydrogen content down to that required for the main body of the nanocrystalline layer. If such rapid crystallization is not done, there will be a significant thickness of amorphous layer in series with a higher conductivity crystalline layer, and the mobility values will represent that of a-Si and not crystalline Si. Typical growth rates for the nanocrystalline film were ~1-2 Å/s. For hot wire deposited films, the initial hydrogen/silane ratio was 50:1, and the final ratio was 11.5:1. n+ doped amorphous Si:H can be used as electron injecting contact because of the close match between the conduction bands of amorphous and crystalline Si. The doped and undoped layers were deposited in different reactors to minimize any cross-contamination induced doping of the n layer. During SCLC measurements, care was taken to not heat up the sample by using a pulse technique at the highest currents. Care was also taken to take account of the inevitable series resistance effects in probes (~0.5 ohms) by using 4 point probe techniques.

The structure of the films was measured using x-ray diffraction and Raman spectroscopy. Grain sizes could be changed by changing the deposition conditions, for example growth temperatures or silane/hydrogen ratios. In Fig. 1, we show the x-ray spectrum of a film deposited using hot wire deposition. Both <111> and <220> grains are present, though the <220> grain dominates. The grain size of the <220> grain is quite large, 56 nm. The corresponding Raman spectrum is shown in Fig.2, showing a high ratio (4.2:1) between the crystalline peak at 520 cm⁻¹ and the amorphous shoulder at 490 cm⁻¹, implying >80% crystallinity.
In Fig. 3A, we show the typical I vs. $V^2$ curve at a measurement temperature of 25 °C for the sample whose Raman and x-ray spectra were shown in earlier figures. Except for the initial region, where the curve is ohmic (See Fig. 3B), the current follows the $V^2$ behavior predicted for SCLC. From the slope, we deduce a mobility of 5.4 cm$^2$/V-s.

Using this value of mobility, from the ohmic region, we deduce a carrier concentration of 2.5x10$^{14}$/cm$^3$ and a Fermi level position of ~0.3 eV below the conduction band, assuming the usual value for the effective density of states for the conduction band of Si. From the curve, the transition from ohmic to SCLC occurs at ~0.8 V. Using the equation for transition voltage for SCLC$^8$, $V = qNdL^2/\epsilon$, this voltage implies a combined trap and carrier concentration of 1.5x10$^{14}$/cm$^3$, in the same range as obtained from the ohmic region of I-V curve. Thus, the results are self consistent for this sample and for every sample reported here. Note that the traps are known to be about 0.35-0.5 eV below the conduction band$^{13}$. Therefore, almost all the traps are filled with electrons at this temperature for this sample.

Since the traps are mostly filled, we only get two regions in I-V curve, an ohmic region and a
SCLC region, and not a third, almost abrupt transition region from trap controlled to trap-free limit case\textsuperscript{9}.

![Figure 3. Plots of current vs voltage (left figure) and current vs. square of voltage (right figure). The mobility is estimated from the I vs. V\textsuperscript{2} plot. The transition point in the curve indicates a changeover from ohmic to square law behavior, and gives an estimate of the native doping in the material.](image)

In Fig. 4, we plot the mobility derived from SCLC vs. the grain sizes measured using x-ray diffraction. As expected the mobility increases with grain size, with the smallest mobilities being in samples grown using ECR plasma-CVD processes, where the grain sizes are very small (~9-10 nm). Note also that the minimum electron mobility in nc-Si:H when the grains are very small is around 1 cm\textsuperscript{2}/V-sec, which makes sense since the electron mobility in a-Si:H is also ~ 1 cm\textsuperscript{2}/V-sec.

To compare our data with mobilities measured using Hall measurements, we measured the mobility of electrons in a nc-Ge:H nin device prepared using the ECR growth technique. The grains were predominantly <220> oriented with a size of 22 nm. The measured electron mobility was

![Figure 4. Electron mobility vs. grain size.](image)
1.1 cm²/V-sec. This value agrees well with mobility in nc-Ge:H films with similar grain sizes, measured using Hall effect.

Note that the mobility values measured here represent an average over thickness for the sample, because it is known that the grain sizes increase with thickness, even when one maintains the same hydrogen/silane ratios during growth. That is one of the reasons why approximately the same thickness was used for most of the samples.

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