A high speed data recovery circuit with lead/lag phase detection

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A high speed data recovery circuit with lead/lag phase detection

by

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A thesis submitted to graduate faculty
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

Major: Computer Engineering

Major Professor: Randall L. Geiger

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Ames, Iowa

2000

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Graduate College
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This is to certify that the Master’s thesis of
Mezyad M. Amourah
has met the thesis requirements of Iowa State University

Signatures have been redacted for privacy
To my parents
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ABSTRACT

A Phase/Frequency Detector (PFD) that has a simple structure and a fast response is presented. This PFD has three signal inputs and no dead zone. The absence of the dead zone reduces an important component of the jitter. An implementation of this PFD in a clock recovery circuit is also presented. A data recovery architecture that uses this fast clock recovery circuit is described. A clock recovery circuit that operates at 1GHz in a 0.6u CMOS N-Well process is discussed.
CHAPTER 1. INTRODUCTION TO PHASE LOCKED LOOPS AND PHASE /FREQUENCY DETECTORS

This chapter reviews basic principles of operation and applications of phase locked loops (PLL's) and identifies the increasing demand on high speed high performance PLL's. The basic architecture of the PLL, and several different phase/phase frequency detector (PD, PFD) structures are discussed. Finally previous work in this field will be reviewed.

1.1 Phase locked loop applications and advantages

Several systems in communications and other fields employ Phase Locked Loops (PLLs) or similar circuits to generate clock signals, or to recover or regenerate clock signals from received waveforms. In integrated systems timing signal generation, detection, and distribution circuits may occupy a significant part of the overall die area. Phase Locked Loops (PLLs) and Delay Locked Loops (DLLs,) find wide applications in areas such as frequency and phase modulation systems, data transmitters, data receivers, electronic drives for data storage devices, and microprocessor systems [1], [2]. PLLs, and DLLs are used to solve several problems in the areas of communication, data transmission, and data storage. These problems include jitter reduction, clock skew suppression, frequency synthesis, and clock recovery. In the recent years the demand for high speed of operation has increased for the I/O interfaces, video, audio, and graphics processors. PLLs and other timing circuits are
highly sensitive to noise and interference [21]. Higher speeds require better performance from the overall timing recovery PLL. [3], [10] in high-speed communication applications.

1.2 Basic phase locked loop (PLL) architecture

Most Phase Locked Loop (PLL) circuits use the basic architecture shown in Figure 1.1. The components include a phase detector (PD) or phase/freq. Detector (PFD), a loop filter, and a voltage controlled oscillator (VCO). There are many variations for the implementation of these components. The detector, PD or PFD, has two inputs and produces an output signal that is proportional to the phase difference or phase and frequency difference between the two input signals. The loop filter, typically a lowpass filter (LPF), is used to filter the signal coming from the phase detector. The output of the loop filter becomes the control voltage for the VCO. The voltage controlled oscillator (VCO) produces an output signal with a frequency dependent upon and ideally linearly proportional to the control voltage at its input. The exact analysis of a PLL is difficult because it is a time varying and

![Figure 1.1 PLL basic architecture](image-url)
non-linear system. A small signal-analysis based upon on the assumptions that the circuit is initially locked and stable, then a small change in the input signal phase or frequency occurs is described in several publications. The assumptions mentioned above are made to be able to deal with the PLL as a linear and time invariant system. A basic PLL is shown in Figure 1.1.

A difference between the input signal phase and the oscillator output phase will produce an error voltage at the output of the phase detector equal to

\[ V_{\text{error}}(s) = K_{pd}(\theta_{in}(s) - \theta_{out}(s)) \]  

(1.1)

where the constant \( K_{pd} \) is the phase detector gain. The output frequency of the VCO is given by

\[ f_{out} = f_c + K_{VCO} \cdot V_{\text{ctrl}}(s) \]  

(1.2)

where \( f_c \) is the free running frequency of the VCO with zero control voltage where \( V_{\text{ctrl}}(s) \) is the output of the loop filter, and the constant \( K_{VCO} \) is the VCO gain or sensitivity

\[ K_{VCO} = \frac{d\omega}{dV_{\text{ctrl}}} \]  

(1.3)

where \( \omega \) is the angular frequency of oscillation of the VCO. Since the angular frequency is the derivative of the phase, if we take the Laplace transform of the integral of Equation 1.3 the oscillator output phase will be

\[ \theta_{out}(s) = \frac{K_{VCO}}{s} \cdot V_{\text{ctrl}}(s) \]  

(1.4)

For a loop filter with the transfer function \( F(s) \), the closed loop transfer function for the PLL, shown in Figure 1.2, is
If the loop filter is of first order, the PLL will be second order. The quantity \( K = K_{\text{vco}} \cdot K_{\text{pd}} \) is called the loop gain and is expressed in rad/sec. [1], [2].

\[
H(s) = \frac{\theta_{\text{out}}(s)}{\theta_{\text{in}}(s)} = \frac{K_{\text{vco}} K_{\text{pd}} F(s)}{s + K_{\text{vco}} K_{\text{pd}} F(s)} \tag{1.5}
\]

1.3 Phase and frequency detectors

Many PLL parameters including the tracking range, acquisition range, loop gain, and transient response depend on the properties of the phase and frequency detectors [1], [2]. What we have interest in are the following properties of the phase detectors:

1) What is the input phase difference range for which the transfer characteristic of the phase detector is monotonic.

2) What is the response of the PFD to unequal input frequencies.

3) How do the input amplitude and duty cycle affect the characteristics.

Following is a short discussion for some of the more popular phase/frequency detectors.
**Multiplier (XOR gate)**

The multiplier has been used in analog circuits as a phase detector in carrier recovery and in Frequency Modulation (FM) systems [5], [6]. For a sinusoidal input signal
\[ x_{in} = V_{in} \cos(\omega t + \theta_{in}) \]
if we have a local oscillator with the signal
\[ x_{lo} = \cos(\omega_1 t + \theta_{lo}) \]
then the output of the multiplier that multiplies the two input signals will be
\[
V_{out} = \frac{1}{2} V_{in} \sin(\theta_{in} - \theta_{lo}) + \frac{1}{2} V_{in} \sin(2\omega_1 t + \theta_{in} + \theta_{lo})
\]  

(1.6)

Using a low-pass filter (LPF) to remove the high frequency component, we end up with
\[
V_{out} = \frac{1}{2} V_{in} \sin(\theta_{in} - \theta_{lo})
\]  

There are several implementations of analog multipliers; one common implementation is the Gilbert multiplier. A MOS transistor-level circuit realization of the Gilbert multiplier is shown in Figure 1.3 [2]. If \( v_1 \) and \( v_2 \) are two-valued bipolar functions with \( v_1^- = -v_1^+ \) and \( v_2^- = -v_2^+ \) it follows that multiplication of these two excitations is also two-valued and this two-valued function that implements the exclusive

![Figure 1.3 Implementation of Gilbert multiplier](image-url)
or (XOR) function. The XOR gate phase detector has the characteristic curve shown in Figure 1.4. When implemented in a PLL a static phase magnitude difference of 90 degrees will exist when the circuit is locked.

• **Two state PD (RS-latch)**

  One of the simple phase detectors is obtained from an edge triggered RS latch. The characteristic curve of the RS latch-based phase detector is shown in Figure 1.5. The rising edge of A drives Q to ONE and that of B drives Q to ZERO. This detector changes state only on one edge of the inputs, it's characteristics differ those of an XOR gate in several respects.

  1) The output frequency (of Q-output) is the same as the input frequency.
  2) Average output doesn’t depend on the input duty cycle.
3) The input/output characteristic crosses ZERO when the inputs are 180 degrees out of phase.

There are some phase detectors based on the RS-latch which may contain other logic gates and maybe more than one latch. The use of the flip-flop as a phase detector was probably first considered by Judd [8].

- **Sequential phase frequency detectors (PFDs)**

Sequential PFDs generate two non-complementary outputs illustrated in Figure 1.6. If the frequency of input A, $\omega_A$, is less than that of input B, $\omega_B$, then the circuit generates pulses at either output $Q_A$ or $Q_B$ with a width equal to the phase difference, average value of $Q_A - Q_B$ is an indication of the frequency and phase difference between A and B. Three logical states are required. Those are $Q_A = Q_B = 0$; $Q_A = 0$, $Q_B = 1$; $Q_A = 1$, $Q_B = 0$. To
avoid dependence of the output on the duty cycle of the inputs the circuit should be implemented as an edge triggered sequential machine. A possible implementation of the above PFD is shown in Figure 1.6. This PFD consists of two edge- triggered re-settable D-flip flops. The PFD characteristic is also shown in Figure 1.6.

- **Charge pump based PFD.**

  The phase information for the PDs and PFDs discussed above is carried in the period or duty cycle at the output. It is necessary to convert this phase information into a voltage or current. One of the most popular methods for making this conversion for integrated applications is the charge pump comparator. The use of the charge pump circuit as a part
of the PD has appeared in the early 1970’s, but the small signal analysis was first done in a systematic way in 1983 by Gardener [13]. A charge-pump based PFD is shown in Figure 1.7. This phase comparator either injects, subtracts, or leaves alone the charge stored across a capacitor in the lowpass filter (LPF). When S1 is closed $I_{ch}$ flows into the LPF increasing the output voltage, which is used in general to drive the VCO, when switch S2 is closed $I_{ch}$ flows out of the LPF decreasing the output voltage. When both switches are open the top plate of the LPF capacitor is open circuited and the output voltage remains constant; see Figure 1.8. The signals $P_{up}$ and $P_{dn}$ are generated by the sequential PFD. The change in the output voltage will be

\[ \Delta V_{cnt} = \frac{\Delta Q_{ch}}{C_p} = \frac{I_{ch} \Delta t}{C_p} \]  

(1.7)
Because of the finite rise and fall times of S1 and S2, the PFD of Figure 1.7 can potentially suffer from a dead-zone which is depicted in Figure 1.8. Whether or not this problem exists depends upon the characteristics of the PFD block internal to Figure 1.7. Some PFD blocks are inherently insensitive to this dead-zone problem and others are inherently vulnerable. The dead-zone is undesirable because the loop will fail to correct for phase errors in a certain input phase range. This creates a peak to peak jitter approximately equal to the width of the dead-zone. The phase will differ when operating in the dead-zone. The dead-zone disappear only if $Q_A$ and $Q_B$ are both guaranteed to be high for a sufficient amount of time at each transition. An implementation of the charge pump circuit is shown in Figure 1.9. This implementation is based on the use of a differential input PFD and is reported [3] by Maniates. The A and B signals in Figure 1.7 are descriptively labeled DN and UP in Figure 1.9 indicating the direction the output voltage will move when the corresponding input is taken high. This simple circuit steers the tail currents in the tails of the two differential pairs.

![Figure 1.8 The charge pump PFD characteristics](image-url)
to either the left or the right. When the current in the left most differential pair is steered to the left, it is mirrored with the mirror comprised of M5 and M8 to the output.

1.4 Previous work

Because of the importance of the applications of the PLLs, there has been a tremendous amount of work done in this area. In the early development of the PLL, the work was primarily on analog phase locked loops (APLL). However, with increasing emphasis on digital circuitry because of decreasing cost, increased reliability, smaller size, and insensitivity to drift, there have been efforts to develop hybrid (analog-digital) PLLs (HPLL), discrete PLLs, and digital PLLs (DPLL) [8].

1.4.1 Analog phase locked loops (APLL)

The first description of the PLL appeared in a paper by Appleton [8]. The basic architecture consists of a PD, a loop filter, and a VCO as shown in Figure 1.1. When the
loop is locked the VCO frequency is ideally exactly equal to the average input signal frequency. The linearized analysis of this PLL was presented in Section 1.2. Both linear and nonlinear models for the PLL have been described both with and without noise in the literature. A systematic survey of this work was done by Gupta [8]. The previous analysis shows that the APLL has a threshold behavior, which means when the carrier to noise ratio (CNR) at the input drops below a certain value, there is a sudden deterioration of the performance of the APLL [5], [6].

1.4.2 Analog-digital (hybrid) phase locked loops (HPLL)

The HPLL is an APLL where one or more, but not all elements in the loop, are digital. A sampler is usually present in the loop in an HPLL. Digitizing the loop partially enables one to use efficient digital elements in the loop. The first HPLL was considered by Westlake [8], where the VCO was replaced by a digital VCO. The sampler was introduced after the loop filter. The digital VCO provides better performance over a wide dynamic range. The use of a digital phase detector has been considered by Judd [8] where the PD is replaced by a flip-flop which is triggered by the zero crossings of a sinusoidal reference signal. The digital counter is used to reduce the frequency feedback from the VCO within one cycle of the reference. The linearized model for the HPLL is shown in Figure 1.10 [8].
1.4.3 *Discrete phase locked loops*

A discrete PLL is modeled as shown in Figure 1.11. The sampler detects the error in the phase and the digital clock corrects it at discrete instances occurring once per cycle of the incoming signal. This type of digital loop can be implemented completely by discrete elements and works very well. The loop was first proposed by Gill and Gupta [8].
1.4.4 Digital phase locked loops (DPLL)

The continued progress in increasing performance, speed, reliability, and the simultaneous reduction in size and cost of integrated circuits (LSI and VLSI) has resulted in strong interest in the implementation of the digital PLL. The earliest efforts in DPLLs concentrated on partially replacing the APLL components with digital ones [9]. Apparently Westlake was the first to document the work in this direction in 1960 [9]. He introduced a sample and hold circuit at the output of the loop filter in order to take advantage of the improvements offered by the digital VCO. The first all digital PLL was reported by Drogin [9] in 1967. The second order loop was used as a VHF omnidirectional range finder to track a slow 30Hz sine wave. All the digital components were clocked synchronously. It is convenient to categorize the implementations of some of the DPLL into four classes. They are

1. Flip-flop DPLL. Uses a Set Reset positive edge triggered flip-flop as the phase detector.
2. Nyquist rate DPLL. The input is sampled at the Nyquist rate.
3. Zero Crossing DPLL. The detector tries to sample the incoming signal at the zero crossings.
4. Lead Lag DPLL. The PD determines at each cycle whether the input leads or lags the locally generated clock. The linear analysis of the DPLL is done in Z-transform.

My concentration in this thesis will be on the implementation of high speed PLLs, especially on the implementation of the phase and phase/frequency detectors. I will present a summery of some work reported recently in this area. An implementation of both a PD, and a sequential PFD in a dual-loop PLL was reported by Ware and Sodini in
1989 [14]. The PD and the PFD, shown in Figure 1.12, were implemented in a 2µm CMOS process and work at a maximum speed of 50 MHz. The whole loop works at a maximum speed of 200 MHz. A popular PFD and VCO delay cell used in a clock recovery circuit are shown in Figure 1.13a,b. This was reported by Rynolds [15] in 1994, the clock recovery circuit was implemented in a 0.8µm CMOS process and reported to

Figure 1.12 Implementation of (a) PD and (b) PFD
work at a maximum speed of 320MHz. These same architectures have been implemented with minor modifications by Horwitz et al in 1996 using a 0.8μm CMOS process where the clock recovery circuit was used for a serial data transceiver. The clock recovery circuit was reported to work at a speed of 320MHz [4]. Also these architectures are implemented by Maniatis using a 0.5μm CMOS process in 1996 [3] with a maximum speed of 550 MHz. Both Horwitz and Maniatis have implemented the voltage-controlled resistor with an active load of comprised of two PMOS transistors as shown in Figure 1.14 [16] using 2μ N-well CMOS process. The delay cell used here is fully differential which reduces the VCO sensitivity to power supply noise. In 1995 an all digital PLL was reported by Dunn et al [17] where they used single ended inverters to form the digitally controlled oscillator (DCO). The frequency was fully digital. The DCO can run at a maximum frequency of 550MHz with a wide dynamic range. The PLL was
implemented using a 0.5µm CMOS process. In 1996 Vincent et al [18] reported a low power PLL for Micro-processor clock generation. The PFD used is the same as the one shown in Figure 1.11. The VCO was built using single ended inverters. The circuit was built using a 0.25µm CMOS process and is reported to work at a max speed of 574MHz. In 1997, a semi-digital delay locked loop (DLL) was reported by Stdivopoulos and Horwitz [19]. The PD used is shown in Figure 1.15. The maximum speed of the circuit that was built using a 1µm CMOS process is 250MHz [19]. Also in 1997 McTaggered et al have reported a
transceiver that works at 1.0625GHz. The VCO is a ring oscillator with differential delay cells. The PFD that works at 106.25 MHz makes use of 10 phase-shifted versions of the VCO output signal. The PFD was implemented using D-FFs followed by XOR logic gates as shown in Figure 1.16. The circuit was built using a 0.5µm CMOS process [24].

In recent years the demand for high speed circuits and high speed PLLs has increased. As the speed of operation of the circuit increased the limitations on the allowed phase noise or timing jitter have become more stringent. Jitter models and jitter analysis for the ring VCO that use differential delay cells were published by Todd and Gray [11], [21]. The timing jitter analysis in the PLL considering all jitter sources was studied by Gray and Kim [11], [12] in 1994. The jitter model for the PLL is shown in Figure 1.17. The optimum loop bandwidth to

Figure 1.16 Implementation of clock recovery circuit (figure reproduced from [24])
minimize the jitter was derived recently by Kim in 1998 [12]. The clock and data recovery circuits based on the phase detectors and VCO's of Figures 1.13, 1.15, and 1.16 used a charge pump to convert phase information to a current output. They were essentially all most of high speed VCO structures reported recently were implemented using differential delay cells in ring oscillators implemented in CMOS sub-micron technology.

1.5 Summary

In this chapter the basic PLL architecture and its basic transfer characteristics were reviewed. Basic types of PDs and PFDs and their characteristics have been summarized. Previous work in PLLs and clock recovery circuits was highlighted. The next chapter will include more details about the PLL linear analysis, and a new PFD will be introduced.
CHAPTER 2. PLL LINEAR ANALYSIS, AND
INTRODUCTION TO THE PROPOSED PFD

This chapter will provide some basic details regarding the PLL model and the small signal analysis. The small signal analysis for a charge pump based PLL will be given. Also in this chapter I will discuss our technique for the phase and frequency detection on a traditional analog model. An advanced model as a hybrid (analog and digital) circuit will be discussed for this method. Finally the characteristics of our phase/frequency detector will be specified and discussed.

2.1 Analog phase locked loop (APLL) small signal model

The PLL circuit has the basic architecture shown in Figure 1.1 and repeated in Figure 2.1 for convenience. As discussed in Chapter 1, The analog phase locked loop (APLL) small signal analysis leads to the transfer function

\[ H(s) = \frac{\theta_{\text{out}}(s)}{\theta_{\text{in}}(s)} = \frac{K_{\text{vco}}K_{\text{pd}}F(s)}{s + K_{\text{vco}}K_{\text{pd}}F(s)} \]  

(2.1)

Where \( \theta_{\text{in}} \) is the phase of the input signal and \( \theta_{\text{out}} \) is the phase of the VCO output carrier, \( F(s) \) is the loop filter transfer function, \( K_{\text{pd}} \) is the phase detector gain, and \( K_{\text{vco}} \) is the voltage controlled oscillator (VCO) gain. Both \( K_{\text{pd}} \) and \( K_{\text{vco}} \) are constants. The loop gain is defined as \( K = K_{\text{vco}} \cdot K_{\text{pd}} \), and the VCO gain is defined \( K_{\text{vco}} = \frac{d\omega}{dV_{\text{ctrl}}} \). The VCO control voltage at the output of the loop filter will be
\[ V_{\text{ctrl}}(s) = (\theta_{\text{in}}(s) - \theta_{\text{out}}(s))K_{pd}F(s) \]  

(2.2)

and the VCO output phase will be

\[ \theta_{\text{out}}(s) = \frac{K_{VCO}}{s} \cdot V_{\text{ctrl}}(s) \]

If we assume a general first order loop filter with the transfer function

\[ F(s) = \frac{a \cdot s + b}{c \cdot s + d} \]  

(2.3)

where \( b/d \) is typically much than \( a/c \). In this situation, the loop filter bandwidth is approximately \( d/c \). Then the loop transfer function will be

\[ H(s) = \frac{K \cdot a \cdot s + K \cdot b}{c \cdot s^2 + (d + K \cdot a)s + K \cdot b} \]  

(2.4)

If we write the denominator, \( c \cdot s^2 + (d + K \cdot a)s + K \cdot b \), in the form \( s^2 + 2\xi \omega_n s + \omega_n^2 \) then we get

\[ \omega_n = \sqrt{\frac{K \cdot b}{c}} \]  

(2.5)

---

**Figure 2.1 Basic analog PLL**
\[ \xi = \frac{1}{2} \frac{d + K \cdot a}{\sqrt{K \cdot b \cdot c}} \] (2.6)

\( \omega_n \) is the natural frequency of the system, and \( \xi \) is the damping factor. Usually \( \xi \) is greater than 0.5 and preferably equal to 0.707 to provide an optimally flat frequency response. The linearized analysis describes the loop dynamics accurately when it is in lock [3]. The range of input signal frequencies in which lock can be attained eventually is defined as the capture range. The time required to attain lock can be approximated by [1], [3]

\[ t_{acq} = \frac{Q(\omega_{in} - \omega_{osc})^2}{\omega_n^3} \] (2.7)

where

\[ Q = \frac{\sqrt{K \cdot b \cdot c}}{d + K \cdot a} \] (2.8)

\[ t_{acq} \propto \frac{c^2}{(d + K \cdot a)(K \cdot b)} \] (2.9)

\( \omega_n \) has to be in the range that the VCO can produce. From Equation 2.9 we can reduce the acquisition time by increasing the loop filter bandwidth, or by increasing the loop gain, K. Once lock is attained, as long as the input signal’s frequency changes only slowly it will remain in lock over a range that is much larger than the capture range [2]. The maximum excursion of the VCO’s frequency away from its free running frequency (lock range) is given by

\[ \omega_{lock} = \pm K_{pd} \cdot K_{vco} \cdot K_{lp} \] (2.10)
where $K_{lp}$ is the DC gain of the loop filter, in our case $K_{lp} = \frac{b}{d}$. From Equation 2.10 the lock range can be increased by increasing the loop gain, $K$, or by increasing the loop filter DC gain. The PLL will track the input signal as long as the frequency of the input signal doesn’t exceed the lock range.

### 2.2 Phase locked loops (PLLs) with charge pump

Phase locked loops incorporating sequential logic Phase/Frequency detectors (PFD) have been widely used since the beginning of the 1970s. Reasons for their popularity include extended tracking range, frequency aided acquisition, and low cost [3], [13]. A charge pump usually accompanies the PFD. The basic charge pump PD is shown in Figure 1.7 and is repeated in Figure 2.2. This phase detector will either inject, subtract, or leave alone the charge stored in the lowpass filter. In this circuit the low pass filter is of second order. When

![Figure 2.2 Sequential PFD with charge pump circuit and loop filter](image-url)
control signal UP is high and control signal DN is low only switch S1 will be closed, $I_{ch}$ flows into the LPF capacitor increasing the output voltage, $V_{out}$. When the control signal UP is low and control signal DN is high only switch S2 will be closed and $I_{dch}$ flows out of the loop filter decreasing the output voltage, $V_{out}$. If $I_{ch} = I_{dch}$, then when the two signals are the same there will be no net change in the charge stored in the loop filter. Because of the switching, the charge pump PLL is a time varying network; an exact analysis must take account of the time variations of the circuit topology. For the small signal analysis the assumption is made that the frequency of the VCO in the PLL changes by only a very small amount during each cycle of the input signal, with this assumption we will be interested only in the average behavior over many cycles [1], [13]. Typical waveforms of a charge pump phase comparator are shown in Figure 2.3. At each leading edge of Vin, S1 turns on which causes a current $I_{ch}$ to flow into the filter. This causes an increase in the output voltage across $C_p$. If $C$ is small compared to $C_p$, the change in the output voltage across $C_p$ will be given by

$$\Delta V_{Cp} = \frac{\Delta Q_{Cp}}{C_p} = \frac{I_{ch} \Delta t}{C_p}$$

(2.11)

The average current flowing into the low pass filter will be

$$I_{avg} = \frac{\Delta \Phi_{in}}{2\pi} I_{ch}$$

(2.12)

By definition, the average charge pump current is related to the phase detector gain $K_{pd}$ by [1], [13]

$$I_{avg} = K_{pd} \Delta \Phi_{in}$$

(2.13)
Figure 2.3 Timing diagram of charge pump as a PFD

So the average phase detector gain will be [3], [13]

\[ K_{pd} = \frac{I_{ch}}{2\pi} \]  

(2.14)

If C=0, the loop filter becomes first-order and the transfer function of this filter is

\[ F(s) = \frac{V_{out}(s)}{I_{in}(s)} = \frac{sC_pR + 1}{sC_p} \]  

(2.15)

Using the loop filter terminology of the previous section we end up with

\[ a = C_pR; b = 1; c = C_p; d = 0, \]  

and the transfer function of the loop will be

\[ H(s) = \frac{K \cdot RC_p \cdot s + K}{C_p \cdot s^2 + (K \cdot RC_p) s + K} \]  

(2.16)

From the equations of Section 2.1 we find out that the loop natural frequency, damping factor, and Q factor are given by

\[ \omega_n = \sqrt{\frac{K}{C_p}} \]  

(2.17)
From the above equations one will be able to determine the lock range, the acquisition time, and the loop bandwidth. Those parameters and the stability of the circuit will be affected by the choice of the values of $I_{ch}$, $C_p$ and $R$.

### 2.3 The phase/ frequency detector

#### 2.3.1 Review

In the traditional APLL the phase detector is multiplier as shown in Figure 2.4. If the input signal is $x_m = V_m \cos(\omega_m t + \theta_m)$ and we have a local oscillator with the signal $x_{lo} = \cos(\omega_{lo} t + \theta_{lo})$ then the output of the multiplier will be

$$V_{out} = \frac{1}{2} V_m \cos(\theta_m - \theta_{lo}) + \frac{1}{2} V_m \cos(2\omega_{lo} t + \theta_{in} + \theta_{lo})$$  \hspace{1cm} (2.20)

Using a low-pass filter (LPF) with unity low frequency gain we get-rid of the high frequency component and we end up with $V_{out} = \frac{1}{2} V_m \cos(\theta_m - \theta_{lo})$. This holds the information about the

![Figure 2.4 Traditional APLL.](image-url)
phase difference between the two waveforms.

To enhance the speed of operation of the traditional PLL there are different approaches like using dual loops to reduce the acquisition time. This approach was used in the Costas loop circuit where we use two loops and a 90 degrees phase shift circuit, a Hilbert transform filter, to double the loop gain as shown in Figure 2.5. Due to the 90 degree phase shift between the VCO output signals we need to subtract the two error signals because they will have opposite signs.

\[
\text{Figure 2.5. The Costas loop.}
\]

If both loop filters have unity DC gain, the control voltage at the output of the adder will be [5], [6].

\[
V_{\text{out}} = V_{\text{in}} \cos(\theta_{\text{in}} - \theta_{\text{lo}})
\]

(2.21)

where \(\theta_{\text{lo}}\) is the phase of the VCO output. Another approach to enhance the speed of the PLL is by adding a frequency detector. The output signal of the frequency detector will be the dominant when a big frequency or phase difference exists. Once the two signals become of the same frequency, the output of the phase detector will become the dominant control signal. The addition of the frequency detector results in increasing the speed of lock enormously,
this property is called the aided acquisition. The PLL with both PD and FD is shown in Figure 2.6.

3.2.2 The proposed detector

The proposed PFD is based on the concept of having dual loops as shown in Figure 2.7. In this circuit we generate phase lead and phase lag versions of the VCO output signal using the $\pm \delta$ and $-\delta$ phase shifters. These outputs are then mixed with the input waveform, and passed through identical upper and lower lowpass filters, (LPF) to generate error signals $e_1$ and $e_2$. Finally we subtract these two error signals to provide the control voltage for the VCO. If we have an input signal $X_{in} = V_{in} \cos(\omega_{in} t + \theta_{in})$, and a sinusoidal oscillator output $V_{lo} \cos(\omega_{lo} t + \theta_{lo})$; then it can be shown from a simple manipulation of trigonometric identities that the error signal $e$, (the VCO control voltage), will be [20]

\[ e = e_1 - e_2 \]  \hspace{1cm} (a)

\[ e = \frac{K_{ip} V_{in} V_{lo}}{2} \left[ \cos(\Delta \omega t + \Delta \theta - \delta) \right] \]  \hspace{1cm} (b)

\[ e = K_{ip} V_{in} V_{lo} \sin(\Delta \omega t + \Delta \theta) \sin(\delta) \]  \hspace{1cm} (c)
Figure 2.7 The Proposed PFD basic architecture.

where $K_{ip}$ is the low pass dc filter gain, $\Delta \omega = (\omega_{in} - \omega_{lo})$, and $\Delta \theta = \theta_{in} - \theta_{lo}$. Signals $e1$ and $e2$ are the control signals in the two loops. The error signal $e$ will be zero when both frequency and phase differences are zeros. The equivalent phase detector is monotonic in the range $[-\pi/2, \pi/2]$. The phase detector is sensitive to both frequency and phase variations. The sensitivity of the phase detector can be increased by choosing $\delta$ to be as close as possible to $\pi/2$.

The implementation of this concept can be simplified if we are using a ring oscillator to implement the VCO since different phase shifted versions of the local oscillator output to provide the $+\delta$ and $-\delta$ phase shifts are inherently available. An implementation of the PFD with a ring VCO is shown in Figure 2.8, where the multipliers are replaced by 2-input AND gates. The VCO is constructed using differential delay cells. The lowpass filters and the subtractor are realized with a charge pump driving a charge storage capacitor in the loop filter [20]. An input sampler is used to allow us to deal with both RZ and NRZ binary input and to pinch the input transitions to the detector between the transitions of the leading and the
lagging outputs from the oscillator. This sampler is implemented by a pass transistor logic And gate.

Typical error signals are shown in Figure 2.9.a, and Figure 2.9.b. In those figures we assume that the loop is initially locked then a small variation in the input data frequency occurs. It is clear from the figures that if the input data frequency becomes higher than the oscillator frequency (Figure 2.9.a) then the pulse width of signal e1 increases, while the e2 signal pulse width becomes narrower. If the input data frequency becomes less than the oscillator frequency (Figure 2.9.b) then the pulse width of signal e1 decreases, while the e2 signal pulse width becomes wider. The area under the curves of the two error signal pulses are subtracted from each other in the charge pump circuit creating an increasing oscillator control voltage if $T_n$ becomes less than $T_io$, and vise versa, where $T_n$ is the input data period.
Figure 2.9 proposed PFD timing diagram for (a) increase and (b) decrease in input frequency

and $T_{lo}$ is the local VCO period. Analytically, after a change in the data frequency timing of error signals and the error voltage at the output of the charge pump are given by

$$e_1 = u\left(t - T_{in} - \phi\right) - u\left(t - \frac{3T_{lo}}{2} + \delta\right)$$  \hspace{1cm} (2.23.a)

$$e_2 = u\left(t - T_{in} - \delta\right) - u\left(t - \frac{3T_{in}}{2} - \phi\right)$$  \hspace{1cm} (2.23.b)

$$e = \frac{I_{ch}}{2C_p} \left\{ \frac{5}{2}(T_{lo} - T_{in}) - 2\phi \right\}$$  \hspace{1cm} (2.23.c)

where $e$ is the error voltage at the output of the charge pump, and $\phi$ is the instantaneous phase shift between the rising edge of the input data, and the rising edge of the output of the VCO. $C_p$ is the charge storage capacitor at the output of the charge pump circuit. The loop will be inherently open during the part of each period when the error signals $e_1$ and $e_2$ are zeros.
In Figure 2.10.a and Figure 2.10.b we show the timing error signals for the case where an instantaneous phase shift occurs at a certain instant, which describes the operation of the circuit as pure phase detector. It is interesting to notice that the two error pulses are not simultaneous, and their widths move in opposite directions. The first note makes the gain of the phase detector to have different values over the allowed range of phase error. In Figure 2.3.8, we show that the gain of the detector is proportional to the sum of the charge current and discharge current divided by the value of charge storage capacitor for the phase error in the range \(-\delta\) to \(+\delta\), which is almost twice the traditional phase detector gain. While in the phase error range from \(-\pi+\delta\) to \(-\delta\) and in the range from \(\delta\) to \(\pi-\delta\) the phase detector gain will be proportional to the difference between the two currents. This behavior is the opposite to the behavior of the traditional state machine PFD that have very low phase detector gain around zero phase error and larger gain for large phase errors. The second note shows that it is never been the case that the width of the two error pulses decrease to a very narrow width simultaneously which makes the detector dead zone free. This property will reduce the jitter in the circuit. As mentioned above the loop will be open when both error pulses \(e_1\) and \(e_2\) have zero level. So on the average the loop will be open for half of the period of high level input data, and will also be open over the period of time when the input has a low level. In this situation, on the average, the loop will be open for 75\% of the time of operation. The equations above show that the detector used is sensitive to both frequency and phase variations. The net integral error will be zero when both \(T_{lo} - T_{ln} = 0, \ \phi = 0\). Since the NAND logic gate is the fastest gate present, and since this PFD is constructed from two And gates followed by a charge pump circuit, this architecture is faster than the traditional PFD circuits. Also, as shown in Figure 2.9, this PFD makes a double check on the timing of every input
Pulse. In fact it compares the relative positions of both the rising and falling edges of the input pulse with those of the VCO output waveform. The phase detection in this manner makes detector operation to be unaffected by reference pulse width variation as long as this pulse width variation is symmetrical around the pulse center. In Figure 2.11 the reference pulse width becomes narrower than the nominal width. Pulse width narrowing in this manner can occur due to channel limited bandwidth. The Figure 2.11 shows that both control pulses e1 and e2 will become narrower by the same amount which will not affect the operation of the phase detector. The characteristics function of the PD including the charge pump circuit
is shown in Figure 2.12 for the case when $I_1=I_2$. In case of $I_{ch}>I_{dch}$ and at lock the pulses of $e_2$ will be wider than the pulses of $e_1$. This case has an advantage that when implemented in a clock recovery circuit, the circuit will start faster, but it will introduce a DC phase shift between the input signal waveform and the output of the VCO. The opposite case is also possible.
2.4 Summary

In this chapter PLL transfer function and properties are shown. Linear analysis for the traditional PLL and the charge pump based PLL are also demonstrated. A new PFD is introduced as an analog circuit. A digital implementation of the PFD including timing diagrams that describes the operation of the detector are presented. The proposed PFD characteristics are highlighted. Next chapter will include design and implementation of the PFD and other sub-circuits in the clock recovery circuit constructed to demonstrate the operation of the proposed PFD.
CHAPTER 3. CIRCUIT DESIGN AND REALIZATION

This chapter will provide some details regarding the implementation of the lead/ lag phase/frequency detector (PFD) and the PLL described in the previous chapter. A transistor level description for the circuits used in the proposed clock recovery circuit to implement the VCO, the loop filter, and the replica biasing circuit is described. A temperature compensation technique is used to overcome the effect of the temperature variation on the circuit operation. The use of the clock recovery circuit to implement a data recovery circuit is also described.

3.1 Realization of the PFD

The proposed lead/lag PFD implemented in a clock recovery circuit is shown in Figure 2.8 and is repeated here in Figure 3.1. In this figure it is assumed that the input data is single-ended.

At high frequencies the input data is often differential such as that in fiber optics transceivers. We thus need to either create fully differential implementations of all of the blocks in Figure 3.1, or make a differential to single-ended conversion some where in the loop. In the later case, the performance of the differential to single-ended conversion becomes critical. For simplicity I will use a front-end circuit to convert the input differential data to single-ended needed. In this conversion, I will assume fiber-channel standards with a high DC level and around one volt peak swing as an input. This will be converted to standard CMOS logic format with 50% duty cycle. A circuit proposed by Maneatis [3] is shown to be able to do this job. The circuit schematic is shown in Figure 3.2. The circuit contains two regular differential pairs connected in parallel followed by a differential pair without a tail.
current source. The later step makes it suitable to provide a wide swing, rail to rail, output signal. Circuit simulation for this converter will be provided in Chapter 5. The output of the differential to single ended circuit is passed through two ratioed inverters to reduce rise and fall times. It is then feed into the sampler. The sampler at the input of the circuit is an AND gate implemented by two transmission gates as shown in Figure 3.3. The sampler is controlled by the differential output of the VCO clock which is denoted by clk and \( \overline{\text{clk}} \).
sampler allows us to pinch the input signal transitions between the leading and the lagging versions of the VCO output and allows us to deal with a NRZ data format. The AND gates used in the PFD are traditional static NAND gates followed by CMOS inverters. The sampler, the AND gate, and the biasing generator schematics for the circuit of Figure 3.1 are shown in Figure 3.3. Equivalently the sampler can be implemented by a static AND gate.

![Figure 3.3](image)

Figure 3.3 The schematics of (a) biasing generator, (b) the sampler, and the (c) AND gate

The PFD also includes a charge pump circuit. A transistor level charge pump implementation with the loop filter is shown in Figure 3.4. The loop filter is composed of R and $C_p$. Transistor M1 will be off, and M2 will be on when the error pulse $e_1$ is a high, and transistor M5 will charge the loop filter capacitor. Transistor M4 will be off, and M3 will be on when the error pulse $e_2$ is a high, and transistor M6 will discharge the loop filter capacitor. Because of the switches present between the charge pump and the loop filter it can be observed that if the input data is a stream of successive low level bits the error pulses will have zero level and the loop will be open. When the input is a stream of successive high level bits the circuit will actually feed the output of the VCO to the phase detector resulting in a period of $e_1$ being equal to that of $e_2$. If charging and discharging currents are equal, the
VCO control voltage will ideally maintain a constant average. In both cases no change will occur on the output frequency or phase.

My goal will be to design this circuit for operation at a 1GHz input frequency or higher with temperatures up to 100 °C using a 0.6µm CMOS process. This means that we are approaching the fundamental switching speed limit that we can reach with this process. While doing the layout for a circuit that will work in those conditions, we will try to reduce the effect of the parasitic elements as much as we can. The layout was done using interdigitized structures for large transistors, dimension > 50λ, to reduce the effect of wafer properties variation over the die area, and the active area was shaved around the contacts to reduce the drain and source areas as shown in Figure 3.5. The number of contacts used depends on the maximum current density that will pass through the transistor in the worst case, highest temperature of operation.
3.2 Clock recovery circuit design

As shown in Figure 3.1 the clock recovery circuit contains the PFD described in the previous section, the VCO, the loop filter, and the bias generator circuit. First the VCO structure will be described and later on the modifications that enhance performance will be discussed. Because of its integrability on chip and its low cost, the ring VCO is widely adopted in the realization of the high speed PLLs, even though it produces more jitter than the LC-tank oscillators. The ring VCO consists of delay cells or inverters in a ring as shown in Figure 3.6. If we are using single ended inverters then the number of inverters in the ring must be odd, but if the inverter delay cells are differential then the number of delay cells can be either odd or even. The frequency of oscillation can be approximated by [11], [22]

\[ f_{lo} = \frac{1}{T_{lo}} = \frac{1}{2N t_d} \] (3.1)

where N is the number of delay cells in the ring and \( t_d \) is the nominal delay period of the
Delay cell. Differential delay cells are generally more immune to the power supply noise [3] than single-ended structures.

In our circuit the VCO has been implemented using differential delay cells. The delay cells are the same as those reported in [3], [4], and [7]. Those cells have symmetric load PMOS transistors. The delay cell is shown in Figure 3.7. If the circuit is designed so all transistors are in saturation, the small signal transfer function of the delay cell is

\[
A(s) = \frac{V_{OS}}{V_{ID}} = \frac{-g_{m1}/C_L}{2(s + g_{m2}/C_L)}
\]

where \(V_{OS}\) is the single ended output voltage and \(V_{ID}\) is the differential input voltage. If we assume the loss \(g_{m2}\) is sufficiently large to maintain a nearly sinusoidal oscillation frequency, it can be shown that the frequency of oscillation is given by the expression

\[
f_{io} = \frac{1}{2\pi} \frac{g_{m1}}{2C_L} \sin\left(\frac{\pi}{N}\right)
\]

where \(N\) is the number of stages in the ring oscillator. Since \(g_{m1}\) is linearly proportional to the excess bias, \(V_{gs} - V_T\), of the transistor that provides the tail current in the differential pair,
it can be shown that $f_{io}$ is linearly proportional to the control voltage $V_p$. So we can increase the frequency of oscillation by increasing $V_p$ which will increase the radius of the circle on which the VCO poles lie and will shift this pole locus circle horizontally to the left. Correspondingly reducing $V_n$ will shift the pole locus circle back towards the origin. This will give a better spectral purity of the VCO output.

The biasing circuit shown in Figure 3.3 is used to generate the control voltage $V_n$ from $V_p$. This biasing circuit is the same one presented in [3],[4], and [7]. Single ended outputs are needed to derive the multipliers (AND gates). A single-ended output is obtained by using a regular differential pair followed by two inverters as a buffer. The buffer circuit schematic is shown in Figure 3.8.

The VCO was designed using 5 differential delay cells. In the implementation discussed in Chapter 5, the VCO can produce output oscillation frequencies in the range from 680MHz-1.35GHz in a 0.6µ CMOS process.
The loop filter is simply a resistor in series with a capacitor as shown in Figure 3.9. The transfer function of the first order lowpass filter (LPF) is given by

\[ F(s) = \frac{V_{out}(s)}{I_{in}(s)} = \frac{sC_p R + 1}{sC_p} \quad (3.5) \]

The loop filter capacitor should be large enough so that we can neglect the effect of the VCO input capacitance. A small signal analysis will lead to the same transfer function for the PLL as was described in Chapter 2. The filter parameters R and C_p should be selected such that the system will be stable with an acceptable phase margin and the loop bandwidth has a value that will reduce the jitter effect.

Figure 3.8 The buffer schematics

Figure 3.9 The loop filter.
3.3 Temperature compensation

As mentioned before we are approaching the maximum speed of operation in a 0.6µm process. This necessitates managing the temperature variation effects on the operation of the circuit. Temperature increases tend to reduce the transconductance, $g_m$, of all the transistors in the circuit which results in slowing down the speed of operation of all circuit components like the VCO and the PFD. For example, simulation results show a design which provide a maximum frequency of oscillation for the extreme setting on the bias generator with five delay cells of 1.35GHz at the nominal temperature, 25°C drops to 1.2GHz at 100°C for the same control voltage. To overcome the temperature variation effect on the speed of the circuit, a temperature sensor was built and the VCO delay cell has been modified so that the delay cell control will have two inputs, one from the PFD output, and one from the temperature sensor. The modified delay cell is shown in Figure 3.11. The additional control inputs are $V_{tn}$ and $V_{tp}$ will come from a second bias generator. The temperature sensor will provide a DC voltage that generates half of the bias current needed to put the VCO around 1GHz. The PFD will drive the first bias generator to provide the other half of the bias current. As the temperature goes up the temperature sensor DC voltage will increase to help the VCO sustain the same frequency of oscillation. A second temperature sensor is connected to the charge pump circuit to increase the gain of the charge pump with temperature since at higher temperatures larger control voltage variations are required for the same frequency variation. The temperature sensor is based on two diode-connected transistors from the same type between the supply voltage, $V_{dd}$, and ground as shown in Figure 3.10. From Figure 3.10 we note that
\[ I_{d1} = I_{d2} \quad ; \quad V_{gs1} + V_{gs2} = V_{DD} \] (3.6)

By assuming the transistor satisfy the square law relationship and neglecting \( \gamma \) effects we obtain the expression

\[ \mu_{n1} \frac{W_1}{L_1} (V_{gs1} - V_T)^2 = \mu_{n2} \frac{W_2}{L_2} (V_{DD} - V_{gs1} - V_T)^2 \] (3.7)

By straight mathematical manipulations and by taking the derivative with respect to temperature we end up with

\[ \frac{\partial V_{gs1}}{\partial T} = \left( \frac{W_1}{L_1} - \frac{W_2}{L_2} \right) \frac{\partial V_T}{\partial T} \left( \frac{W_1}{L_1} + \frac{W_2}{L_2} \right) \] (3.8)

Figure 3.10. Temperature sensor with amplifier

From the equation above it follows that we can build a positive or negative temperature coefficient circuit depending on the ratios of the transistor sizes. For our implementation the amplifier in Figure 3.10 is a traditional differential pair. The other side of the differential pair is connected to a fixed voltage generated by equal size diode connected transistors since this
structure has zero temperature coefficient. The ratio between the sizes of transistors M1 and M2 should be large enough to overcome the effect of the reduced amplifier gain at high temperatures.

The temperature compensation inputs are $V_{tn}$ and $V_{tp}$. The amplified temperature sensor output is connected to a bias generator to provide the temperature controlled voltage $V_{tn}$ from the temperature controlled voltage $V_{tp}$. This new bias generator is a replica bias generator shown in Figure 3.12. The temperature compensation circuit doesn’t eliminate the temperature variation effects completely but does reduce the effects of temperature. Simulation results are presented in Chapter 5.

Figure 3.11. The modified delay cell.
3.4 Data recovery implementation

The clock recovery circuit shown in Figure 3.1 and described in this chapter can be easily modified to perform data recovery task. In Figure 3.13 a block diagram describing a possible data recovery circuit implementation using a previously designed clock recovery circuit is shown. The problem with this implementation is that we need the delay period of the delay unit to be exactly equal to the propagation delay of the register used to recover the data. The implementation for the data recovery can be simplified by using the available phase shifted versions of the VCO output. The implementation is shown in Figure 3.14 where we use two data registers, The first regular one is used to recover the data. The second data register is the same as the previous one but modified to become double edge triggered register and it is used to make the VCO output sample it’s phase leading version which will reproduce the VCO output but shifted by the propagation delay of the data register. The VCO
Figure 3.13 Proposed implementation of data recovery circuit using clock recovery circuit

Figure 3.14 The data recovery circuit
shifted version should lead the VCO output by a period larger than the setup time of the flip-flop. The schematic of a GHz flip flop is shown in Figure 3.15

3.5 Summary

In this chapter a fast clock recovery circuit was introduced. A transistor level design and description of the PFD including a charge pump circuit, sampler, bias generator, loop filter and VCO were presented. A temperature compensation technique was described. An implementation of a data recovery using the clock recovery circuit was presented.
CHAPTER 4. INTRODUCTION TO TIMING ERRORS

Timing errors is an important issue for data recovery circuits especially for high speed of operation. This chapter summarizes recent results from the literature on analyzing timing errors in high speed PLLs. It is presented for completeness. The only substantive difference between what is presented here and what appears in the literature is the straightforward change in the active load of the delay cell from one transistor operating in the triode region to two similar transistors operating in the saturation region.

4.1 Introduction to timing errors

Data transfer rate or processor cycle period can be limited by timing errors present in the system and in the timing circuits that used for clock recovery, or frequency synthesis [21]. As an example the maximum speed of system clock can be written as a function of the setup and hold time and the timing error in the system, $\Delta t_{\text{error}}$, as

$$ f_{\text{max}} \leq \frac{1}{t_{\text{sh}} + \Delta t_{\text{error}}} $$

Timing errors encountered in electronic systems can be classified by four categories [21].

1- Random phase variations, timing jitter, result from thermal noise.

2- Systematic phase variation due to interfering signals from else where in the system.

   Interference can occur by coupling of power supply or substrate noise to clock or oscillator signal.

3- DC timing errors, offsets in phase or frequency which results in clock skew.

4- Phase or frequency drift due to temperature variations, and glitches in power supply.
In our design we have shown in Chapter 3 how to take care of temperature variation effects on the operation of the whole circuit. Moreover the VCO architecture with its differential delay cells and replica-biasing scheme is reported by several published work to be independent on the supply noise and process variations. In fact a mismatch in one of the delay cells of which we connect there output for edge comparison will result in a DC phase error, phase shift, when the circuit is locked, which is the same effect observed if we have a mismatch in the charge pump currents. A possible solution for this error is to make one of the charge pump currents a sum of two currents one of which can be adjusted while applying a training reference to the circuit. A mismatch in the other delay cells that are not between the mentioned delay cells will not affect the operation of the detector. So the main source of error in our circuitry is the random phase noise or timing jitter.

4.2 Introduction to jitter analysis

4.2.1 Overview

As mentioned before the demand on high-speed circuits have been increased recently especially for the input/output (I/O) interfaces, and processors. Higher speed of operation in the PLL requires better performance from the VCO and the overall PLL [3], [10]. The ring VCO is adopted because it is attractive from an integration point of view, but it suffers larger timing jitter than the LC-tuned oscillator [12]. The loop jitter is mainly affected by the internal noise sources such as the VCO, the PFD, and also by the loop bandwidth selections [12]. Jitter in the VCO is usually the dominant contributor for frequency synthesis applications [10], [21]. In clock recovery applications there is often a significant amount of
jitter from the input source as well as the VCO [10], [12]. A narrow bandwidth PLL rejects the input jitter but doesn’t correct VCO timing errors as quickly. A wide bandwidth PLL can correct the VCO errors more quickly but leaves the system input jitter unlimited [10] [21]. High frequency transceivers that work around 1GHz use a clock recovery circuit with the VCO of the PLL running at a division of the data frequency have been reported [4], [24], [25], even though this approach results in reducing the dissipated power, and allowing the use of slow phase detectors, but it results in a high phase noise, jitter, which results in a high bit error rate. The lower the frequency of oscillation we have the higher the amount of jitter we get [21]. Moreover the frequency division by a factor M will boost the phase noise by factor of \( M^2 \) when referred to the output [21]. To simplify the analysis flicker noise is ignored because of its 1/f nature, and shot noise is negligible because of the small CMOS leakage current. Thermal noise is considered the dominant device noise [21], [23]. Timing jitter is the time domain characterization of the phase noise. The model for various jitter sources in the PLL is shown in Figure 4.1 [21]. The response to phase errors injected by the VCO can be determined by

\[
\frac{\theta_{\text{out}}(s)}{\theta_{\text{VCO}}(s)} = \frac{s^2}{s^2 + Ks + K\tau}
\]

(4.1)

Where \( K = K_{pd}K_{vco}K_f \) and \( F(s) = \frac{K_f(s + \tau)}{s} \), \( K_f \) is the loop filter DC gain. In terms of the loop filter described in Chapter 3 \( K_f = R \) and \( \tau = \frac{1}{RC_p} \). As mentioned above the jitter contribution of the PD and the loop filter are insignificant if compared to the jitter injected by the VCO and the input reference. The response of the loop to phase errors injected by the reference, input, data can be determined
Figure 4.1 Linearized small signal model with noise sources

\[ \frac{\theta_{\text{out}}(s)}{\theta_{\text{ref}}(s)} = \frac{K(s + \tau)}{s^2 + Ks + K\tau} \]  

(4.2)

To describe the jitter injected by the VCO we have to describe the jitter at the output of the delay cell first.

### 4.2.2 Jitter analysis for the delay cell

Cycle to cycle jitter is measured as the root mean square (r.m.s.) variation in the output period of the oscillator. The delay cell has a nominal time delay \( t_d \) and timing error \( \Delta t_d \). For \( N \) stage ring VCO the nominal period will be \( T = 2Nt_d \) [11], [22]. The differential delay cell with transistors thermal noise sources are shown in Figure 4.2. The power spectral density of thermal noise current source is given by \( \overline{i_n^2} = 4KT \gamma g_m \Delta f \), for a transistor in the saturation region, and by \( \overline{i_n^2} = 4KT \gamma g_m \Delta f \) for a transistor in the triode region. The constant \( \gamma \)
depends on the technology used, is considered in most cases to be equal to one, \( K \) is Boltzmann’s constant, and \( T \) is temperature in Kelvin. The nominal time delay of the delay cell is approximated by

\[
t_d = \frac{C_L V_{SW}}{I_{SS}}
\]

(4.3)

where \( \frac{I_{SS}}{C_L} \) is the slew rate, and \( V_{SW} = 1 \) Volt for similar structures [21], [22], \( C_L \) is the equivalent capacitance at the output of the delay cell, and \( I_{SS} \) is the tail current of the differential delay cell. Voltage error, \( \Delta V_n \), due to timing error \( \Delta t_d \) at switching instant is

\[
\Delta V_n = \Delta t_d \frac{dV_o}{dt} \quad \text{where} \quad \frac{dV_o}{dt} = \frac{I_{SS}}{C_L}
\]

It is assumed that the next stage will begin switching when the differential output voltage reaches zero as shown in Figure 4.3 the variance of the timing jitter is
\[ \Delta t_d^2 = \Delta V_n^2 \frac{I_{ss}}{C_L} \]  

(4.4)

The single stage figure of merit is defined as

\[ \frac{\Delta t_d^2}{t_d^2} = \frac{\Delta V_n^2}{V_{SW}^2} \]  

(4.5)

As a simplifying assumption we assume that we have constant noise sources so that the output voltage error variance at nominal switching time can be written as

\[ \overline{\Delta V_{on}^2} = \sum_{l=0}^{7} i_{m_i}^2(f) |H_i(f)|^2 df \]  

(4.6)

Note that the phase noise of transistor M5 is neglected because it is a common mode signal. Moreover the effect of transistors M6 and M7 is included with transistors M1 and M2 since \( g_{m,1,2} = g_{m,6,7} \). Also load transfer function, H(f), at the output of the delay cell is given by

\[ H(f) = \frac{R_L}{sC_L R_L + 1} \]  

(4.7)
Which is a resistor \( R_L \) in parallel with a capacitor \( C_L \). So voltage noise variance, power, at the output of the delay cell due to thermal noise of transistors M3 and M4 is

\[
\Delta \bar{V}^2_{on,3,4} = \int_0^\infty 4KT \gamma_3 g_m \left| \frac{R_L}{1 + 2j\pi f R_L C_L} \right|^2 df \tag{4.8}
\]

Since

\[
f_0 = f_{3dB} = \frac{1}{2\pi R_L C_L} \tag{4.9}
\]

then

\[
\Delta \bar{V}^2_{on,3,4} = 4KT \gamma_3 R_L^2 \int_0^\infty \left( \frac{1}{1 + \frac{f}{f_0}} \right)^2 df = \frac{KT}{C_L} \gamma_3 g_{m,3} R_L \tag{4.10}
\]

for transistors M1 and M2

\[
\Delta \bar{V}^2_{on,1,2} = 2\int_0^\infty 4KT \gamma_1 g_{m,1} \left| \frac{R_L}{1 + 2j\pi f R_L C_L} \right|^2 df \tag{4.11}
\]

Applying Equation 4.9 and the fact that \( g_{m,1} = \frac{1}{R_L} \) and adding the two voltage error variances we get the total error variance in the differential output as

\[
\Delta \bar{V}^2_{tot} = \Delta \bar{V}^2_n = 2 \cdot \Delta \bar{V}^2_{on,1,2} + \Delta \bar{V}^2_{on,3,4} = \frac{KT}{C_L} \left( 4\gamma_1^2 + 2\gamma_3 a_v \right) ; \quad a_v = g_{m,3} R_L \tag{4.12}
\]

The factor 2 in Equation 4.12 is to include the noise effect of transistors M6 and M7. From figure of merit defined earlier we can write the timing error variance of the delay cell as shown below

\[
\Delta t_d^2 = \frac{\Delta \bar{V}^2_n}{V_{\text{SW}}^2} \frac{t_d^2}{t_{\text{SW}}^2} = \frac{KT}{C_L} \left( 4\gamma'_p + 2\gamma'_n g_m R_L \right) \left( \frac{C_L}{I_{\text{SS}}} \right)^2 \tag{4.13}
\]
4.2.3 Jitter in VCO, and PLL

To determine the jitter injected by the VCO in the PLL some assumptions are adopted to simplify the analysis. First the VCO and reference jitter are assumed to be white gaussian in nature with zero mean [21], [12]. Moreover the noise sources in successive delay cells are independent. So the cycle to cycle timing jitter variance injected by the VCO equals

\[
\Delta t_{VCO}^2 = 2N \Delta t_d^2
\]

(4.14)

For multiple cycles of oscillation the total timing error variance relative to reference transition at time t=0 is given by

\[
\Delta t_{tot}^2 = \frac{\Delta t_{VCO}^2}{T} t
\]

(4.15)

The previous equation shows that we have a linear accumulation of timing jitter. It is shown in some publications [10], [12], [21] that the loop acts to correct the resulting phase error. The timing error will be reduced with a settling time inversely proportional to the loop bandwidth. So

\[
\Delta t_{PLL}^2 = \alpha^2 \Delta t_{VCO}^2
\]

(4.16)

where \( \alpha = \sqrt{\frac{\omega_{ref}}{2W_{PLL}}} \) and \( W_{PLL} = K_{pd} K_{vCO} K_f \) which is the loop bandwidth [12]. An optimization of the loop bandwidth to minimize the total r.m.s jitter is done by Kim et al, [12] and the optimal bandwidth obtained is

\[
W_{OPT} = \frac{1}{NT} \left( \frac{\Delta t_{d, rms}}{M} + \frac{T^2}{2\pi} K_{vCO} \Delta V_{4, rms} \right)
\]

\[
\frac{\Delta t_{ref, rms}}{K_{pd}} + \frac{T}{2\pi} \frac{\Delta I_{3, rms}}{K_{pd}}
\]

(4.17)
\( \Delta V_4, \Delta I_3 \) are the noise r.m.s values for the loop filter and the phase detector respectively. This noise contribution is insignificant as mentioned before, so if we take into consideration the jitter due to VCO and reference input jitter only then the optimum loop bandwidth will be

\[
W_{OPT} = \frac{1}{T} \left( \frac{\Delta f_{d, rms}}{\Delta f_{ref, rms}} \right)
\] (4.18)

\( N=M=1 \) in our case where \( M \) and \( N \) are the frequency division performed on the input signal frequency and VCO frequency respectively. It is shown by Kim et al, [12] from practical measurements that at frequency of 900MHz \( \Delta f_{ref, rms} = 5 \Delta f_{VCO, rms} \) which results in \( W_{OPT} = \frac{1}{5T} \).

### 4.3 Summary

In this chapter the systematic and random timing errors have been discussed. The jitter analysis in the PLL has been investigated starting from the jitter in the delay cell due to device thermal noise, and proceeding to the jitter in the VCO. Finally the jitter in the PLL due to the jitter inserted by the VCO and the input signal jitter has been derived. The optimum loop bandwidth to minimize the PLL jitter has been investigated.
CHAPTER 5. SIMULATION RESULTS

The complete clock recovery circuit schematic and layout are shown at the end of this chapter. The circuit was designed using 0.6µm Nwell CMOS process available through MOSIS and designated as HP process. Process model parameters appear in the appendix. Transient simulation was performed for the circuit using level 13 model and the HSPICE simulator. Unless stated, all simulations were for the nominal process parameters operating at a nominal temperature of T=25°C. Realistic drain and source areas and perimeters were included for all devices to model the parasitic capacitors.

The VCO has five delay cells in a ring. The VCO gain, \( K_{\text{vco}} = \frac{\Delta \omega}{\Delta V_{\text{cm}}^\text{vco}} \) is measured from simulation. Figure 5.1 shows the VCO output frequency vs. the VCO control voltage for a control voltage range from 850mV to 1.7V. From this simulation, operation in the frequency range 680MHz to 1.21GHz was obtained. The VCO gain is found to be 4.469\( \times 10^9 \) rad/Volt.

![Figure 5.1. VCO output frequency vs. input control voltage.](image-url)
The other hand the phase detector gain $K_{pd} = \frac{I_{avg}}{\Delta \Phi}$ was measured from simulation for an input signal frequency of 1GHz. The phase detector gain is found to be 0.1273mA/rad. The simulation result for the differential to single ended 50% duty cycle converter of Figure 3.2 is shown in Figure 5.2. The input signal is a differential sinusoidal signals with 500MHz, amplitude 1 volt peak to peak, and 2 volts DC offset to represent the 1GHz NRZ digital data at the optical receiver side. Figure 5.2 shows that the output is in CMOS logic format, rail to rail with 50% duty cycle. The circuit was also simulated at 1GHz sinusoidal input to represent 1GHz RZ data, and again the circuit shows proper data format conversion.

![Figure 5.2 the simulation result for the differential to single ended simulation](image)

The whole clock recovery circuit was simulated at 1GHz data rate. The results of simulation that are typical of the locking characteristics of the structure are shown in Figure 5.3 for an input data sequence. The input is NRZ data and the recovered clock must have a period that is equal to 1 bit-time of the input data. Figure 5.3.a shows simulation results when the loop acquires lock to the data clock. In this simulation the oscillator was running initially at 750MHz. Figure 5.3.b shows the loop maintaining lock. Figure 5.3.a shows that the acquisition time is in the order of $10T_{lo}$ where $T_{lo}$ is the period of the local oscillator. In Figure 5.3.a it is apparent that the frequency lock is achieved very quickly but phase-lock denoted by $t$-lock is slower. But due to the PFD simple structure with no feedback the
locking process is very fast if compared with the known PFDs. Figure 5.3.b shows circuit operation for an input of random binary data sequence where the circuit maintains lock to the input data transitions. The simulation of the circuit working as a frequency multiplier is shown in Figure 5.4. In this case the input frequency is 250MHz while the VCO frequency is

![Figure 5.3. a, b](image)

(a) Start of lock, (b) Maintaining lock.

![Figure 5.4](image)

Figure 5.4 Frequency multiplication
1GHz. The challenge with high order frequency multiplication is that the number of transitions at the input is low relative to the VCO frequency which means that the circuit will see the input clock as long sequences of zeroes and ones.

The circuit was also simulated in the temperature range 0-100°C. The lock process becomes slower as temperature goes higher. For example, at 25°C it takes around $10T_{lo}$ for the circuit to lock to the input data transitions, while at 100°C it takes around $30T_{lo}$. The lock range and capture-range are measured by simulation and their values appear in Table 1.

Table 1 Simulation results

<table>
<thead>
<tr>
<th>Frequency of operation</th>
<th>1 GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lock range</td>
<td>830MHZ-1.17GHz</td>
</tr>
<tr>
<td>Capture range</td>
<td>925MHz-1.075GHz</td>
</tr>
<tr>
<td>Temp range</td>
<td>0-100°C</td>
</tr>
<tr>
<td>Loop BW</td>
<td>200MHz</td>
</tr>
<tr>
<td>Natural freq. $\omega_n$</td>
<td>$754 \times 10^6$ rad/sec</td>
</tr>
<tr>
<td>Filter Q-factor</td>
<td>0.8327</td>
</tr>
</tbody>
</table>

Table 1 also includes simulation measured parameters of the loop bandwidth, natural frequency, and loop filter quality factor (Q). Results from one of the simulation-runs used to measure the lock range is shown in Figure 5.5 where we have used another VCO to generate the input signal. Once the local VCO locks to the reference signal we start to change the
frequency of the reference VCO and observe the range over which the circuit will be able to maintain lock.

Finally a stability test was done by simulation as shown in Figure 5.6, where we have used a square wave generator as the reference input and at a certain moment a step delay has been inserted to observe the settling of the circuit. One of the simulation results is shown in Figure 5.8 where a step delay of $0.3T_0$ is inserted where the control voltage goes down as a response to the phase delay, and then it adjusts its level back as it locks to the data transitions with no oscillation in the control voltage. The complete clock recovery circuit is shown in Figure 5.7.

The simulation result for the temperature sensor is shown in Figure 5.8. The figure shows a linear relation between the output DC voltage and the temperature. The gain of the temperature circuit is measured using the simulator and found to be $5\text{mV/degree C.}$
Figure 5.6 Stability test

Figure 5.7 The complete clock recovery circuit schematic
Finally the transistor sizes for the major blocks are as follows

1. For the delay cell tail current transistors are two NMOS transistors with $W/L=42\mu m/0.6\mu m$, two differential pair transistors have $W/L=21\mu m/0.6\mu m$, and active load six PMOS transistors each have $W/L=21\mu m/0.6\mu m$.

2. For the charge pump circuit we have three NMOS current sink transistors with $W/L=15\mu m/0.9\mu m$, the PMOS current mirrors have three transistors with $W/L=30\mu m/0.9\mu m$, two PMOS transistor switches with $W/L=30\mu m/0.6\mu m$, and finally two NMOS transistor switches with $W/L=15\mu m/0.6\mu m$.

3. The AND logic gates have NMOS transistors with $W/L=12\mu m/0.6\mu m$, and PMOS transistors with $W/L=24\mu m/0.6\mu m$.

4. The Buffer have a differential pair with NMOS tail current transistor $W/L=45\mu m/0.6\mu m$, differential pair NMOS transistors with $W/L=21\mu m/0.6\mu m$, and active load PMOS transistors with $W/L=42\mu m/0.6\mu m$, The following two inverters have two NMOS transistors
with \( W/L = 30\mu/0.6\mu \) and \( 60\mu/0.6\mu \), and two PMOS transistors with \( W/L = 75\mu/0.6\mu \) and \( 120\mu/0.6\mu \). The complete circuit layout is shown in Figure 5.9.

5.2 Conclusion

PLLs and clock recovery circuits have important rule in communication and microprocessor systems. The demand on high speed PLLs have been increased. The PFD is the slowest block in the PLL circuit. In this work we have shown that by using different phase shifted versions of the VCO output we can build a very fast PFD that has a very simple structure which is no longer the slow component in the PLL. The circuit implementation shows that the proposed PFD allows the PLL to work at a very high speed without the use of frequency multipliers or dividers. A new temperature sensor and temperature compensation technique is also shown.

5.3 Future work

Even though the proposed PFD is implemented in a clock recovery circuit. Future work will include fabrication and test on the circuit, proposing additional circuitry to reduce the effects of both the deterministic and random timing errors. Adaptive techniques can be implemented to choose different phase shifts to speed-up the operation of the circuit while tracking the input carrier by choosing big phase shifts, or to reduce the allowed jitter in the circuit when locked by choosing small phase shifts between the leading and the lagging harmonics.
Figure 5.9 The clock recovery circuit layout
APPENDIX: PARAMETERS OF MODEL LEVEL=13

The model level 13 for both NMOS, and PMOS transistors are listed below

```
..MODEL CMOSN NMOS
level=13 vfb0=-667.77E-3 lvfb=-9.88E-3 &
wvfb=-32.94E-3 phi0=860.65E-3 lphi=0.0 &
wphi=0.0 k1=817.94E-3 lk1=-46.57E-3 &
wk1=47.58E-3 k2=42.58E-3 lk2=35.26E-3 &
wk2=-2.77E-3 eta0=-61.46E-6 leta=18.91E-3 &
weta=-11.85E-3 muz=583.83 d10=140.29E-3 &
dw0=507.56E-6 u00=329.59E-3 lu0=97.75E-3 &
wu0=-93.23E-3 ul=19.94E-3 ul1=36.20E-3 &
wul=-2.87E-3 x2m=12.91 lx2m=-8.28 &
x2m=6.91 x2e=754.03E-6 lx2e=-3.43E-3 &
wv2e=518.76E-3 x3e=237.99E-6 lx3e=-1.61E-3 &
w3e=-5.40E-3 x2u0=-6.36E-3 lx2u1=-3.86E-3 &
w2u0=5.33E-3 x2u1=-568.01E-6 lx2u1=1.23E-3 &
w2u1=285.10E-6 mus=684.17 lms=25.43 &
wms=921.34E-3 x3ms=4.83 lx3ms=4.02 &
w3ms=-5.34 x2ms=4.89 lx2ms=-1.91 &
x2ms=7.94 x3u1=7.21E-3 lx3u1=-137.19E-6 &
x3u1=-3.71E-3 toxm=10.00E-3 tref=25.00 &
vdem=5.00 cdgdom=363.00E-12 cgsom=363.00E-12 &
cgbom=452.50E-12 xpart=1.00 deem=0.0 &
dum2=0.0 n0=1.00 ln0=0.0 &
w0=0.0 nb0=0.0 lnb=0.0 &
wm=0.0 nd0=0.0 lnd=0.0 &
wm0=0.0 k2lim=0.0 version=95.20 &
rs=2.40 cjm=773.21E-6 cjw=290.00E-12 &
ijs=10.00E-9 pj=800.00E-3 pjw=800.00E-3 &
mj0u=1.10 mjw=260.00E-3 wdf=0.0 &
ds=0.0 &
tcv=1.00E-3 ltcv=0.0 wtcv=0.0 &
bex=-1.50 lbex=0.0 wbex=0.0 &
fx0=0.0 lfx0=0.0 wfx0=0.0 &
trs=0.0 ltrs=0.0 wtrs=0.0 &
trd=0.0 ltrd=0.0 wtrd=0.0
```

```
..MODEL CMOSP PMOS
level=13 vfb0=-65.97E-3 lvfb=-17.83E-3 &
wvfb=-2.45E-3 phi0=768.18E-3 lphi=0.0 &
wphi=0.0 k1=285.65E-3 lk1=-16.46E-3 &
wk1=30.89E-3 k2=-66.25E-3 lk2=24.95E-3 &
wk2=462.78E-6 eta0=-7.91E-3 leta=19.23E-3 &
weta=-2.35E-3 muz=141.70 d10=214.00E-3 &
dw0=534.41E-3 u00=195.41E-3 lu0=62.21E-3 &
wu0=-59.47E-3 ul=8.56E-3 ul1=13.95E-3 &
wul=765.80E-6 x2m=6.79 lx2m=-1.44 &
x2m=656.48E-3 x2e=108.48E-6 lx2e=-1.25E-3 &
```

wx2e=97.72E-6 x3e=433.47E-6 lx3e=142.45E-6 &
wx3e=-1.72E-3 x2u0=8.74E-3 lx2u0=-1.32E-3 &
wx2u0=478.07E-6 x2u1=306.83E-6 lx2u1=441.19E-6 &
wx2u1=349.20E-6 mus=147.75 lms=17.86 &
wx3ms=124.74E-3 x3ms=-318.66E-3 1x3ms=2.80 &
wx3ms=1.71 x2ms=6.09 lx2ms=-161.40E-3 &
wx2ms=1.25 x3ul=-1.23E-3 lx3ul=106.18E-6 &
wx3ul=1.08E-3 toxm=10.00E-3 tref=25.00 &
vddm=5.00 cgaom=554.00E-12 cgsom=554.00E-12 &
cgbom=467.04E-12 xpart=1.00 dum1=0.0 &
dum2=0.0 n0=1.0 ln0=0.0 &
wn0=0.0 nb0=0.0 lnb=0.0 &
wnb=0.0 nd0=0.0 lnd=0.0 &
wnd=0.0 k2lim=0.0 version=95.20 &
rsdm=2.10 cjm=931.91E-6 cjw=156.37E-12 &
ijs=10.00E-9 pj=850.00E-3 pjw=850.00E-3 &
mj0=487.07E-3 mjw=478.48E-3 wdf=0.0 &
ds=0.0 &
tcv=-1.0e-3 ltcv=0.0 wtcv=0.0 &
bex=-1.50 lbex=0.0 wbex=0.0 &
fex=0.0 lfbex=0.0 wfbex=0.0 &
trs=0.0 ltrs=0.0 wtrs=0.0 &
trd=0.0 ltrd=0.0 wrd=0.0
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