Design of 1 V bulk-driven programmable gain instrumentation amplifier

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Design of 1 V bulk-driven programmable gain instrumentation amplifier

by

Tao Han

A thesis submitted to the graduate faculty
in partial fulfillment of the requirements for the degree of

MASTERTOF SCIENCE

Major: Electrical Engineering
Major Professor: Dr. Edward K.F. Lee

Iowa State University
Ames, Iowa
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This is to certify that the Master's thesis of
Tao Han
has met the thesis requirements of Iowa State University

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CHAPTER 1

INTRODUCTION

1.1 Overview

Recent years, the interest towards low-power and low-voltage integrated circuits (IC) has considerably grown in the industry. Portable applications have become popular in all market and consequently increase the demand for the low-power and low-voltage applications [1]. Lowering supply voltage is also the consequence of technology scaling. Since CMOS technology has shown its advantage, especially in cost saving, in the case when a very large silicon area is needed, it has been widely used in a variety of low voltage applications [2].

The trends of IC technology suggest that future implementation of mixed analog-digital circuits using standard CMOS technology will have power supplies less than 1.5V [3]. On the other hand, the threshold voltage of future standard CMOS technologies may not decrease much below what is available today. As a result, it is important to develop circuit techniques that permit existing CMOS to implement analog circuits at power supply voltage as low as 1 volt.

Solutions to this low supply voltage challenge have been made, such as, 1) reduction of threshold voltage from 0.7V to 0.3V-0.4V, or 2) use of voltage multipliers [13]. The use of low-threshold devices is a high-cost solution since it requires a special technology. For voltage multipliers, since they need to generate clock phases higher than the supply voltage to drive critical switches, therefore they can not be used for scaled-down technologies.
Obviously, threshold voltage is the major limitation for implementing analog circuits at 1 V power supply. In order to perform any signal processing, the MOS transistor must be turned on, which means that for CMOS technology the power supply must satisfy the following requirement for strong inversion operation:

\[ V_{DD} + |V_{SS}| \geq V_{GS} = V_{DSsat} + |V_T| \]  \hspace{1cm} (1-1)

where, \( V_{DD} \) is the positive power supply, \( V_{SS} \) is the negative power supply, and \( V_T \) is the magnitude of the largest threshold of the NMOS or PMOS transistors, normally in the range of 0.6V – 0.8V for a 1.2µm process. Further, if the MOS transistor is gate-driven, the requirement for supply voltage becomes

\[ V_{DD} + |V_{SS}| \geq V_{GS} = V_{DSsat} + |V_T| + |V_{signal} \]  \hspace{1cm} (1-2)

Consider a simple transmission gate, it requires the supply voltage at least equal to the sum of the magnitudes of the p-type and n-type threshold voltages.

\[ V_{DD} + |V_{SS}| \geq |V_Tp| + |V_Tn| \]  \hspace{1cm} (1-3)

For a 1.2µm process, the sum will be in the range of 1.2V – 1.6V. Clearly, it does not suitable for operating at 1 volt supply voltage. To overcome this conflict, circuit techniques must be developed that are compatible with this future standard CMOS technology trends.

1.2 The Bulk-Driven MOSFET

Figure 1-1 illustrates a PMOS cross section structure with an n-well process. Bulk-Driven technique can only be applied to the MOSFET that can be fabricated in its own separate well. The parasitic lateral (QP) and vertical (QV) pnp type bipolar junction transistors are also shown.
The operation of the bulk-driven MOSFET is much like a JFET. The inversion layer forming the conduction channel beneath the gate is established by connecting the gate terminal to a fixed voltage of sufficient magnitude to form a channel. The conduction channel of the JFET is the inversion layer of the MOSFET beneath the gate structure. The thickness of the depletion layer beneath the source, inversion layer, and drain of the MOSFET is determined by the bulk potential [4]. By varying the bulk-source voltage, the thickness of this depletion layer changes, and the inversion layer through which the drain current flowing is modulated. The channel current can be modulated with very small DC
values of the bulk-source potential resulting in a device that is useful for low voltage applications.

The performance of the bulk-driven MOSFET is somehow similar to that of the gate-driven MOSFET. Compared with the gate-driven scheme, the physical size of the bulk-driven MOSFET is a major concern. This can be minimized through the layout techniques. The 1/f noise of the bulk-driven MOSFET is approximately equal to that of a gate-driven MOSFET [3].

The first-order theory [5] gives the dependence of the drain current, \( I_D \), of a MOSFET as

\[
I_D = \frac{KW}{L} (V_{GS} - V_T - \frac{n}{2} V_{DS}) V_{DS}, \quad V_{DS} \leq V_{DSAT}. \tag{1-4}
\]

and

\[
I_D = \frac{KW}{2nL} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}), \quad V_{DS} \geq V_{DSAT}. \tag{1-5}
\]

where

\[
n = 1 + \frac{C_{BC}}{C_{OX}} + \frac{qNFS}{C_{OX}} = 1 + \frac{\gamma}{2\sqrt{\phi_j - V_{BS}}}
\]

\[
= 1 + \eta = 1 + \frac{g_{mb}}{gm} \tag{1-6}
\]

and

\[
V_{DSAT} = \frac{V_{GS} - V_T}{n} \tag{1-7}
\]
The parameters in (1-6) are identical with standard SPICE parameters for MOSFETs. Further, in order to describe bulk-source operation, the \( V_T \) term in (1-4) and (1-5) can be expanded as

\[
I_D = \frac{K'W}{L} (V_{GS} - V_{T0} - \gamma \sqrt{2\phi_F} - V_{BS} + \gamma \sqrt{2\phi_F} - \frac{n}{2} V_{DS}) V_{DS}, \quad V_{DS} \leq V_{DSAT}. \quad (1-8)
\]

and

\[
I_D = \frac{K'W}{2nL} (V_{GS} - V_{T0} - \gamma \sqrt{2\phi_F} - V_{BS} + \gamma \sqrt{2\phi_F})^2 (1 + \lambda V_{DS}), \quad V_{DS} \geq V_{DSAT}. \quad (1-9)
\]

These equations are used to predict the theoretical drain current of the bulk-driven MOSFETs. However, test results suggest that they need to be reexamined to permit better correlation between experimental and theoretical results [6]. It is found that the Berkeley short-channel insulated-gate (BSIM) model can model bulk-source operation reasonably well. Figure 1-2 (a), (b) illustrates the \( I_D \) versus \( V_{DS} \) plot for both bulk-driven and gate-driven case.

The bulk-driven MOSFET has several advantages. The most significant advantage is the depletion characteristic which allows zero, negative, and positive values of bias voltage to achieve the desired DC currents. This will lead to larger input common-mode ranges that could not otherwise be achieved at low power supply voltage. Figure 1-3 shows the \( I_D \) versus \( V_{BS} \) and \( V_{GS} \) plot.
Figure 1-2. $I_D$ versus $V_{DS}$ plot
Another interesting advantage of the bulk-driven MOSFET is the use of the poly gate to modulate the bulk-driven MOSFET. Because the gate can totally shut off the channel, the on/off ratio of the bulk-driven MOSFET modulated by the gate is very large. This implies that a low voltage switch can be realized by turning on or shutting off the gate. This characteristic is very important in the low power supply applications. Because a transmission gate will not work at the power supply voltage at 1 volt or below and due to the threshold voltage limitation, a single NMOS or PMOS switch has a poor performance at such a low supply voltage as well. Therefore a bulk-driven MOSFET switch becomes ultimate useful in the low power supply application.
A potential advantage of the bulk-driven MOSFET is that the small signal transconductance, $g_{mb}$, can in theory be larger than the MOSFET transconductance, $g_m$. This can be demonstrated by examining the expression for $g_{mb}$ given below:

$$g_{mb} = \frac{di_D}{dV_{BS}} = \frac{\eta g_m}{2\sqrt{2}\phi_F - V_{BS}} \quad (1-10)$$

It is clear that the bulk-driven MOSFET transconductance can exceed the gate-driven MOSFET transconductance if

$$V_{BS} \geq 2\phi_F - 0.25\gamma^2 = 0.5V \quad (1-11) [6]$$

Certainly, this is under the assumption that there will be enough current flowing in the bulk-source junction under these conditions.

One disadvantage of the bulk-driven MOSFET is its fairly large input capacitance. Compare the frequency response of the bulk-driven MOSFET to that of a gate-driven MOSFET, the gate-driven MOSFET frequency response capability is described by its transitional frequency, $f_T$.

$$f_{T, \text{gate-driven}} = \frac{g_m}{2\pi C_{gs}} \quad (1-12)$$

where, $C_{gs}$ is the gate-to-source capacitance [5]. At frequency beyond $f_T$, the device no longer provides signal gain. Likewise, for the bulk-driven MOSFET, the transitional frequency, $f_T$, can be described as

$$f_{T, \text{bulk-driven}} = \frac{g_{mb}}{2\pi(C_{gs} + C_{bsub})} = \frac{\eta g_m}{2\pi(C_{gs} + C_{bsub})} \quad (1-13)$$

where, $\eta$ is the ratio of $g_{mb}$ to $g_m$ and typically has a value in the range of 0.2 to 0.4, $C_{bs}$ is the bulk-to-source capacitance, and $C_{bsub}$ is the well-to-substrate capacitance. According to [7],
for an interdigitated layout, $C_{bs} = 0.18C_{gs}$ for the NMOS. The proportionality of $C_{sub}$ to $C_{gs}$ is approximated using the bulk area and periphery, the well doping density, the substrate doping density, and applied voltage bias across the bulk-substrate pn junction. For digital CMOS technology, the well and substrate doping density are approximately $10^{16}$ cm$^{-3}$ and $10^{15}$ cm$^{-3}$, respectively [8]. Similar to the $C_{bs}$ estimate, estimate for $C_{sub}$ using the doping information of [8] with the zero-bias condition, $C_{sub}$/area estimated value is 0.087 fF/µ$^2$. With the reverse-bias of the well-substrate increase, the $C_{sub}$ reduces accordingly [8].

Once a bulk area is selected, a comparison to $C_{gs}$ can be made for a given MOSFET. A reasonable estimate of bulk area is approximately three times the source/drain diffusion area of a MOSFET. For a minimum gate length, $L_{min}$, device with a gate width $W$, the bulk area is approximately $12 \times W \times L_{min}$. If the bulk-to-substrate sidewall depletion capacitance is considered, the resulting capacitance should be multiplied by 2 conservatively. For saturated strong inversion MOSFET operation and using the previously mentioned approximations it can be shown that

$$f_{T, bulk-driven} = \frac{\eta}{[(0.18 + 2 \times 12 \times 0.087) / \frac{2}{3}]} \quad f_{T, gate-driven} = \frac{\eta}{3.8} f_{T, gate-driven} \quad (1-14)$$

Another potential disadvantage of the bulk-driven MOSFET is noise. The channel noise current is identical in both the gate-driven and bulk-driven cases. However, the gain factor referring the channel noise current to the input distinguishes the bulk-driven case from the gate-driven case. Furthermore, the bulk-driven MOSFET can contribute additional thermal noise. The bulk-referred mean-square noise voltage expression for the MOSFET is given by [9].
\[ \nu^2_{n_{\text{bulk}}} = \left( \frac{8kT(1 + \eta)}{3\eta^2 g_m} + \frac{KF}{2fC_{\text{ox}}WL\eta^2} + 4kT \left( \frac{1}{N} \right)^2 \times \left( \sum_{i=1}^{N} R_{bi} + \frac{1}{\eta^2} \sum_{i=1}^{N} R_{gi} \right) \right) \Delta f \] (1-15)

where, \( N \) is the number of gate finger within an interdigitated MOSFET structure, \( R_{bi} \) is the effective series bulk resistance for the \( i \)th gate. MOSFET white noise and flicker noise referred to the bulk terminal are described by the first and second terms, respectively. The last two terms describe the thermal noise attributed to bulk-metal and gate-metal resistance. The \( N^2 \) coefficient seems a promising result. In order to minimize bulk-referred noise for the bulk-driven MOSFET, the physical layout of the device should use bulk contacts generously. The contacts need to be as close as possible to each gate fingers. This arrangement can minimize the noise contribution of the bulk resistance determined by well sheet resistance.
CHAPTER 2

DESIGN OF 1V BULK-DRIVEN OPERATIONAL AMPLIFIER

The objective of this thesis is to design and implement a programmable gain instrumentation amplifier that can be operated at 1 V supply voltage in standard technology. This task also address the challenges of a 1 V CMOS operational amplifier (Op Amp) design, as the Op Amp is the main building block of the instrumentation amplifier. Operational amplifier is a fundamental building block in a wide range of analog and mixed-signal circuits. However, many of the existing techniques used in CMOS Op Amps does not suitable for low-voltage operation. One of the reasons is that a low-voltage differential pair is difficult to implement in digital CMOS technology with a good input common-mode range (ICMR). This chapter focuses on the design of 1 V Op Amp with bulk-driven differential pair technique. The design of the instrumentation amplifier will be discussed in the next chapter.

2.1 Bulk-Driven Differential Pair

The bulk-driven differential pair (BDDP) is shown Figure 2-1. As an example, the PMOS input pair is shown. The gates of both devices are tied to $V_{SS}$ so that an inversion layer channel is formed within each MOSFET. In addition, each MOSFET must have isolated individual well so that the input signal can be applied to the well directly. When a differential voltage signal is applied between the bulk terminals of M1 and M2, through the bulk-to-channel transconductance action of the pair, the differential input signal causes the current to be steered between M1 and M2 such that
where, $G_{mb}$ is the differential transconductance and $v_{in}$ is the differential input voltage signal.

From equation (1-10), we know that $g_{mb} = \frac{g_m}{2\sqrt{2\phi_F - V_{BS}}}$, and knowing from Figure 1-3, $V_{BS} = V_{cm} - V_s$, therefore the differential transconductance of the input pair can be described by

$$G_{mb} = \frac{g_m}{2\sqrt{2|\phi_F| - V_{cm} + V_s}} = \frac{\sqrt{\mu_p Cox(W/L)I_{tail}}}{2\sqrt{2|\phi_F| - V_{cm} + V_s}}$$

(2-2)

where, $\mu_p$ is the PMOS mobility, $V_{cm}$ is the common mode voltage to both bulk terminals, $V_s$ is the source-coupled node voltage, and $I_{tail}$ is the tail current of the differential pair. One advantage of the bulk-driven differential pair is that $V_{cm}$ can move rail-to-rail thereby...
providing the rail-to-rail ICMR. This is because the MOSFET bulk-source junction is still able to provide sufficient impedance while the source potential is higher than the bulk potential to some degree. Within 1-volt power supply, \( V_{cm} \) can not forward bias the bulk-source junction enough to strongly turn on the parasitic vertical and lateral BJTs, so that a fairly high input impedance of the input pair is guaranteed.

Figure 2-2 qualitatively illustrates the region of the ICMR when the bulk-source junctions are forward biased case. As shown in Figure 2-2, \( V_1 \) represents to the portion of ICMR where the bulk-source junctions of M1 and M2 are forward biased provided the threshold voltage is constant. However in the real case, the threshold voltage changes with common-mode voltage. The threshold voltage will decrease with the forward biasing of the bulk-source junction. As a result, \( V_s \) follows \( V_{cm} \) to a degree. For a PMOS pair, as \( V_{cm} \) moves beyond mid-supply towards \( V_{ss} \), the source-coupled node, \( V_s \), moves towards \( V_{ss} \) as well. Consequently, \( V_2 \) becomes the actual region of ICMR over which the bulk-source junctions of M1 and M2 are forward biased. The maximum forward biasing of the M1, M2 bulk-source junction is \( V_{bs} = -500\text{mV} \) when \( V_{cm} = V_{ss} \). This is the limit of bulk-source forward biased for maintaining a MOSFET bulk terminal as a high impedance node.

Figure 2-3 shows the simulation of how \( V_s \) changes with \( V_{cm} \). The results were simulated using Cadence® Analog Artist with AMI® 1.2\( \mu \)m n-well CMOS technology. The circuit schematic for the simulation is shown in Figure 2-4. The aspect ratios of M1 and M2 in all case are 540\( \mu \)m/1.8\( \mu \)m with the power supply of \( \pm 0.5\text{V} \) and tail current equals to 50\( \mu \)A, 100\( \mu \)A, 150\( \mu \)A, and 200\( \mu \)A, respectively. The p-substrate is tied to \( V_{ss} = -0.5\text{V} \). Figure 2-5
Figure 2-2. ICMR of the bulk-driven differential pair for M1, M2 are forward bias

Figure 2-3. Plot of $V_s$ versus $V_{cm}$ for PMOS bulk-driven differential pair
Figure 2-4. Schematic for simulation of Bulk-driven differential pair

shows the simulated transconductance characteristic ($I_d$ versus $V_{in}$) of the bulk-driven differential pair for four different tail currents. The common-mode voltage is set as halfway between the two supply rails.

As shown in Figure 2-5, the slope of each curves at the center point stands for the transconductance of the circuits, varying from -25 $\mu$S for $I_{tail} = 50 \mu$A to -100 $\mu$S for $I_{tail} = 200 \mu$A. In addition, the transconductances of bulk-driven differential pair are plotted as a function of common-mode voltage in Figure 2-6.

In Figure 2-6, a second-order polynomial curve fitting technique is used in order to draw the curves. Using the transconductance of $V_{cm} = 0.0V$ for each tail current as the nominal values, the transconductances of PMOS bulk-driven differential pair at $V_{cm} = V_{SS}$ are 31.1%, 35.6%, 37.6%, and 38.7% below the nominal value for the tail current equals to
Figure 2-5. Transconductance characteristic of PMOS bulk-driven differential pair

Figure 2-6. The influence of common-mode voltage on transconductance of PMOS bulk-driven differential pair
50µA, 100µA, 150µA, and 200µA, respectively. The transconductances of PMOS bulk-driven differential pair at $V_{cm} = V_{DD}$ are 1.3%, 6%, 10.4%, and 14.3% above the nominal value for the tail current equals 50µA, 100µA, 150µA, and 200µA, respectively. This behavior of $G_{mb}$ as a function of common-mode voltage is also predicted in equation (2-2). Taking the derivative of equation (2-2) with respect to $V_{cm}$, we have

$$\frac{\partial G_{mb}}{\partial V_{cm}} = \frac{V}{2} g_m (2|\phi_r|-V_{cm}+V_s)^{-3/2}$$ \hspace{1cm} (2-3)

This presumably explains the reason of the variation of $G_{mb}$ at $V_{cm} = V_{SS}$ much higher than that of at $V_{cm} = V_{DD}$ case. Further more, the behavior of $V_s$ changing with $V_{cm}$ which shown in Figure 2-2 also needs to be taken into account. In Figure 2-2, at $V_{cm} = V_{DD}$, the differences of $V_{cm}$ and $V_s$, for all four tail currents case reach the minimum values whereas the differences of $V_{cm}$ and $V_s$ for all four tail currents case reach the maximum values at $V_{cm} = V_{SS}$. Thus makes the variation of $G_{mb}$ at $V_{cm} = V_{SS}$ much higher than that of at $V_{cm} = V_{DD}$ case.

### 2.2 Parasitic Capacitance of the Bulk-Driven Differential pair

The frequency response of bulk-driven differential pair is mainly determined by its input and output parasitic capacitance. The dominant parasitic capacitors of the bulk-driven differential pair are shown in Figure 2-7. In addition, the equivalent input capacitance ($C_{in,eq}$) and the equivalent output capacitance ($C_{L,eq}$) are illustrated as well. $R_L$ represents an arbitrary load of this circuit. For comparison, a similar illustration for a gate-driven case is shown in Figure 2-8.

For the bulk-driven differential pair,
\[(C_{in,eq})_{bulk-driven} = C_{bs} + C_{bsub} + (1 + g_{mbR_L})C_{bd} \quad (2-4)\]

and

\[(C_{L,eq})_{bulk-driven} = C_{gd} + C_{bd} \quad (2-5)\]

where, \(g_{mbR_L}\) is the inverting voltage gain across each \(C_{bd}\) that causing Miller Effect [10].

For the gate-driven differential pair,

\[(C_{in,eq})_{gate-driven} = C_{gs} + (1 + g_{mbR_L})C_{gd} \quad (2-6)\]

and,

\[(C_{L,eq})_{gate-driven} = C_{gd} + C_{bd} \quad (2-7)\]

where, \(g_{mbR_L}\) is the Miller multiplying voltage gain across each \(C_{gd}\).

Figure 2-7. Dominant parasitic capacitance of the bulk-driven differential pair
The equivalent load capacitance in both cases is assumed to be equal. If the two differential pairs are equivalently loaded, the pole at their respective outputs is identical. There is a significant difference in input capacitance. In fact, in terms of input capacitance, there is no common capacitive elements shared between the two circuits. Furthermore, due to the factor of $\eta$ difference in voltage gain between the two circuits, there is a factor of $\eta$ difference in Miller Effect influencing each input capacitance. Since $\eta = \frac{g_{mb}}{g_m}$ is less than 1, this imply that the influence of the Miller Effect to the bulk-driven differential pair is less than that of the gate-driven differential pair. This means that the voltage gain of bulk-driven
differential pair is less than that of gate-driven differential pair for the same tail circuit. Same conclusion is also made in [9].

2.3 Low Voltage Self-Cascode Current Mirror

The operation of the low voltage self-cascode current mirror [11] is described in Figure 2-9. As shown in Figure 2-9, the bias voltage $V_{\text{bias}}$, is generated by the bias current $I_{\text{bias}}$ flowing into the diode connection of device M4 with M3 in series. Both device M1 and M2 are biased by the same voltage $V_{\text{bias}}$ to form a self-cascode current mirror. The channel length $L_1$ of M1 is made longer than the channel length $L_2$ of M2. The gate dimensions of M3 and M4 are identical to that of M1 and M2, respectively. For device M1, the bias voltage is given as

$$V_{\text{bias}} = V_{GS1} = V_{T1} + V_{\text{SAT1}}$$  \hspace{1cm} (2-8)

where $V_{T1}$ is the threshold voltage of M1, and $V_{\text{SAT1}}$ is the saturation voltage of M1.

For device M2, the gate-source voltage can be express as

$$V_{GS2} = V_{\text{bias}} - V_{\text{drain}} = V_{T2} + V_{\text{SAT2}}$$  \hspace{1cm} (2-9)

where $V_{T2}$ is the threshold voltage of M2, and $V_{\text{SAT2}}$ is the saturation voltage of M2.

Combine (2-8) with (2-9), we have

$$V_{\text{bias}} - V_{\text{drain}} = V_{T1} + V_{\text{SAT1}} - V_{\text{drain}} = V_{T2} + V_{\text{SAT2}}$$

which yield,

$$V_{\text{drain}} = V_{T1} - V_{T2} + V_{\text{SAT1}} - V_{\text{SAT2}}$$  \hspace{1cm} (2-10)

To let device M1 operated in the saturation region, the drain of M1 must satisfy the condition that

$$V_{\text{drain}} = V_{\text{SAT1}}$$  \hspace{1cm} (2-11)
From (2-10) that this condition is met if
\[ V_{SAT2} = V_{T1} - V_{T2} \] (2-12)

In AMI 1.2 µm CMOS process, for \( L1 = 7.2 \, \mu m \) and \( L2 = 1.8 \, \mu m \), \( V_{T2} \) is about 0.15V smaller than \( V_{T1} \). This means that \( V_{SAT2} \) need to be around 0.15V to satisfy the condition (2-12). By carefully choosing the size of the channel width of M2 and adjusting the biasing current going through M1 and M2, condition (2-12) can be met. Therefore, M1 and M2 can be both operate in saturation region and thus provide an increased output impedance. The explanation for the threshold voltage changing with different channel length of the self-cascode current mirror can be found in reference [11].

Figure 2-10 shows the low frequency small signal equivalent output impedance. The rightmost figure is the simplified small signal equivalent circuit. For node X, we have
\[ V_X = I_t r_1 \text{ and the voltage across } r_2, \quad V_{r_2} = (I_t + g_{m2} V_X) r_2, \]

\[ V_t = V_{r_2} + V_X = (I_t + g_{m2} V_X) r_2 + I_t r_1 = I_t \left[(r_1 + r_2) + g_{m2} r_1 r_2\right] \tag{2-13} \]

Therefore the output impedance of the self-cascode NMOS is

\[ r_{out} = \frac{V_t}{I_t} = g_{m2} r_1 r_2 + (r_1 + r_2) \tag{2-14} \]

If \( r_1 = r_2 \), then

\[ r_{out} = g_{m2} r^2 + 2r = g_{m2} r^2 \tag{2-15} \]

Figure 2-10. The equivalent output impedance of the self-cascode NMOS

\[ 2.4 \text{ Output Stage – Distortion} \]

In ideal case, the common-source gate-driven MOSFET shown in Figure 2-11 does not contribute odd harmonic distortion if the MOSFET follows the square-law operation. For a pure sinusoid input signal with amplitude of \( V_{in} \) and fundamental frequency \( \omega_0 \), the second harmonic distortion is described by [12]

\[ HD_2 = \frac{1}{4} \frac{Z_L(2\omega_0)}{Z_L(\omega_0)} \frac{V_{in}}{V_{GS} - V_{TN}} \tag{2-16} \]
where

\[ Z_L(\omega) = \left( \frac{1}{R_L + j\omega C_L} \right)^{-1}. \] (2-17)

It is clear that lower \((V_{GS} - V_{TH})\) will benefit the output signal swing, but will also increase the second harmonic distortion, \(HD_2\). For 1 V operation, however, it is unavoidable. Fortunately, the \(HD_2\) described above only corresponds to the open loop case. When this structure is applied as the output stage of a two-stage Op Amp, the harmonic distortion of the output stage is reduced by a factor equal to the product of the compensation feedback loop gain and external feedback loop gain [12].

The output stage shown in Figure 2-11 is Class-A, where the output driver, in this case NMOS, is biased by a current source. For Class-A operation, the quiescent current of NMOS, \(I_{bias}\), must large than the largest amount of current needed for the load. For other operations, such as Class-B and Class-AB, both provide lower quiescent power dissipation lower than Class-A.

![Common-source circuit exhibiting second harmonic distortion.](image)

Figure 2-11. Common-source circuit exhibiting second harmonic distortion.
2.5 Complete Operational Amplifier Circuit

The 1 V bulk-driven Op Amp is shown in Figure 2-12. This schematic corresponds to the dual power supply with $V_{DD} = 0.5\text{V}$ and $V_{SS} = -0.5\text{V}$. It is convenient to set the common mode voltage at ground (0V) for this configuration. The Op Amp is a two-stage structure with a folded-cascode input stage. The input stage consists of a bulk-driven PMOS differential pair, M1-M2, loaded by a wide-swing cascode NMOS current mirror, which consists of transistors M6-M10. One reason for using wide-swing cascode mirror is its relatively small input impedance at node D and since only one $V_{DSAT}$ will drop at M8 and M9, the differential pair can have larger common-mode input swing without running into triode region. Therefore, it is ideally suitable in the 1 V power supply application. PMOS transistor M4, M5, M12, and M13 consist of the self-cascode gain stage which has described in the previous chapter. The only difference is to use the PMOS device instead of NMOS device in here. With the careful sizing each aspect ratio of the PMOS device, the self-cascode gain stage can effectively operate in such a low power supply and provide enough high gain. Whereas the normal cascode gain stage can not even operate at this low voltage. As described earlier, the length of PMOS transistor M4 and M5 should be greater than that of M12 and M13, whereas the width of M12 and M13 should be much larger than that of M4 and M5, respectively, in terms of effectively reduce the threshold voltage. M3 acts as the tail current source for the bulk-driven input differential pair M1 and M2. The Class-A output stage uses NMOS driver M10 loaded by the current source M11 to obtain high output swing as described previously.

The current source $I_{bias2}$ provide the bias current for the differential input pair and the output stage of the Op Amp, which is replicated and scaled accordingly through the diode
connected PMOS M16 to M3 and M10. Biasing the self-cascode transistors need to be totally separated from biasing the simple transistor. Otherwise, a great deal of the mismatches will occur. Therefore current source $I_{bias1}$ provide the bias current for the self-cascode gain stage, which is replicated and scaled accordingly through the diode connected self-cascode PMOS M14 plus M15 to M4 and M5. $R_z$ and $C_C$ are the compensation elements. As the Miller pole-splitting capacitor $C_C$ generates a right-half-plane zero, nulling resistor $R_z$ cancels this zero and shifts it to the left-half-plane to improve phase margin, as discussed in the following section. The gain-bandwidth product and DC open-loop gain are given by

$$GBW = \frac{g_{mb1}}{2\pi C_C}$$

and

$$\text{and}$$
2.6 1-V Op Amp Frequency Compensation

The small signal equivalent circuit for the 1 V bulk-driven Op Amp is given in Figure 2-13. The resulting analysis for the circuit are identical to those described in [13] for the nulling resistor compensation technique, which shape the Op Amp’s open-loop frequency response with three poles and one zero. Figure 2-13 (a) shows the simplified output stage of Figure 2-12, where $R_S$ is denoted as the output resistance of the first gain stage, $C_E$ is the equivalent capacitance at node $E$, and $R'_L = r_{ds10} / r_{ds11} \parallel R_L$. For moderate values of $R_Z$, the third pole is located at high frequencies and the first two poles are close to the values calculated with $R_Z = 0$ as shown in Figure 2-13(b). Moreover, in two-stage Op Amps with Miller compensation, a right-half-plane zero appears at $\omega_z = g_{m10} / (C_C + C_{GD10})$ [13]. With the $R_Z$ introduced in the circuit and in series with $C_C$, the zero frequency is given by

$$\omega_z = \frac{1}{C_C \left( \frac{1}{g_{m10}} - R_Z \right)}$$  \hspace{1cm} (2-20) [13]

then $R_Z$ can be decided as

$$R_Z = \frac{C_L + C_E + C_C}{g_{m10} C_C}$$  \hspace{1cm} (2-21)

as shown in Figure 2-13 (C).

These poles $\omega_{p1}$, $\omega_{p2}$, and $\omega_{p3}$, are described by

$$\omega_{p1} = \frac{1}{R_S \left[ (1 + g_{m10} R'_L) (C_C + C_{GD10}) + C_E \right] + R'_L (C_C + C_{GD10} + C_L)}$$  \hspace{1cm} (2-22)
\[ \omega_{p2} = \frac{R_s \left[ (1 + g_{m10} R'_L) (C_C + C_{GD10}) + C_E \right] + R'_L \left( C_C + C_{GD10} + C_L \right)}{R_s R'_L \left( (C_C + C_{GD10})(C_E + C_L) + C_E C_L \right)} \] (2-23)

\[ \omega_{p3} = \frac{1}{R_z C_C} \] (2-24)

where, \[ R_s \approx \left[ g_{m7} r_{ds7} (r_{ds2} || r_{ds9}) \right] \left[ (g_{m13} (r_{ds13} r_{ds5})) \right] \] (2-25)

and \[ C_E = (C_{gd} + C_{ld})_{M13} + (C_{gd} + C_{bd})_{M7} + (C_{gd} + C_{eg})_{M10} \] (2-26)

The approximations used to describe the frequency response depend on widely spaced poles which typical to CMOS Op Amps. Although the transconductance, \( g_{mb1} \), of differential pair does not affect the poles and zero locations [9], it is however directly proportional to the Op Amp’s unity-gain frequency. If properly compensated, the Op Amp’s second pole is placed beyond the Op Amp’s unity-gain frequency. The spacing between the second pole and the unity-gain frequency determines the Op Amp’s open-loop phase margin and consequently, affects the transient response of the Op Amp.

Figure 2-13. Small-signal equivalent circuit for 1 V bulk-driven Op Amp
2.7 Simulated Performance

Simulations of the 1 V bulk-driven Op Amp were performed to verify the design. $V_{DD}$ and $V_{SS}$ of +0.5V and -0.5V, respectively, were chosen so that the common-mode voltage can be conveniently set at 0V. The BSIM3 models for HSPICE level-49 were performed throughout the entire simulations. The AMI 1.2µm standard n-well CMOS digital technology was selected for the simulation. The simulated DC open-loop transfer characteristic of the 1 V bulk-driven Op Amp is shown in Figure 2-14.

This result indicates the rail-to-rail swing capability of the output stage. The input offset voltage of 38µV is also indicated in this figure. A larger offset may result due to transistor mismatch in actual implementation. Illustrated by the two ends of the linear region in the curve, where the DC gain still remains 1,000, the output swing is -418mV ~ 340mV, where a minimum open loop DC gain of 1,000 is still achieved. The input common-mode range (ICMR) is shown in Figure 2-15. The simulation indicates the ICMR has a range of -481mV ~ 441mV.

Figure 2-16 illustrates open-loop frequency response. Both the open-loop gain plot and the phase plot are shown for common-mode voltage of 0V. The plot indicates that the open-loop gain of the 1 V bulk-driven Op Amp is 69 dB with the unit-gain frequency of 2.75 MHz and the phase margin of 81°.

The common-mode rejection ratio (CMRR) is shown in Figure 2-17. As shown in Figure 2-17, the CMRR of the Op Amp has the value of 90.2 dB. This indicates that the bulk-driven scheme should provide a reasonable CMRR performance when compared the gate-driven case.
Figure 2-14. The open loop transfer characteristic of 1 V bulk-driven Op Amp

Figure 2-15. Input Common-Mode Range of the 1 V bulk-driven Op Amp
The noise and distortion simulations were performed using the HSPICE® simulation tools. Figure 2-18 shows the DFT analysis of the 1 V bulk-driven Op Amp with 200mV_p-p 10KHz sinusoidal input signal. The Op Amp was configured in non-inverting configuration with a gain of one. As indicated in Figure 2-18, the THD of approximately –62.7 dB is achieved at frequency of 10KHz. Table 2-1 summarizes the aspect ratio of each transistor of the 1 V bulk-driven Op Amp. The simulated specifications are listed in Table 2-2.
Figure 2-17. Common-mode rejection ratio frequency response

Figure 2-18. Simulation of the DFT analysis for the 1 V bulk-driven Op Amp
Table 2-1. The parameters of the transistors (\(\mu\)m)

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Length/Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2</td>
<td>1548/1.8</td>
</tr>
<tr>
<td>M3</td>
<td>288/1.8</td>
</tr>
<tr>
<td>M4, M5</td>
<td>138/7.2</td>
</tr>
<tr>
<td>M6, M7</td>
<td>840/2.4</td>
</tr>
<tr>
<td>M8, M9</td>
<td>319.2/1.8</td>
</tr>
<tr>
<td>M10</td>
<td>2716.8/2.4</td>
</tr>
<tr>
<td>M11</td>
<td>960/2.4</td>
</tr>
<tr>
<td>M12, M13</td>
<td>960/1.8</td>
</tr>
<tr>
<td>M14</td>
<td>168/7.2</td>
</tr>
<tr>
<td>M15</td>
<td>960/1.8</td>
</tr>
<tr>
<td>M16</td>
<td>1.8/3.6</td>
</tr>
<tr>
<td>Rz</td>
<td>8.5K</td>
</tr>
<tr>
<td>Cc</td>
<td>5.5pF</td>
</tr>
<tr>
<td>Ib1, Ib2</td>
<td>10(\mu)A</td>
</tr>
</tbody>
</table>

Table 2-2. 1 V Bulk-driven Op Amp simulation results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Simulated Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC open-loop gain</td>
<td>69dB</td>
</tr>
<tr>
<td>Unity-gain frequency</td>
<td>2.75MHz</td>
</tr>
<tr>
<td>Phase margin</td>
<td>81°</td>
</tr>
<tr>
<td>ICMR</td>
<td>-481mV~441mV</td>
</tr>
<tr>
<td>Output swing</td>
<td>-418mV~340mV</td>
</tr>
<tr>
<td>(at DC gain=1,000)</td>
<td></td>
</tr>
<tr>
<td>Input offset</td>
<td>38(\mu)V</td>
</tr>
<tr>
<td>CMRR</td>
<td>90.2dB at 100Hz</td>
</tr>
<tr>
<td>PSRR+((V_{DD}))</td>
<td>71.3dB at 100Hz</td>
</tr>
<tr>
<td>PSRR-((V_{DD}))</td>
<td>70.5dB at 100Hz</td>
</tr>
<tr>
<td>Equivalent input noise</td>
<td>55.45(nV / \sqrt{Hz})</td>
</tr>
<tr>
<td>Total harmonic distortion (THD)</td>
<td>-75.6dB</td>
</tr>
<tr>
<td>(100mV_{p-p}, 10KHz sinewave)</td>
<td></td>
</tr>
<tr>
<td>Power dissipation</td>
<td>300(\mu)W</td>
</tr>
</tbody>
</table>

(Note: \(V_{DD}=+0.5\)V, \(V_{SS}=-0.5\)V, \(R_L=5K\Omega\), and \(C_L=10pF\))
The simulation results indicated that the design of 1V bulk-driven Op Amp has achieved the input common-mode range and rail-to-rail output swing with satisfactory results.

In the next chapter, using 1V bulk-driven Op Amp as a building block to design and implement a programmable gain instrumentation amplifier will be discussed in detail.
CHAPTER 3

DESIGN OF 1V BULK-DRIVEN PROGRAMMABLE GAIN INSTRUMENTATION AMPLIFIER

Instrumentation amplifiers (INA) are used in applications at which a small differential signal must be precisely amplified from a large common-mode signal and provide a single ended output. Hence, the instrumentation amplifier needs to have high input impedance, high common-mode rejection ratio, and low offset voltage drift. Furthermore, some other important specifications such as gain, bandwidth, and power dissipation, etc. are also the features that people look for when an instrumentation amplifier is used. First, a popular structure of an instrumentation amplifier is analyzed in this chapter.

3.1 Analysis of a Popular Structure of an Instrumentation Amplifier (INA)

As shown in Figure 3-1, the circuit consists of two stages: The first stage is formed by Op Amp A1 and A2 and their associated resistors, and the second stage is formed by Op Amp A3 together with its four associated resistors.

Analysis of the circuit, assuming all Op Amps are ideal, as illustrated in Figure 3-1. The key point is that the virtual short circuits at the inputs of the Op Amp A1 and A2 cause the input voltages \( v_1 \) and \( v_2 \) to appear at the two terminals of the resistor R1. Thus the differential input voltage \( (v_1-v_2) \) appears across R1 and causes a current \( i = \frac{(v_1 - v_2)}{R1} \) to flow through R1 and the two resistors labeled R2. This current in turn produces a voltage difference between the output terminals of A1 and A2 given by
\[ v_{o1} - v_{o2} = \left(1 + \frac{2R2}{R1}\right)(v_1 - v_2). \]  

(3-1)

The difference amplifier, formed by A3 and resistors labeled R3 and R4, senses the voltage difference \((v_{o1} - v_{o2})\) and provides a proportional output voltage \(v_o\), where,

\[ v_o = -\frac{R4}{R3}(v_{o1} - v_{o2}). \]  

(3-2)

Combine equation (3-1) and (3-2) results in

\[ v_o = \frac{R4}{R3}\left(1 + \frac{2R2}{R1}\right)(v_2 - v_1). \]  

(3-3)

Thus the instrumentation amplifier has a differential voltage gain

\[ A_d \equiv \frac{v_o}{v_2 - v_1} = \left(1 + \frac{2R2}{R1}\right)\frac{R4}{R3}. \]  

(3-4)
This indicates that, ideally, if an input common-mode signal $V_{CM}$ is applied to both input terminals of the INA, $v_{CM}$ will be conveyed through the first stage resulting in $v_{o1} = v_{o2} = v_{CM}$. Therefore, if the second-stage difference amplifier A3 is properly balanced, a zero output voltage in response to $v_{CM}$ can be expected, which indicating that the INA has the nature of rejecting the common-mode gain.

### 3.2 Block Diagram of the 1 V Bulk-Driven Programmable-Gain Instrumentation Amplifier

As shown in Figure 3-2, the proposed 1 V Bulk-Driven Programmable-Gain Instrumentation Amplifier (BDPGINA) has the similar structure with the FGINA. The only additional function blocks are the programmable resistor network (PRN), low voltage switching (LVS) and bias circuits. The Amp1 and Amp2 in the first stage of the BDPGINA are identical to the 1 V bulk-driven Op Amp as discussed in the Chapter 2. The third amplifier (the difference amplifier) in the second stage of the BDPGINA, Amp3, is a new structure with trans-impedance function. It also has a new designed output stage, which will be discussed in detail in the next. In order to let the programmable gain function efficiently and realize conveniently, the value of resistors R3 and R4 at Amp3 are chosen to be equal to 25 KΩ. Therefore the gain of BDPGINA is depend on the programmable resistor network at the first stage. Details will be discussed in the later section.
3.3 The New Output Stage of the Third Amplifier

In the previous chapter, the 1 V bulk-driven Op Amp has been introduced and analyzed. Since one of the goals of the instrumentation amplifier is capable of driving 1 KΩ resistor in parallel with 20 pF capacitor load, this will need the third Op Amp in INA to have high current driving capability, large output swing, and low output impedance. However, the output stage of the Op Amp described in previous chapter lacks of the ability to provide either the lower output impedance or a higher current driving capability. Therefore, a new output stage [15], which can match the requirements mentioned above, is employed. The output stage of the third Op Amp is shown in Figure 3-3. The output stage is made of transistors M1 – M7. The gate of M1 and M4 are connected to the input node of this output stage directly. M2, M3 and M5, M6 consist of two current mirrors, respectively. M7 serves as a current source, which has the same bias point as that in 1 V bulk-driven Op Amp. The circuit behavior is described as follows.
Figure 3-3. The output stage of the third amplifier in BDPGINA

With the voltage of the input signal going from 0 towards $V_{DD}$, transistor M1 and M4 will turn on from triode to saturation. The drain current of M1, $I_{D1}$, will also increase until equals to the bias current $I_{b1}$, which is generated by M7. At the same time, the current flows into the diode connected M2 will decrease to zero. This will cause the NMOS current mirror M2 and M3 turn off, and the node D will be pushed to $V_{DD}$. Thus the PMOS current mirror M5 and M6 will be turned off and the output current is provided by M4 only. Similarly, when the voltage of the input signal going from 0 towards $V_{SS}$, transistor M1 and M4 will turn off and the current flows into the diode connected M2 equals to $I_{b1}$. Hence the NMOS current mirror of M2 and M3 will turn on to pull the node D towards $V_{SS}$. This makes the PMOS current mirror of M5 and M6 turned on, causing the output current solely provided by M5. For low input levels, the output transistor M4 and M5 are both in saturation region and the circuit performs a Class-AB operation.

Since M7 and M6 are current source providing bias current $I_{b1}$ and $I_{b2}$, respectively, M2 and M3 consist of a NMOS current mirror, current $I_{D1}$ is given by
\[ I_{D1} = I_{b1} - \left( \frac{W}{L} \right)_2 I_{b2}. \]  \hspace{1cm} (3-5)

In stand-by condition, current \( I_{D4} \) is equal to \( I_{D5} \), and both are given by
\[ I_{D4} = \left( \frac{W}{L} \right)_4 I_{b1}. \]  \hspace{1cm} (3-6)

By using (3-1) and (3-2), with carefully sizing the aspect ratios of each transistor, the bias currents in the output stage can be set accurately [15].

Assume a sinusoidal input signal with amplitude \( V_p \) is applied at \( V_{in} \) node in Figure 3-3, and assume the output stage performs an ideal Class-B operation. The circuit will have different transconductance gains, \( a \) and \( b \), for the two half waves, which is given by
\[ a = g_{m4} \]  \hspace{1cm} (3-7a)
\[ b = Gg_{m5} \]  \hspace{1cm} (3-7b)
where \( G \) is the small-signal gain of the mirror amplifier \( M1 - M3 \) and is given by
\[ G = g_{m1} \left( \frac{W}{L} \right)_3 (r_{ds3} \parallel r_{ds6}) \]  \hspace{1cm} (3-7c)[15]

Therefore, current \( i_{D4} \) and \( i_{D5} \) can be expressed as
\[ i_{D4} = \begin{cases} \alpha v_{in}, & \text{for } 0 < t < T/2 \\ 0, & \text{for } T/2 < t < T \end{cases} \]  \hspace{1cm} (3-7d)
\[ i_{D5} = \begin{cases} 0, & \text{for } 0 < t < T/2 \\ -b v_{in}, & \text{for } T/2 < t < T \end{cases} \]  \hspace{1cm} (3-7e)

By expanding \( i_{D4} \) and \( i_{D5} \) in Fourier series and considering the first two terms only, we have
Thus an output stage with high current driving capability can be achieved.

\[ i_{\text{out}} = -(i_{D4} + i_{D5}) \]
\[ \approx \frac{1}{2} (a + b) V_p \sin(\omega t) + \frac{2}{3\pi} (b - a) V_p \cos(2\omega t). \quad (3-8) \]

### 3.4 Complete Circuit of the Third Op Amp

Figure 3-4 shows the complete schematic of the third Op Amp. The cascode gain stage is identical to that in the first and second Op Amp. For the input stage, the input differential pair is replaced by two current input nodes, \( i^+ \) and \( i^- \) connected to the source of M6 and M7, respectively. Therefore M6 and M7 act as common-gate amplifier. This structure is desirable for current mode input rather than voltage mode input for its relatively small input impedance at the source of M6 and M7. Typically, the input impedance at the source of M7 is on the same order of magnitude of \( 1/g_{m7} \) at low frequency, normally in the order of \( 10^3 \) ohm or less. The impedance at output node M7 is in the order of \( 10^6 \) ohm or more, because of the nature of the cascode mirror structure. In this case, the output impedance of node E at low frequency, \( r_E \), will have

\[ r_E = (g_{m13} r_{ds13} r_{ds4}) \parallel (g_{m7} r_{ds7} r_{ds9}). \]

Therefore, a small input current change will result in a big voltage change at node E due to the large output impedance at node E. For simplicity, \( V_E = \Delta i \cdot r_E = (i^+ - i^-) \times [(g_{m13} r_{ds13} r_{ds4}) \parallel (g_{m7} r_{ds7} r_{ds9})], \) where \( V_E \) is the voltage at node E. Thus a trans-impedance amplifier is formed. The parameters of the third amplifier are summarized in Table 3-1.
Figure 3-4. The schematic of the third Amplifier

Table 3-1. Parameters of the transistors in third Op Amp (µm)

<table>
<thead>
<tr>
<th>Device</th>
<th>Dimensions</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2</td>
<td>1548/1.8</td>
</tr>
<tr>
<td>M3</td>
<td>288/1.8</td>
</tr>
<tr>
<td>M4, M5</td>
<td>138/7.2</td>
</tr>
<tr>
<td>M6, M7</td>
<td>840/2.4</td>
</tr>
<tr>
<td>M8, M9</td>
<td>319.2/1.8</td>
</tr>
<tr>
<td>M10</td>
<td>2610/1.8</td>
</tr>
<tr>
<td>M11</td>
<td>18663/1.8</td>
</tr>
<tr>
<td>M12, M13</td>
<td>960/1.8</td>
</tr>
<tr>
<td>M14</td>
<td>168/7.2</td>
</tr>
<tr>
<td>M15</td>
<td>960/1.8</td>
</tr>
<tr>
<td>M16</td>
<td>1.8/3.6</td>
</tr>
<tr>
<td>M17</td>
<td>330/1.8</td>
</tr>
<tr>
<td>M18, M19</td>
<td>540/1.8</td>
</tr>
<tr>
<td>M20</td>
<td>900/1.8</td>
</tr>
<tr>
<td>M21</td>
<td>600/1.8</td>
</tr>
<tr>
<td>Rz</td>
<td>5K</td>
</tr>
<tr>
<td>Cc</td>
<td>5pF</td>
</tr>
<tr>
<td>Ib1, Ib2</td>
<td>10µA</td>
</tr>
</tbody>
</table>
3.5 Programmable Resistor Network (PRN)

As discussed in the previous section and from the equation (3-4), as well as referring to the conventional INA in Figure 3-1, the resistors R3 and R4 are set to be equal so that the gain of the BDPGINA is determined by R1 and R2 only. Therefore equation (3-4) can be written as

$$A_{d, BDPGINA} = \left(1 + \frac{2R2}{R1}\right).$$  \hspace{1cm} (3-9)

Since R1 represents the input resistor of the first stage of BDPGINA and R2 represents the feedback resistor of each Amps in the first stage of BDPGINA, therefore, if a different combination of $R_2/R_1$ is chosen, then a different set of close-loop gain of the BDPGINA can be achieved. In other words, by programming the resistance of R1 and R2, the instrumentation amplifier with programmable gain can be realized [17].

One topology of realizing the PRN is shown in Figure 3-5. Each switch position corresponds to one particular fixed gain. The switches are controlled externally so that a digitally programmable INA with a variety of combinations of gains can be realized. With this type of the configuration, the gain can be any value of combinations, which can also be expressed as

$$Gain = \left(1 + \frac{2R_{II}}{R_I}\right)$$  \hspace{1cm} (3-10)

where, $R_I$ represents the effective input resistance under one particular switch position, and $R_{II}$ represents the effective feedback resistance under such particular switch position. In this design, a total of five gains have been chosen for demonstration, which are 1, 5, 10, 20, and
30. To determine each resistor's value under a specific set of gain step is straightforward:

From (3-10),

with gain = 1; \[ \Rightarrow \quad 1 + \frac{2R_H}{R_I} = 1 \]

\[ \Rightarrow \quad \begin{cases} R_H = 0 \\ R_I = 2R_4 + 2R_3 + 2R_2 + 2R_1 + R_0 \end{cases} \]

... ⑦
with gain = 5; \[ 1 + \frac{2R_{II}}{R_i} = 5 \Rightarrow R_{II} = 2R_i \]

\[ \{ R_{II} = R_i \\
R_i = 2R_4 + 2R_3 + 2R_2 + R_0 \} \]

\[ R_4 = 4(R_4 + R_3 + R_2 + \frac{R_0}{2}) \quad \ldots \oplus \]

with gain = 10; \[ 1 + \frac{2R_{II}}{R_i} = 10 \Rightarrow R_{II} = \frac{9}{2}R_i \]

\[ \{ R_{II} = R_2 + R_1 \\
R_i = 2R_4 + 2R_3 + R_0 \} \]

\[ R_2 + R_1 = 9(R_4 + R_3 + \frac{R_0}{2}) \quad \ldots \ominus \]

with gain = 20; \[ 1 + \frac{2R_{II}}{R_i} = 20 \Rightarrow R_{II} = \frac{19}{2}R_i \]

\[ \{ R_{II} = R_3 + R_2 + R_1 \\
R_i = 2R_4 + R_0 \} \]

\[ R_3 + R_2 + R_1 = 19(R_4 + \frac{R_0}{2}) \quad \ldots \ominus \]

with gain = 30; \[ 1 + \frac{2R_{II}}{R_i} = 30 \Rightarrow R_{II} = \frac{29}{2}R_i \]

\[ \{ R_{II} = R_4 + R_3 + R_2 + R_1 \\
R_i = R_0 \} \]

\[ R_4 + R_3 + R_2 + R_1 = \frac{29}{2}R_0 \quad \ldots \ominus \]

Combine \( \oplus, \ominus, \ominus, \text{and} \ominus \). We have,
If we choose \( R_0 = 1 \, \text{K}\Omega \), then all resistor values can be decided, that is,

\[
\begin{align*}
R_4 &= \frac{1}{4} R_0 \\
R_3 &= \frac{3}{4} R_0 \\
R_2 &= \frac{3}{2} R_0 \\
R_1 &= 12R_0
\end{align*}
\]

(3-11)

If we choose \( R_0 = 1 \, \text{K}\Omega \), then all resistor values can be decided, that is,

\[
\begin{align*}
R_4 &= 250\Omega \\
R_3 &= 750\Omega \\
R_2 &= 1.5\, \text{K}\Omega \\
R_1 &= 12\, \text{K}\Omega \\
R_0 &= 1\, \text{K}\Omega
\end{align*}
\]

(3-12)

3.6 Low Voltage Switching Scheme (LVS)

One of the challenges of realizing the programmable gain is the low voltage switch. Since the supply voltage of 1 volt is used, the traditional transmission gate switch or simple N(P)MOS switch cannot operate properly. Even if these types of switch can be barely turned on, their large “on” resistance may affect the frequency response as well as gain error. In this design, a new type of switching scheme that suitable in low voltage condition is proposed.

The theory of operation of the LVS is base on that of the bulk-driven differential pair, which has discussed in Chapter 2. For Amp1 and Amp2 in the first stage of the BDPGINA, their input bulk-driven differential pairs are replaced with the structure shown in Figure 3-6. Comparing the structure as shown in Figure 3-6 to the bulk-driven differential pair shown in Figure 2-5, M1 and M3 remain no change, the input terminal Vin+ connects to the bulk
terminal of M1 and gate of M1 connects to $V_{SS}$ to ensure M1 turns on all the time. M2 in Figure 2-5 replaces its name as M2-1, with four identical PMOS device connected in parallel, namely, M2-2 to M2-5. D1 through D5 are digital control terminals that connected to the gate of M2-1 through M2-5, respectively, in which the gain steps of 5, 10, 20, 30, and 1 are controlled correspondingly. Terminal Vin-1 through Vin-5 link the bulk terminal of M2-1 through M2-5, respectively, to the corresponding positions of the PRN, in which the effective combinations of $R_{II}$ and $R_1$ can be made and thus the corresponding gain step is formed.

![Figure 3-6. A proposed Low Voltage Switching Scheme](image-url)
For instance, if the gain = 5 is needed, then D1 is set to -0.5V to turn M2-1 on while D2 through D5 are set to +0.5V to remain M2-2 through M2-5 off. Therefore, M1 and M2-1 form a bulk-driven differential input pair, with the two input terminals Vin+ and Vin-, this makes the Op Amp operate properly. With terminal Vin- links the bulk of M2-1 to the corresponding position (R4) in PRN, the Rn Jd R1 can be determined, and hence the gain = 5 is chosen. This example shows that the gain steps can be easily set by digitally controlling the combinations of the resistance network. In other word, it is achieved by switching different bulk-driven transistor to make a differential input pair.

The disadvantage of this scheme is that when a different gain setting is used, the offset voltage due to transistor mismatch will become different.

### 3.7 The Complete Schematic of the BDPGINA

Table 3-2 illustrates the gain steps and the corresponding digital settings. The complete schematic of the BDPGINA is shown in Figure 3-7. The details of the bias circuit with the actual size of each transistor are shown in Figure 3-8.

<table>
<thead>
<tr>
<th></th>
<th>Gain=1</th>
<th>Gain=5</th>
<th>Gain=10</th>
<th>Gain=20</th>
<th>Gain=30</th>
</tr>
</thead>
<tbody>
<tr>
<td>D1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>D2</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>D3</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>D4</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>D5</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

(Note: "1" = applying +0.5V, and "0" = applying -0.5V)
Figure 3-7, Complete schematic of the 1 V Bulk-driven Programmable Gain Instrumentation Amplifier

Figure 3-8. The tails of the bias circuit
3.8 Simulation Results of the BDPGINA

The conditions for simulating the BDPGINA are identical to that of simulating 1 V bulk-driven Op Amp. $V_{DD}$ and $V_{SS}$ of +0.5V and -0.5V, respectively, were chosen and the BSIM3 models were used for all the simulations. A $5mV_{p-p}$, 1KHz sinusoidal signal is used as the input source and a $1K\Omega$ resistor in parallel with a 20pF capacitor is loaded at the output of the BDPGINA. Figure 3-9 illustrates ICMR of the five different gain steps. Table 3-3 summarizes the simulation results for ICMR at five gain steps.

![Figure 3-9. ICMR of the five gain steps](image-url)
Table 3-3. Summary of ICMR for BDPGINA at 5 different gain steps

<table>
<thead>
<tr>
<th>Gain</th>
<th>$V_{CM}$ range</th>
<th>$V_{out}$ range</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-491mV ~ 467mV</td>
<td>-245mV ~ 233.3mV</td>
</tr>
<tr>
<td>5</td>
<td>-278mV ~ 268mV</td>
<td>-347mV ~ 328.4mV</td>
</tr>
<tr>
<td>10</td>
<td>-307mV ~ 291mV</td>
<td>-334.1mV ~ 317.2mV</td>
</tr>
<tr>
<td>20</td>
<td>-314mV ~ 302mV</td>
<td>-330mV ~ 311.8mV</td>
</tr>
<tr>
<td>30</td>
<td>-319mV ~ 304mV</td>
<td>-331.2mV ~ 308.2mV</td>
</tr>
</tbody>
</table>

Figure 3-10 shows the DC sweep of the BDPGINA at five different gain steps. The results also indicated a rail-to-rail characteristic of the modified output stage. The output swings for five different gain steps are almost identical, which is -483mV ~ 476.6mV. This result verified that the modified output stage of the Amp3 in the BDPGINA has a better driving capability and rail-to-rail performance than that of the Amp1 and Amp2. The slope of each curve in Figure 3-10 indicating the respective gain step. Table 3-4 summarizes the corresponding input ranges for the five different gain steps.

![Figure 3-10. DC responses for five gain steps.](image-url)
Table 3-4. Summary of the input range for 5 different gain steps

<table>
<thead>
<tr>
<th>Gain steps</th>
<th>Input Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain=1</td>
<td>-487mV ~ 482.7mV</td>
</tr>
<tr>
<td>Gain=5</td>
<td>-96.6mV ~ 98.8mV</td>
</tr>
<tr>
<td>Gain=10</td>
<td>-48.5mV ~ 49.8mV</td>
</tr>
<tr>
<td>Gain=20</td>
<td>-24.2mV ~ 20.2mV</td>
</tr>
<tr>
<td>Gain=30</td>
<td>-16.2mV ~ 18.2mV</td>
</tr>
</tbody>
</table>

Figure 3-11 shows the CMRR at five different gain steps. The plots indicate that the CMRR for gain of 1, 5, 10, 20, and 30 has the value of 54dB, 68dB, 74dB, 80dB, and 83.5dB, respectively. The common-mode gain at each gain step has no significant difference, therefore higher gain step results in a higher CMRR.

The results of the AC responses from Figure 3-12 are summarized in Table 3-5. The low gain errors for all 5 gain steps reveals that the proposed structure is suitable for precision low voltage applications. The transient waveforms for the five gain steps are presented in Figure 3-13(a), (b). The noise and distortion simulations are summarized in Table 3-6.

The layout floor plan of the BDPGINA is shown in Figure 3-14. Device matching issue is also considered in the layout floor plan. Particularly, Amp1 and Amp2 are symmetrically placed as they are identical. Dummy resistors are generally placed outside programmable resistor network (PRN) to improve the resistor matching. The actual layout of the BDPGINA with the pad frame is present in Figure 3-15.
Table 3-5. Summary of AC response for 5 gain steps

<table>
<thead>
<tr>
<th>Gain</th>
<th>1</th>
<th>5</th>
<th>10</th>
<th>20</th>
<th>30</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ideal Output Voltage (mV)</td>
<td>5.00</td>
<td>25.00</td>
<td>50.00</td>
<td>100.00</td>
<td>150.00</td>
</tr>
<tr>
<td>Output Voltage (mV)</td>
<td>4.99</td>
<td>24.98</td>
<td>50.02</td>
<td>100.30</td>
<td>150.70</td>
</tr>
<tr>
<td>Actual Gain</td>
<td>0.998</td>
<td>4.996</td>
<td>10.004</td>
<td>20.06</td>
<td>30.14</td>
</tr>
<tr>
<td>Gain Error(%)</td>
<td>0.2</td>
<td>0.08</td>
<td>0.04</td>
<td>0.3</td>
<td>0.47</td>
</tr>
<tr>
<td>Gain Bandwidth(MHz)</td>
<td>1.58</td>
<td>0.76</td>
<td>0.79</td>
<td>0.81</td>
<td>0.81</td>
</tr>
</tbody>
</table>

(Note: Vin = 5mV, 1KHz Sinusoidal signal)

Table 3-6. Summary of noise and distortion simulations for 5 gain steps

<table>
<thead>
<tr>
<th>Gain</th>
<th>Equivalent Input Noise</th>
<th>Total Harmonic Distortion (THD)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(nV/√Hz)</td>
<td></td>
</tr>
<tr>
<td>Gain = 1</td>
<td>149</td>
<td>-59.1dB</td>
</tr>
<tr>
<td>Gain = 5</td>
<td>103.3</td>
<td>-52.7dB</td>
</tr>
<tr>
<td>Gain = 10</td>
<td>101.4</td>
<td>-52.7dB</td>
</tr>
<tr>
<td>Gain = 20</td>
<td>100.9</td>
<td>-52.4dB</td>
</tr>
<tr>
<td>Gain = 30</td>
<td>100.7</td>
<td>-51.6dB</td>
</tr>
</tbody>
</table>

Figure 3-11. CMRR at five different gain steps
Figure 3-12. AC responses of the five gain steps

Figure 3-13. Transient responses of BDGPINA with a 5mV pp, 1KHz sinusoidal signal input
(b) Gain of 10, 20, and 30

Figure 3-13. (Continued)

Figure 3-14. Layout floor plan of the 1 V BDPGINA
The total die area for BDPGINA is 1,604.4\textmu m\times1,068\textmu m. The simulated total power dissipation is 605.5\textmu W. The output amplifier of the BDPGINA, Op Amp3, was working properly with a -3dB bandwidth of about 1.5 MHz. The output swing is quite close to the simulation results with similar load. However, the bulk-driven Op Amp1 and Op Amp2 of the BDPGINA, did not work properly even though the post-layout simulation is performed properly. Therefore all the other measurement data are not available to present. The failure of the chip is presumably due to the limitation of the transistor models in the simulation tools when simulating the bulk-driven case.
CHAPTER 4

CONCLUSIONS

4.1 Summary

Bulk-driven technique for satisfying the need of the applications for power supply of 1 volt with standard CMOS technology has been discussed in this thesis. A bulk-driven differential pair based on this concept has been presented that provides a satisfactory input common-mode range performance.

A 1 V bulk-driven operational amplifier has been designed. The self-cascode current mirror technique can effectively increase the output impedance of the gain stage while maintaining all the transistors in saturation region for a supply voltage of 1 V. It provides enough DC gain for the Op Amp. A common-source amplifier configuration is selected with Class-A operation for the output stage to provide rail-to-rail output signal swing. Simulations have verified that the Op Amp achieves a DC open-loop gain of 71.4 dB, an unity-gain frequency of 2.75MHz, and a phase margin of 81°. The ICMR has a range of -481mV~441mV, and the output swing reaches -406mV~385mV.

A 1 V bulk-driven programmable gain instrumentation amplifier has been proposed and the performance has been verified through simulations. A novel low voltage switching scheme based on the bulk-driven technique is also proposed and simulated to be effective under the 1 V power supply switching condition. Thus, a digital programmable gain instrumentation amplifier can be realized. Gain steps of 1, 5, 10, 20, and 30 are chosen for this design as an example. Gain errors of 0.2%, 0.08%, 0.04%, 0.3%, and 0.47%, were
obtained for gain settings of 1, 5, 10, 20 and 30, respectively, which shows the precision of this type of the instrumentation amplifier under 1 V power supply condition. A modified output stage with Class-AB operation has been used for the last stage of the instrumentation amplifier, which is capable of driving the load of 1KΩ resistor in parallel with 20pF capacitor. A output swing of -483mV ~ 476.6mV is achieved. The entire 1 V bulk-driven programmable gain instrumentation amplifier consumes only 605.5µW.

4.2 Future Work

To make the designed chip fully working is the major job to do in the future. A different transistor model for simulation needs to be developed. The mechanism of the bulk-driven device needs to be further investigated.

There are still plenty of the rooms for improving the performance of the current design. Even though the DC open-loop gain, the gain bandwidth, ICMR, CMRR and power dissipation, etc, are competitive with many other type of the low voltage CMOS amplifiers, the performance of phase margin, slew rate, settling time, noise, and distortion, etc, are less attractive. Future work should be mainly targeted on these improvements.

A 1 V switched Op Amp can be developed based on the current design in the future. The Op Amp will be switched on or off with the external clock signal. With the Op Amp turned on, the signal will be passed through and amplified by the Op Amp. With the Op Amp turned off, the output of the Op Amp goes to the VDD. It can be used as a front-end interface for switched-Op amp circuits with other circuits.
REFERENCES


