

2019

## An investigation of an ionic liquid analog to the conventional metal-oxide-semiconductor field-effect transistor

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**An investigation of an ionic liquid analog to the conventional metal-oxide-  
semiconductor field-effect transistor**

by

**Richard Effler**

A thesis submitted to the graduate faculty  
in partial fulfillment of the requirements for the degree of  
**MASTER OF SCIENCE**

Major: Mechanical Engineering

Program of Study Committee:  
Reza Montazami, Major Professor  
Sonal Padalkar  
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Xiang Chunhui

The student author, whose presentation of the scholarship herein was approved by the program of study committee, is solely responsible for the content of this thesis. The Graduate College will ensure this thesis is globally accessible and will not permit alterations after a degree is conferred.

Iowa State University

Ames, Iowa

2019

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**NOMENCLATURE**

ITO	Indium-Tin Oxide
HCL	Hydrochloric Acid
FET	Field-Effect Transistor
IL	Ionic Liquid, $C_7H_{11}F_3N_2O_3S$
BJT	Bipolar Joint Transistor
MOSFET	Metal-Oxide-Semiconductor FET
$V_{TH}$	Threshold Voltage
$V_{OV}$	Overdrive Voltage
$I_{DS}$	Current at the drain relative to the source
DI	De-ionized

**ACKNOWLEDGMENTS**

I would like to thank my committee chair, Reza Montazami, and my committee members, Sonal Padalkar, Nicole Hashemi, and Xiang Chunhui for their guidance and support throughout the course of this research. In addition, I would also like to thank my wife Sarah, as well as my friends, colleagues, the department faculty and staff for making my time at Iowa State University a wonderful experience. I want to also offer my appreciation to those who were willing to participate in my surveys and observations, without whom, this thesis would not have been possible.

**ABSTRACT**

An ionic circuit analogous to a traditional metal-oxide semiconductor was investigated, using 1-ethyl-3-methylimidazolium trifluoromethanesulfonate as the ionic liquid in the gating element. The circuit was observed to perform with comparatively high threshold and overdrive voltages in a region below the saturation current of the transistor. The concept of the design was successfully verified, although further improvements in electrode positioning and manufacturing precision are warranted.

## CHAPTER 1. INTRODUCTION AND BACKGROUND

### 1.1 Transistor Background

In 1947, three physicists pieced together a few pieces of germanium in a laboratory at Bell Labs and ran an electrical current through them. To their great delight they found that under the correct loading conditions the current through them could be greatly amplified – and the world was never the same again. Together, William Shockley, Walter Brattain, and John Bardeen had developed the world's first commercially mass producible transistor [1]. Even the Nobel Prize they would later receive for their efforts was inconsequential compared to the eventual future ramifications of their new device.

Transistors currently are used in virtually every electronic device imaginable. From computers to cell phones, to satellites, to surgical equipment they are ubiquitous throughout modern society and are the workhorses that empower modern life as we know it. Without them life in the digital age would simply not be possible. As such, new and innovative ideas about ways to improve them or customize them to different types of applications are extremely promising areas of research.

#### 1.1.1 Types of Transistors

The type of transistor created by the Bell Labs scientists was a Bipolar Junction transistor (BJT) [2]. The Bipolar Junction transistor is so named because its current is carried by both negative and positive charge carriers, electrons and holes respectively, making it bipolar, and because there are physical points of contact between the electrodes, forming the junction. Specifically, the bipolar junction transistor generally is constructed from three

layers of semiconducting materials, each doped with either a positive or negative charge.

These charges are denoted P and N in Figure 1 below.

### Sample BJT Design Schematic

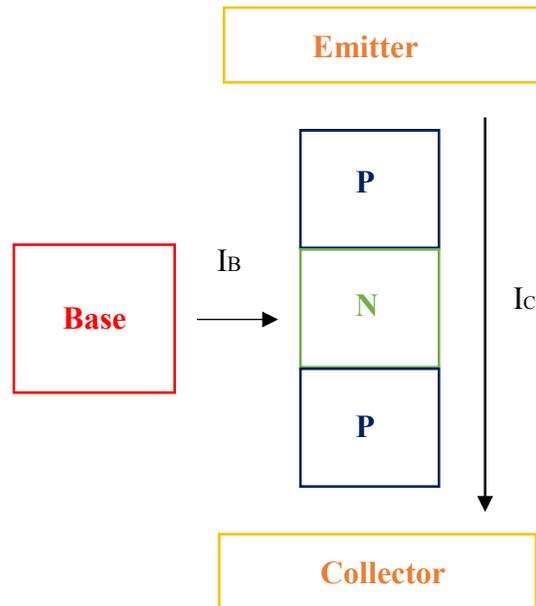


Figure 1. *Sample BJT Design Schematic. Boxes labelled P and N denote layers of positively and negatively doped semiconductor materials. A base current applied to the middle negatively charged layer affects the electrical conductivity of that layer and allows electrons from the other layers to flow more freely through from the emitter to the collector [2].*

The figure above shows only one possible generic design of a bipolar joint transistor; however, it is representative of the general principle of operation. Layers of semiconductors are used to carry a charge from one electrode to another, with an applied current in the middle affecting the electrical conductivity of the carrier material and regulating the flow of electrons. This ability to regulate current flow allows BJT designs to be used both in applications requiring electrical switches, as well as in applications requiring signal amplification [2]. Although BJTs were the first type of transistor to be made commercially viable, they were actually not the first type of transistor ever developed. That distinction belongs instead to the field-effect transistor (FET), first patented by Julius Linienfield in

1928 [2]. The FET differs in many ways from the BJT, starting with its construction. Figure 2 shows a typical generic design schematic for a FET transistor.

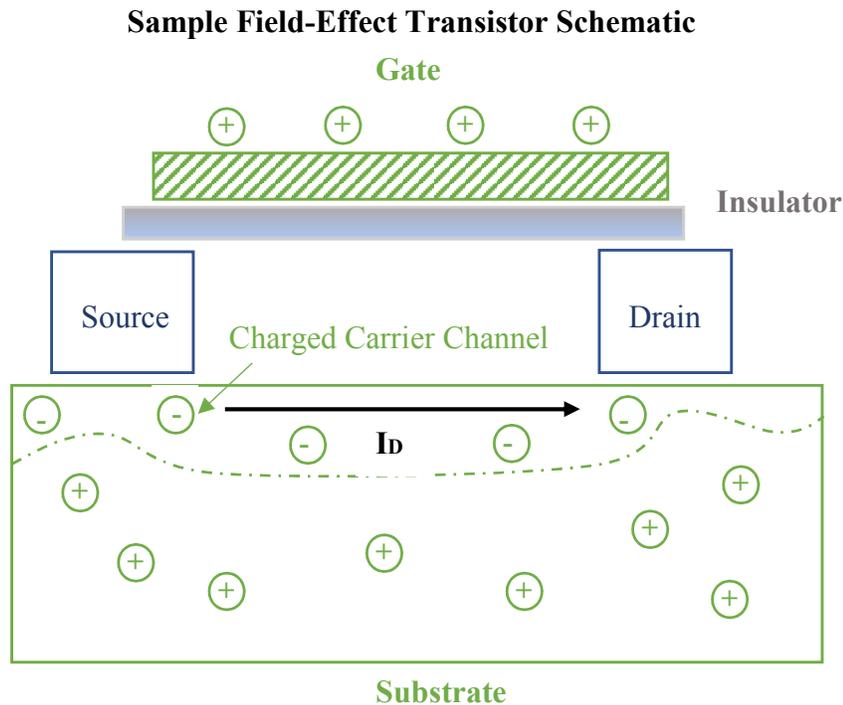


Figure 2. *Sample field-effect design schematic. An electrically isolated gate creates a field effect in the substrate, allowing a charged carrier channel to form between the source and drain electrodes [2].*

There are many types of field-effect transistors, but the one shown above is a representative sample to illustrate the mechanics of their operation. In a FET, an electrically isolated gate is charged with a voltage to create a field-effect around it. The field-effect causes electrons in a nearby substrate to align into regions of like charge, which allows a channel to form carrying a current from the source electrode to the drain electrode. The region of the substrate near the gate where like charged particles have been forced away is referred to as the depletion layer and is an important parameter of these types of transistors [2]. This specific type of FET is

referred to as a metal-oxide-semiconductor-field-effect transistor (MOSFET), so named because the gate material is traditionally made of metal and the substrate material is traditionally made of silicon dioxide.

### **Comparison of BJT and FET Transistors**

The FET design in general and MOSFET configuration specifically have several distinct differences from the BJT. To begin with, as previously discussed, the BJT is a bipolar design because it uses both positively and negatively charged charge carriers [3]. By contrast, the FET design uses only charge carriers of the same charge as the current applied to the gate. The FET transistor is, therefore, a unipolar design. Another major difference between the two designs is that the BJT transistor is regulated by a current, as previously discussed. By contrast, because the FET approach uses an electrical-field, it is inherently a voltage regulated mechanism [4]. Largely due to this, FETs are much more sensitive to small voltage changes than BJTs. This allows them both to be both useful in detecting small voltage changes, but also makes them more susceptible to damage from static electricity [2]. Another large functional difference between the two approaches is that a BJT requires a small amount of current to switch on the transistor. That required current generates a small amount of heat and limits the degree to which the transistor can be miniaturized [2]. For these reasons, among others, FET designs are much widely used today and will be the principal focus of the research presented here.

#### **1.1.2 Important MOSFET Characteristics**

Several characteristics of field-effect transistors make are important to consider when evaluating their performance. The most obvious such characteristic is the current across the source drain electrodes. The drain current can be thought of as the total charge in the

inversion layer divided by the carrier's flow from the source to the drain, given the time required as the length of the gate divided by the velocity of the carrier particle, and the velocity of the particle as the product of the mobility and electric fields [2]. This is described below by Equations 1-3.

$$\text{Eqn 1: } I_D = \frac{-Q_{inversion} WL}{t_r}$$

$$\text{Eqn 2: } t_r = \frac{L_{gate}}{v}$$

$$\text{Eqn 3: } v = \mu E = \frac{\mu V_{DS}}{L}$$

[2]

Noting that  $W$  and  $L$  are the width and length of the gate respectively, and that  $V_{DS}$  is the voltage change from the drain to the source, while further noting that a constant velocity has been assumed for the carrier particles, assuming a steady-state condition to exist. Combining these equations provides a description of gate current as a function of the charge in the inversion field, the properties of the gate, the mobility of the carrier particles, and the voltage change, as shown below in Equation 4.

$$\text{Eqn 4: } I_D = -\mu Q_{inv} \frac{W}{L} * V_{DS} [2]$$

**Constant under Steady-State Conditions**

Of note is that, all of the conditions in Equation 4 can be considered to be constant under steady state conditions, which means that a linear relationship exists between drain current and voltage change across the transistor. This is an important property of FET designs that allows much of their function as a switch between analog and digital signals [3].

Another important parameter to consider when evaluating a MOSFET is its threshold voltage, denoted here as  $V_{TH}$ . The threshold voltage is the minimum voltage that can be applied to the gate in order to form a stable depletion zone and allow steady state current to flow. It is, in effect, the gate voltage required to activate the transistor. The threshold voltage directly affects another important parameter of the transistor, referred to as overdrive voltage. The overdrive voltage can be thought of as the voltage present in the gate-source circuit above the threshold voltage, and is given below by Equation 5 [3].

$$Eqn\ 5: V_{OV} = V_{DS} - V_{TH} \ [3]$$

In a physical sense, the overdrive voltage can be thought of as excess voltage added to the gate circuit strengthening the field-effect and making the conducting channel deeper and better defined. Thus, there is a direct physical connection between the overdrive voltage and the current present in the drain relative to the source, denoted here as  $I_{DS}$ . In cases where the gate voltage exceeds the threshold voltage and overdrive voltage is less than the voltage in the gate-source circuit, additional voltage could still be added to the gate to improve the condition of the conducting channel, and as such increasing gate voltage should increase  $I_{DS}$  current [3]. In cases where the gate voltage exceeds threshold voltage but overdrive voltage has become greater than voltage present in the gate-source circuit, adding further gate voltage will have no further effect on the strength of the electrical field present, and thus the current cannot be further increased. This condition is referred to as current saturation [4].

Finally, the transconductance, denoted below in Equation 6 as mutual conductance is the last MOSFET parameter that will be considered here.

$$Eqn\ 6: g_m = \frac{\Delta I_{out}}{\Delta V_{in}} = \frac{2I_D}{V_{OV}}$$

As previously addressed during the discussion on drain current, the voltage present in the gate and the drain current are linearly related in the region below the point of current saturation. Mathematically, transconductance can be thought of as the linear coefficient relating the two variables. Physically, it can be thought of as the inverse of electrical resistance. It is an important parameter that affects the degree of sensitivity the transistor has to voltage changes and the rate at which it will achieve saturation current. [4]

## **1.2 Ionic Liquids in Field-Effect Transistors**

*“Every year there are more transistors made than raindrops that fall on the state of California”* – Gordon Moore, cofounder of the Intel Cooperation, 2003. [2]

Historically, research into transistors has focused on making transistors as small as possible. For many decades, the race to make transistors as small as possible dominated all discussion in the field [1]. With such avenues of research having been very well explored, fundamental transistor research into other focus areas has recently accelerated greatly though. One such area has been in the materials involved. Ionic liquids are emerging as a promising area of study within the transistor community [5-9].

### **1.2.1 Dielectric Applications of Ionic Liquids in Field-Effect Transistors**

Research into traditional MOSFET type devices without metal gates is hardly new, and has been ongoing for several decades. Early research into the idea was focused on dipping the MOSFET into an aqueous solution to allow a double layer of ions to build along the oxide-solution interface [10]. That layer of ions interacted with the silicon-oxide double-layer already present, which in turn could be used to control the flow of ions and current. More recent research has focused on using ionic liquids in thin-films forming the gating

mechanisms in such devices. The ionic liquid thin-films have been found to have superior capacitance [10].

Ionic liquids have been used in many novel ways in field-effect transistors. Among others, research from Weingarth *et al.* in 2013 has shown the potentials of 1-ethyl-3-methyl imidazolium bis(trifluoromethylsulfonyl)imide ionic liquid as an effective gating method in a wide variety of different structures and geometries [11-13]. Ionic liquids have been used in other, more traditional, means as gating mechanisms as well. An interesting application of ionic liquids to FETs is to replace the insulating dielectric material with an ionic liquid instead. Research from Fujimoto *et al.* in 2009 showed that a FET based on a gate dielectric insulating layer of N-diethyl-N-methyl(2-methoxyethyl) ammonium bis(trifluoromethylsulfonyl)imide) ionic liquid was able to exhibit very high carrier mobility of  $2.4 \times 10^{-2} \text{ cm}^2/\text{Vs}$  at comparatively low power levels [14]. An interesting property of ionic liquids as dielectrics is their potential for inducing high capacitance properties in transistors utilizing them. Because they are using large –and often very large– ions, rather than electrons, to transfer electric charge their potential to store electric energy in the form of capacitance is great [3]. A study similar to the preceding one was conducted by Ortiz *et al.* in 2018 in which a high capacitance ionic liquid was used as the insulating material for an FET and was able to achieve average charge density orders of magnitude better than traditional silicon dioxide due to better than average charge injection into the carrier channel and reduced contact resistance [15]. Indeed, other groups reported similar results using related innovative approaches to IL insulators. For example, a group led by Zhou in 2012 compared traditional electrostatically doped oxide gate insulators with a double layer of an ionic liquid-based gating insulator [16]. Such double-layered configurations have been explored by many

other researchers, with ionic liquid-graphene interfaces becoming a subject of much interest in recent years [5,7,8]. In 2015 Gonnelli et al. studied the temperature dependence of electrical properties of structures based on three to five layers of graphene. They were able to demonstrate large surface charge densities in the layered graphene, on the order of  $6.8 \times 10^{14}$  /cm<sup>2</sup>. [8] Another study investigating bi layer graphene systems in conjunction with lithium by Kuhne et. al. found that such systems could greatly increase ionic diffusion. They were able to demonstrate diffusion coefficients as high as  $7 \times 10^{-5}$  cm<sup>2</sup>/s within the graphene layer [14]. While in a 2012 study by You *et al.*, traditional oxide-based FET gates were found to be able to achieve a carrier particle concentration of approximately  $10^{13}$  particles per square centimeter, while the double layered ionic liquid approach was able to achieve carrier particle densities of approximately  $10^{14}$  particles per square centimeter – an entire order of magnitude larger [16]. Interestingly, the additional particle density opens up the possibility of inducing a phase-transition in several commonly used oxide materials – a prospect the authors viewed as a promising area for further research [16].

One interesting approach to using ionic liquids in FETs is to take advantage of their chemical properties and use them as detectors. By changing the classic MOSFET gating mechanism to make use of an ionic liquid, in 2008 a group led by Saheb used the IL 1-butyl-3-methylimidazolium bis(trifluoromethanesulfonyl)-imide in a composite in conjunction with camphor-sulfonic acid to detect the presence of ammonia gas [17]. The ammonia reacted with the composite gate, changing the gating voltage present in the circuit and triggering the detection of the gas. The device was able to detect concentrations of the gas as low as 0.5 ppm [17]. Ono et. al. investigated an IL with the same base cation and five different anions, including the bis(trifluoromethanesulfonyl)-imide variant investigated by Saheb's group, as

well as four other anion combinations to attempt to optimize the choice of IL for a given application [7]. By optimizing the gating IL, that group was able to show mobility of up to  $9.5 \text{ cm}^2 / \text{V s}$ , which they concluded verified the efficacy of the field-effect switching mechanism [7]. In another study by Ohn's group, rubrene single-crystal transistors with an IL bilayer used for gating. That study showed fast ionic-diffusion allowed the capacitances of the bilayers to stay at more than  $1 \mu\text{F} / \text{cm}^2$  even while operating at 1 MHz [8]. The study suggested that such transistors could be readily adapted to low power, fast-switching operations [8].

Indeed, ionic liquids have been used as a wide variety of different gating mechanisms and applications. Perhaps one of the most interesting is one reported by Greenlee et al. in 2014. Currently, most attempts at neuromorphic computing applications involve the use of either digital or analog silicon devices to emulate the biological phenomena of the brain [6]. A more intuitive approach would perhaps be to pursue an ionic-electronic device more similar in morphology and function to the actual brain itself. This was the approach pursued by Greenlee et al. when they studied the effects of a lithium-cobalt-dioxide ionic liquid-based transistor. Their conclusions include that similar nanoscale-based transistors would use much less power than conventional alternatives while also being less prone to damaging phase changes. These properties may make the material the ideal basis for a neuromorphic computing application [6].

### **1.2.2 Geometric Design Considerations of Ionic Liquids in Field-Effect Transistors**

An entirely different approach to using ionic liquids in transistor design involves their potential for innovations on the classical MOSFET design. Although conventional research

on the miniaturization of FETs has focused on the more conventional designs previously discussed, currently ionic liquid gating has been shown to be the best method of controlling field-electric effects in nanoscale semiconductor structures [18]. As the search for new ways to miniaturize transistors continues, the future may indeed belong to ionic liquid FETs. One approach to nanoscale ionic liquid FETs involves the use of conical nanoparticles [19]. Research has been conducted by Kalman *et. al.* into varying the cross-sections of the transistors in question from the standard, symmetrical layered configuration into a conical shape making use of ionic transport. The configuration was found to increase the polarization of particles at the gate and lead to linear type changes in output current not typical for conical configurations when the gate voltage was varied [19]. Conical nanopores are also easily scalable and appear to be an exciting new area of research for scientists in several different research areas including solid state physics [20], electrochemistry [21], and others [19]. Another interesting area where ionic liquids are changing the structures of existing FET designs in the realm of nanowires. Recently (in 2019) Lieb *et al.* conducted the first comprehensive study of an ionic-liquid based gating mechanism in individual semiconductor nanowires [5]. The nanowires showed an incredible transconductance value of approximately 30 times that of a conventional silicon-dioxide substrate. Like many other groups using ionic liquids in FETs, they reported high carrier particle density and attributed the high transconductance observed to this phenomenon [5]. Due to the interesting new geometry of the nanowires, the potential exists that they could be used in a wide variety of different configurations and that they may be well suited for emulating biological systems. Perhaps the most novel application of ionic liquids in FETs is in the area of three-dimensional transistors. Historically, in regard to their core functionality transistors have

been essentially treated as two dimensional devices. A recent novel approach has used a three-dimensional graphene structure immersed in an ionic liquid to create a three-dimensional ionic liquid-based FET [18]. The three-dimensional structure was used as a hypersensitive pH sensor, demonstrating sensitivity of  $71 \pm 7$  mV/pH in molarities as high as  $298 \pm 1$  mM. The sensor is made more accurate, in part, due to the increased surface area of the three-dimensional structure. However, like other studies discussed so far, it also makes use of the increased efficiency of the carrier particle density in the channel to increase gating control of ions and lead to greater sensitivity; the three-dimensional nature of this example simply magnifies the effect [18]. Clearly, there are many interesting applications of ionic liquids to FETs with much potential remaining for their future development.

### **1.3 Discussion of the Experimental Design**

The focus of the research presented here will be to investigate an ionic-liquid FET modeled on a classical MOSFET design. The transistor will use 1-ethyl-3-methylimidazolium trifluoromethanesulfonate ionic liquid, using the same cation base and very similar to the 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide proven to be effective in ionic transistors in other well documented research [7, 11]. Figure 3 provides a conceptual schematic of the transistor design to be studied.

### Ionic-Liquid Field-Effect Transistor Schematic

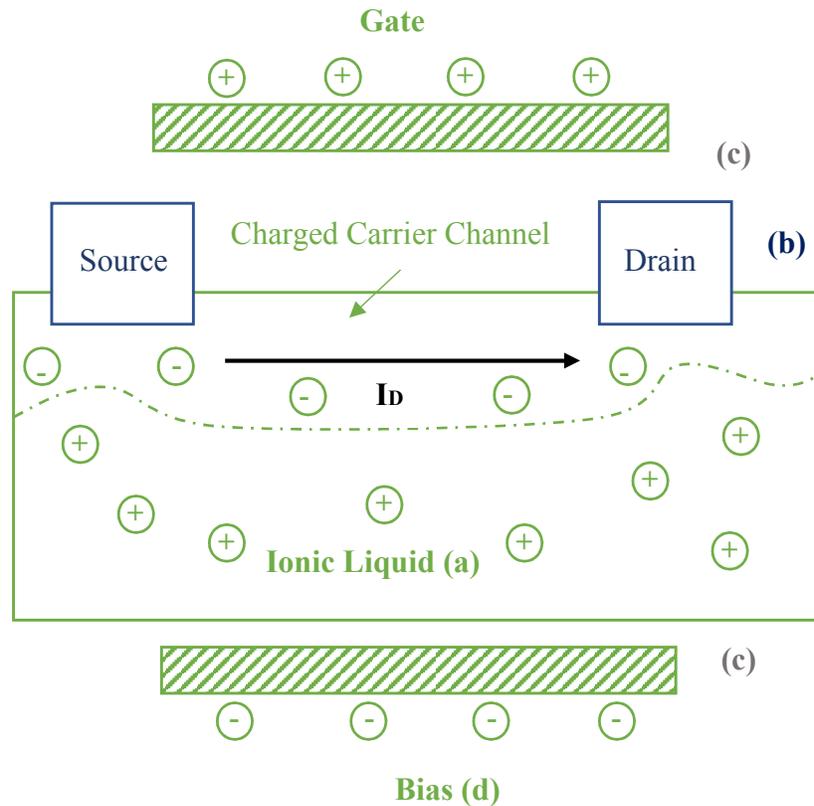


Figure 3. *Ionic-liquid field effect transistor-schematic. (a) Substrate from MOSFET design replaced with an ionic liquid. (b) Source and Drain electrodes immersed in the ionic liquid, rather than resting on top of it. (c) Gate insulator removed and replaced with air. (d) Second bias gate emitter added.*

The schematic above shows several differences from the generic MOSFET transistor design previously discussed. Notably, the substrate material has been replaced with an ionic liquid.

The much larger ions of the ionic liquid will replace the electrons of the substrate as the charge carrying particles. The source and drain electrodes have been immersed in the ionic liquid in order to facilitate this function. Additionally, the insulating material between the gate and the source and drain electrodes has been replaced with a simple air gap. Finally, a second bias electrode has been added opposite the gate to better facilitate the generation of an electric field across the ionic liquid. The second gating electrode strengthens the field

present. This should ideally serve to lower the threshold voltage of the circuit so that smaller gate voltage inputs can be explored while simultaneously reducing the overdrive voltage required for current saturation.

## CHAPTER 2. EXPERIMENTAL PROCEDURE AND RESULTS

### 2.1 Experimental Setup

The pattern shown below, Figure 4, was cut onto vinyl using a US Cutter Model SC vinyl cutter. The vinyl used was manufactured by ORACAL, product number 631M-070.

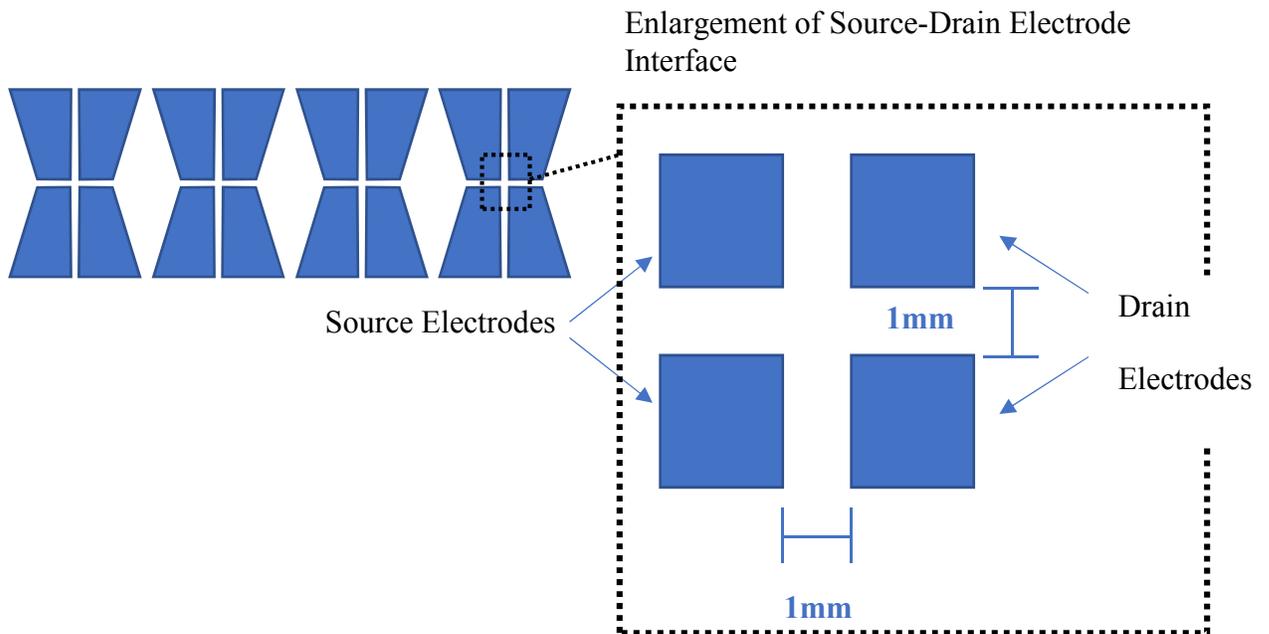


Figure 4. *Basic source-drain electrode geometry. The geometry was replicated multiple times to allow for quicker repeated experimentation.*

The design was sized to be 75.7 mm in length by 24.9 mm in width, to match the size of a standard laboratory slide. It was chosen primarily for its spacing between electrodes, its ease of manufacture with the available printer, and so that multiple circuits would be available for testing at a time. The electrodes were spaced to be 1 mm apart in order to allow adequate room for the development of the depletion layer, while still allowing sufficient field strength from the gate electrode to be an ideal spacing for facilitating ionic movement. At the range of

voltages involved, this spacing should ideally allow maximum benefit from the electromagnetic field throughout the fluid while not being so small as to allow electrical arcing between the two electrodes without requiring transmission through the fluid. It is one of the primary design considerations of this approach.

Once the vinyl was cut into this shape, it was manually transposed onto the coated side of a single-side coated Indium-Tin Oxide (ITO) slide, manufactured by Delta Technologies of Loveland, CO (Part number CG-51IN-S107) to mask electrode patterns from acid etching (next step) using transfer tape.

The next step of the experimental procedure involved the preparation of an acid bath to submerge the slide into and remove the ITO coating from the areas of the slide not protected by the vinyl mask. Doing so left ITO coating only on the areas in the original design from Figure 1 intended to be electrodes. The etching solution was composed of 75 ml of hydrochloric acid (HCL 36.5%, 38% wt%, BDH), and 75 ml of DI water. The ITO slide was submerged into the etching solution and mixed vigorously for 20 minutes at room temperature. The slide was then washed in DI water, dried, and tested for removal of ITO from the desired areas.

The next step of the experimental process was the creation of copper electrodes from copper foil of 5 mm thickness. A diagram showing the design of the copper electrodes is shown in Figure 5.

### Top Down View

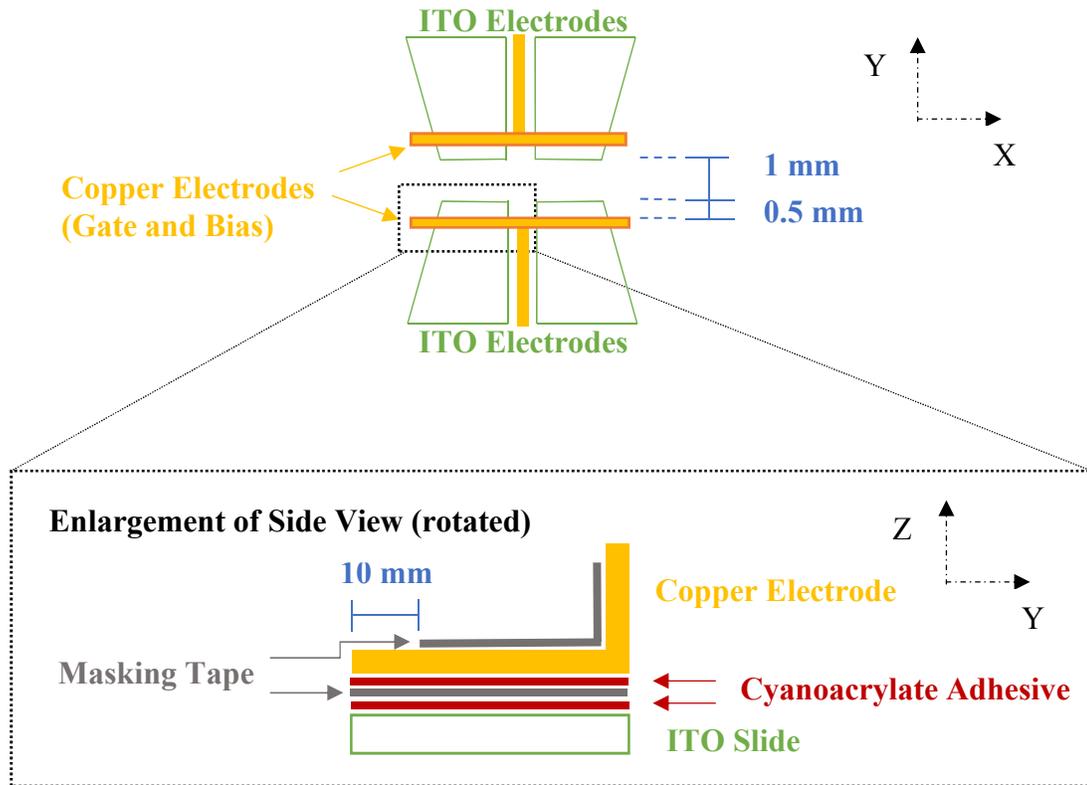


Figure 5. Schematic of the copper electrodes, used to create the bias and gate circuits. Orientation of the enlargement changed to show position of insulation and adhesives.

In order to fabricate the gate and bias circuits, two copper electrodes were cut out of a 5 mm thick copper foil into the shapes shown above in Figure 5. Masking tape was affixed to the bottom of the copper electrodes in areas it would potentially contact the ITO coating with cyanoacrylate, to serve as an electrical insulator between the copper and the ITO. The same masking tape was then affixed into position on the top side of the copper with the cyanoacrylate from the top of the copper electrode to 10 mm from the base of the copper electrode in order to insulate it as much as possible from potential electromagnetic interference in the background. The base of the copper electrode was left exposed in order to attach a power supply later in the experimental process. The copper electrodes were then positioned 0.5 mm above the edge of the exposed ITO electrode –in order to assure part of

the ITO electrode remained exposed for later experimentation– and affixed into place using the cyanoacrylate. The setup was dried for 15 minutes to assure the proper bonding of the adhesive. Finally, a hot glue gun was used to form a thin wall connecting the two copper electrodes at each end. The hot glue was placed from the bottom portion of the copper electrode in contact with the slide to the top of the electrode. These hot glue connections served to both maintain the distance of the copper electrodes from each other throughout the experiment, and also to contain ionic liquid that was subsequently added. The hot glue was allowed enough time to solidify.

The next portion of the experimental process involved the electrical setup. A GW INSTEK Model GPS-18500 DC power supply was connected to the exposed base of the copper electrodes using alligator clips. The positive terminal of a second power supply, a BK Precision Model 1686A DC power supply, was connected to one of the exposed ends of an ITO electrode along the base of the slide using an alligator clip. The negative terminal of the second power supply was connected directly to a Tektronix DPO 3014 Digital Oscilloscope channel. The corresponding second port of the oscilloscope was then attached to the adjacent ITO electrode with an alligator clip, in order to measure potential change across the circuit. The electrical setup is shown in Figure 6.

## Diagram of the Experimental Setup

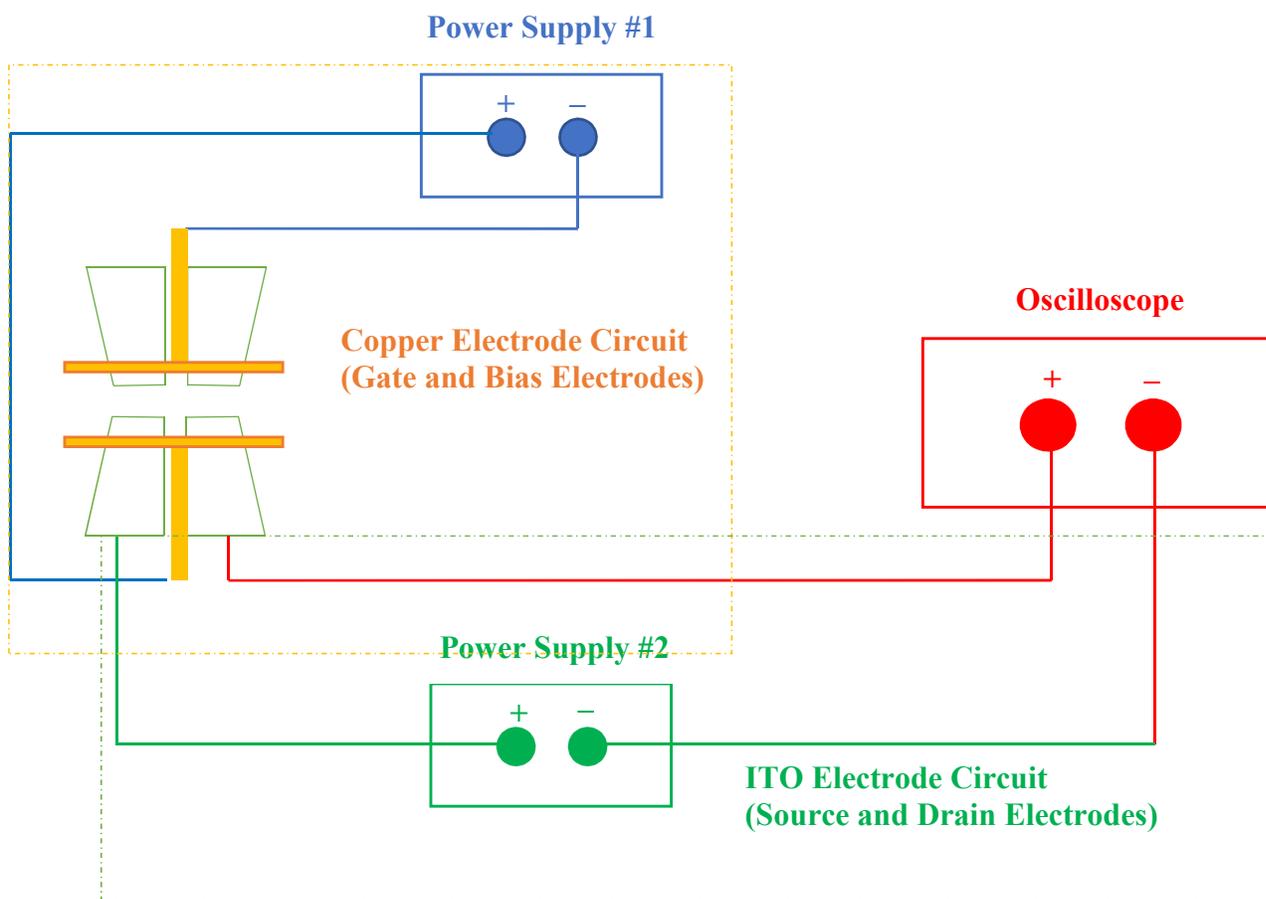


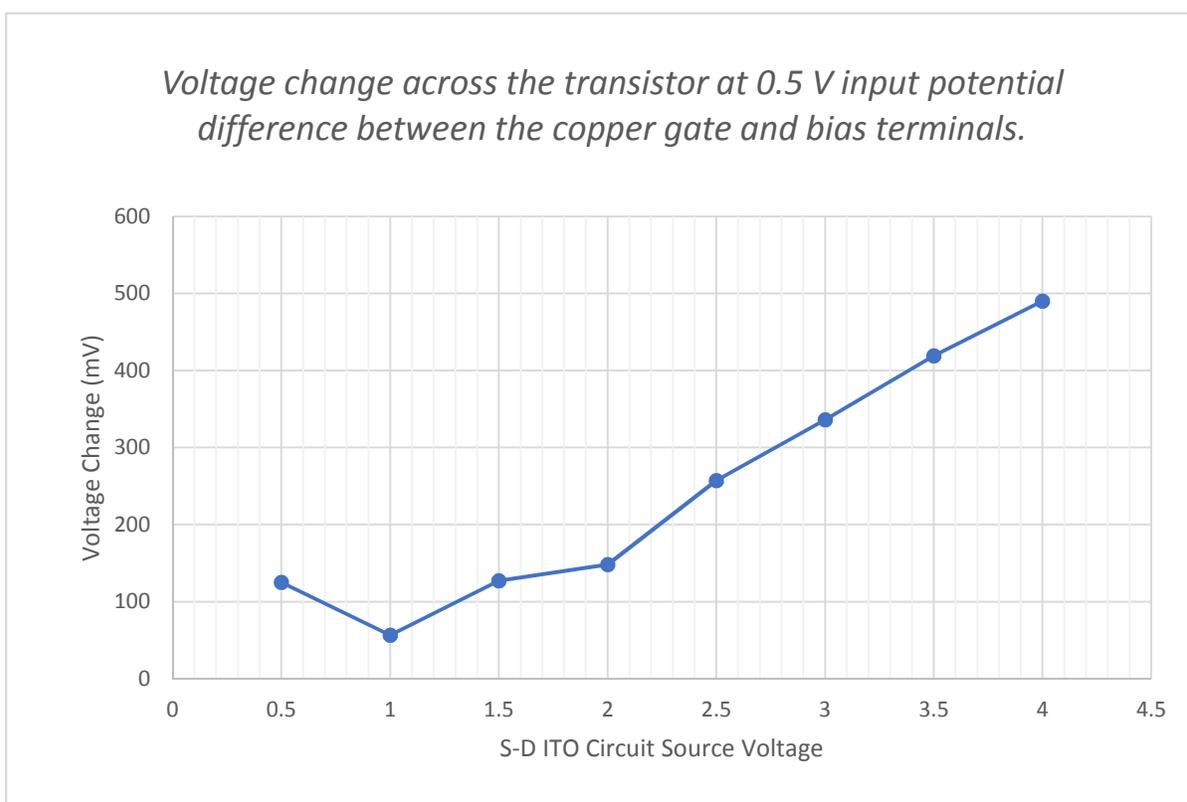
Figure 6. *Electrical diagram of the experimental setup. All circuits are connected via commercially available copper wiring and alligator clips provided with the various devices.*

Finally, enough of the ionic liquid was inserted in the space between the two copper electrodes with a micropipette so that it formed a thin layer across the entire enclosed surface. The ionic liquid used was 1-ethyl-3-methylimidazolium trifluoromethanesulfonate (EMI-Tf, molecular formula:  $C_7H_{11}F_3N_2O_3S$  Sigma Aldrich, St. Louis, MO, USA). This step concluded the experimental setup.

### 2.2 Experimental Process and Results

With the experimental setup completed, the first power supply was turned on and set at 0.5 V. The second power supply was turned on set at 0.5 V. The potential voltage change across

the ITO circuit was measured using the oscilloscope. The voltage in the second power supply was then slowly adjusted in 0.5 V increments, starting from the initial 0.5 V and increasing up to 4 V, with the voltage change across the ITO circuit measured by the oscilloscope at real-time. A limit of 4 V was selected primarily because the ionic liquid selected here begins to degrade at approximately 4.5 V. Three minutes were allowed between each reading to allow the ionic circuit ample time to adjust to the new electrical setting before a measurement was taken. Four different measurements were taken at each voltage level. Results from this process are shown in Figure 7.



(a)

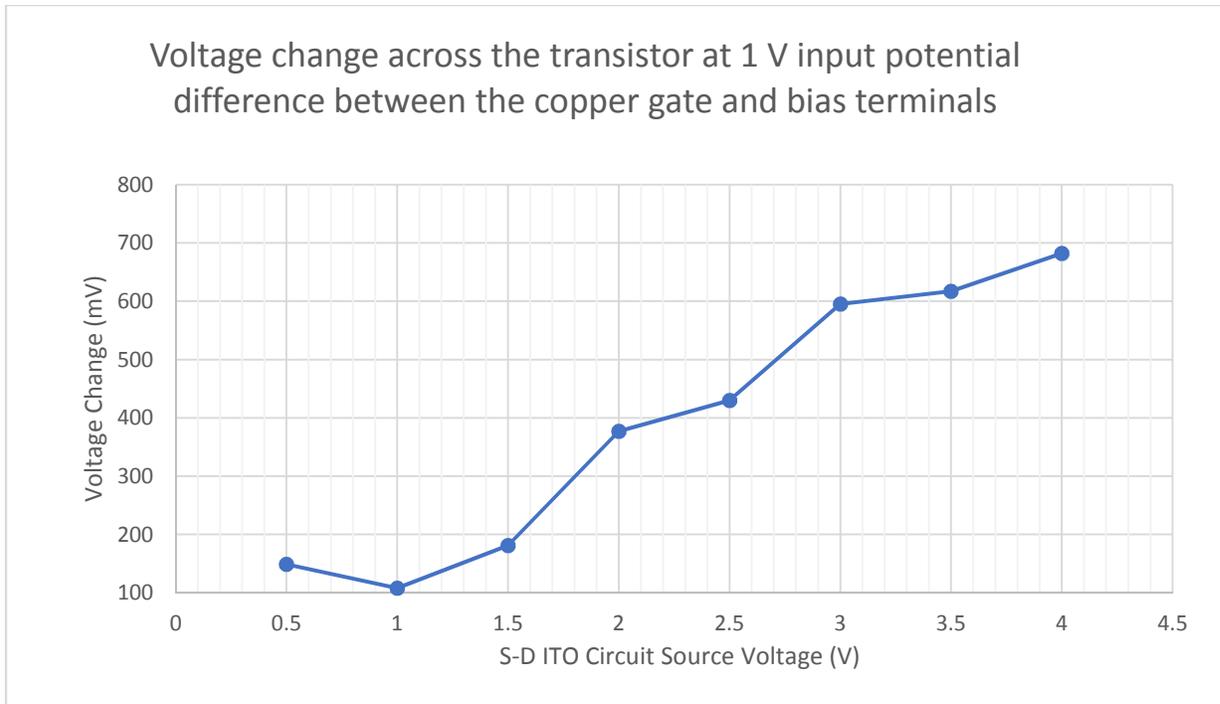
Figure 7. (a) Graph of voltage change across the transistor at 0.5 V input potential difference between the copper gate and bias terminals.

<b>Gate Circuit Voltage: 0.5 V</b>		
<b>Source Voltage (V)</b>	<b>Voltage Change (mV)</b>	<b>Standard Deviation (mV)</b>
0.5	125 ± 42.5	43.4
1	56.5 ± 37.8	38.6
1.5	127 ± 37.2	38.0
2	148 ± 23.2	23.7
2.5	257 ± 22.9	23.4
3	336 ± 40.0	40.9
3.5	419 ± 60.8	62.1
4	490 ± 45.9	46.8

(b)

Figure 7. (continued) (b) Table of voltage change across the transistor at 0.5 V input potential difference between the copper gate and bias terminals. Values given with voltage change include 95% confidence intervals and standard deviations.

As suggested by the data (Figure 7a), the voltage gain across the transistor did increase in an approximately linear way. Noteworthy, however, is that when the voltage was increased from 0.5 V to 1 V, there was an unexpected drop in potential across the transistor. This occurred only at the 1 V level. The surprising result can possibly be attributed to a combination of three factors. First, in general the transistor seems to be less responsive at low voltages and has likely been unable to firmly establish a depletion region. Second, as seen by the confidence intervals and standard deviations in Table 7b, there exists a significant degree of uncertainty in the measurement itself, which is amplifying the degree of the variance. Third, in the earlier tests a significant ambient background noise was found affecting the results of the experiment. The effects of this background radiation were addressed by adding further insulation where possible. This additional insulation was found to greatly mitigate the problem. However, it may still be that this unprecedented observation is a result of that ambient background radiation.



(a)

Gate Circuit Voltage: 1 V		
Source Voltage (V)	Voltage Change (mV)	Standard Deviation (mV)
0.5	149 ± 26.6	27.2
1	108 ± 39.1	39.9
1.5	181 ± 23.9	24.5
2	377 ± 34.6	35.4
2.5	430 ± 30.9	31.6
3	595 ± 61.5	62.8
3.5	617 ± 55.5	56.7
4	682 ± 82.5	84.2

(b)

Figure 8. (a) Graph of voltage change across the transistor at 1 V input potential difference between the copper gate and bias terminals. (b) Table of voltage change across the transistor at 1 V input potential difference between the copper gate and bias terminals. Values given with voltage change include 95% confidence intervals and standard deviations.

Interestingly, as can be seen above, the same aberration at the 1 V level appears again in this new set of data – the voltage gain across the transistor again dropped lower than the 0.5 V reading when the gate voltage to the copper circuit was set at 1 V. This suggests the depletion

layer and carrier channels at this gate voltage have not been able to be fully established and that this is effectively below the threshold voltage for this transistor. Otherwise, the data from this test seems to once again follow a relatively linear progression as would be expected.

The next stage of the experimental process was to continue increasing the voltage present in the copper circuit in half-volt increments, repeating the experiment as before. It was determined that 4 V would be an appropriate upper limit for several reasons. First, the ionic liquid used here begins to degrade at approximately 4.5 V. Second, this lower voltage area is of more interest in many practical applications appropriate for small-scale transistors [4] the transistor could possibly be applied toward, and the number of data points acquired was sufficient to verify the success of the design. Furthermore, this gate voltage level is analogous to many other comparable transistors [3]. Additionally, due to the small distance between the two source and gate electrodes and the potential for electricity to arc across them without using the ionic liquid at all as a transport mechanism the gate voltage had to be limited. In order to completely avoid the potential for electrical arcing in this manner, the maximum limit was set to 4 V. The process was thus further repeated with the first power supply supplying 1.5 to 4 V of power, in 0.5 V increments, while varying the second power supply between 0.5 to 4 V each time as before. As such, in total 64 readings of electrical potential change across the transistor were measured. The remaining readings no longer showed as significant dips at the 1 V input level, and generally showed linear behavior as described above. For these reasons, the data from these six additional tests in the 1.5 to 4.0 V range have been combined with the first two tests at the 0.5 V and 1.0 V levels, and are presented together below in Figure 9 for ease of comparison and simplicity. Additional tables

for the results of the data presented in Figure 9 are available in Appendix A.

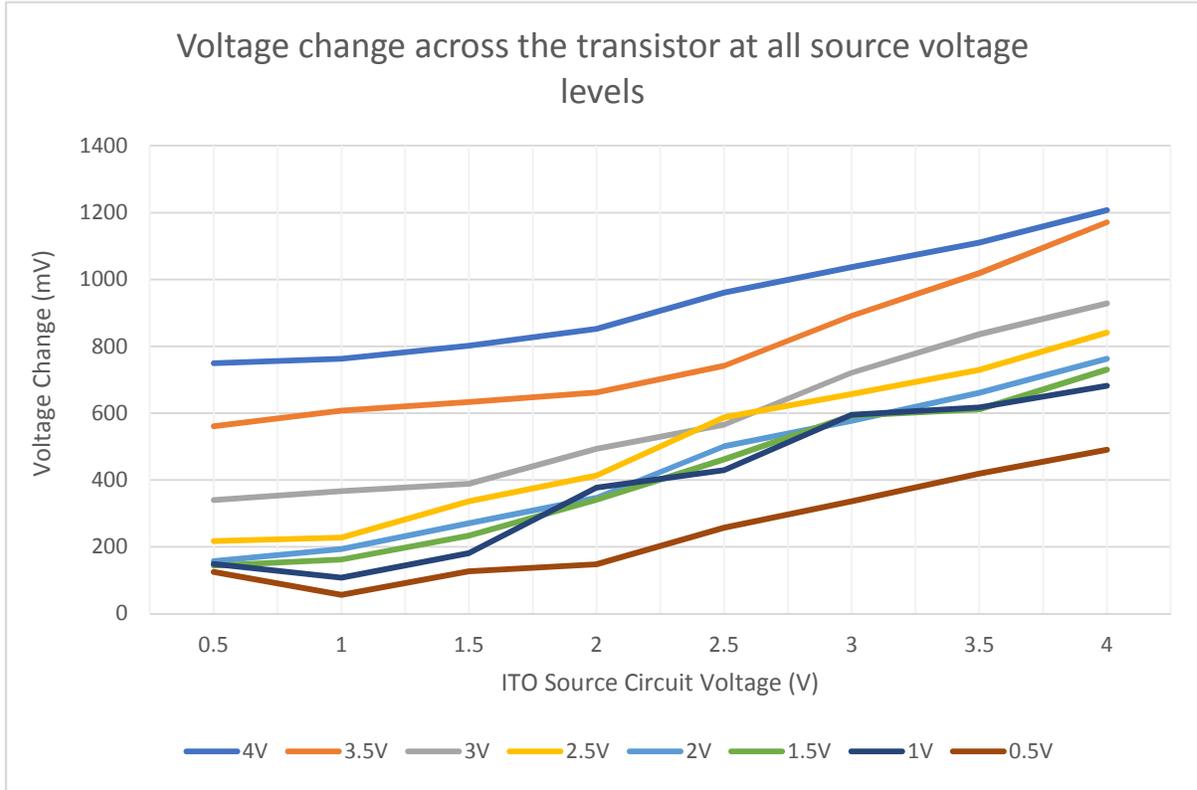


Figure 9. *Voltage change across the transistor at all source voltage levels. Colored values indicate various gate-bias potential differences.*

There are several interesting points of note in the chart above. Theoretically, the voltage change would be expected to increase as the voltage to both the copper circuit and the ITO circuit are raised within the linear region below the current saturation zone in which the transistor is clearly operating. The change across the transistor should, in turn, theoretically always be higher when compared at the same copper circuit gate-bias voltage if the ITO source-drain circuit voltage is increased as long as the transistor remains in this region. This predicted behavior, does in fact hold throughout most of the readings taken, with three exceptions. Twice during the 1 V input test, the voltage change across the transistor was measured to be higher than that during either the 1.5 V or 2V tests. These were the most

significant exceptions since the values exceeded not one but both of the tests immediately afterward. Another more minor exception occurred with the voltage set at 2.5 V for both circuits; at this setting the change across the transistor slightly exceeded the measured change with the ITO circuit input voltage set at 3 V. Looking more broadly at the values from the 1 V through 2.5 V tests, all of the values were much closer together with less percent difference separating them than other test ranges. The transistor, in effect, was less sensitive to changes in the copper circuit gate voltage within this 1 V to 2.5 V range. Above this range, the readings become much more linear and predictable. Another additional interesting point of note here is that, although the dip at the 1 V level previously discussed during the discussion of the results from the 0.5 V and 1 V copper circuit input levels was no longer present in measurements taken above 1.5 V, the rate of voltage change between 0.5 and 1.5 V ITO circuit input was consistently less than the same rate within the 2.0 to 4.0 V ITO circuit input ranges. Thus, in effect, the transistor behaved the most erratically at gate-bias circuit input levels below 2.0 V and at source-drain circuit input levels below 3.0 V.

Another interesting point of note with this transistor design is that it behaves differently from a standard transistor in that the input voltage is being greatly reduced rather than increased. For this reason, and because the sensitivity of the transistor to changes at various levels is of interest in its design and function, it is useful to know the percentage of the original voltage applied to the ITO circuit that successfully travelled across the transistor at various power levels. Figure 10 shows these percentages.

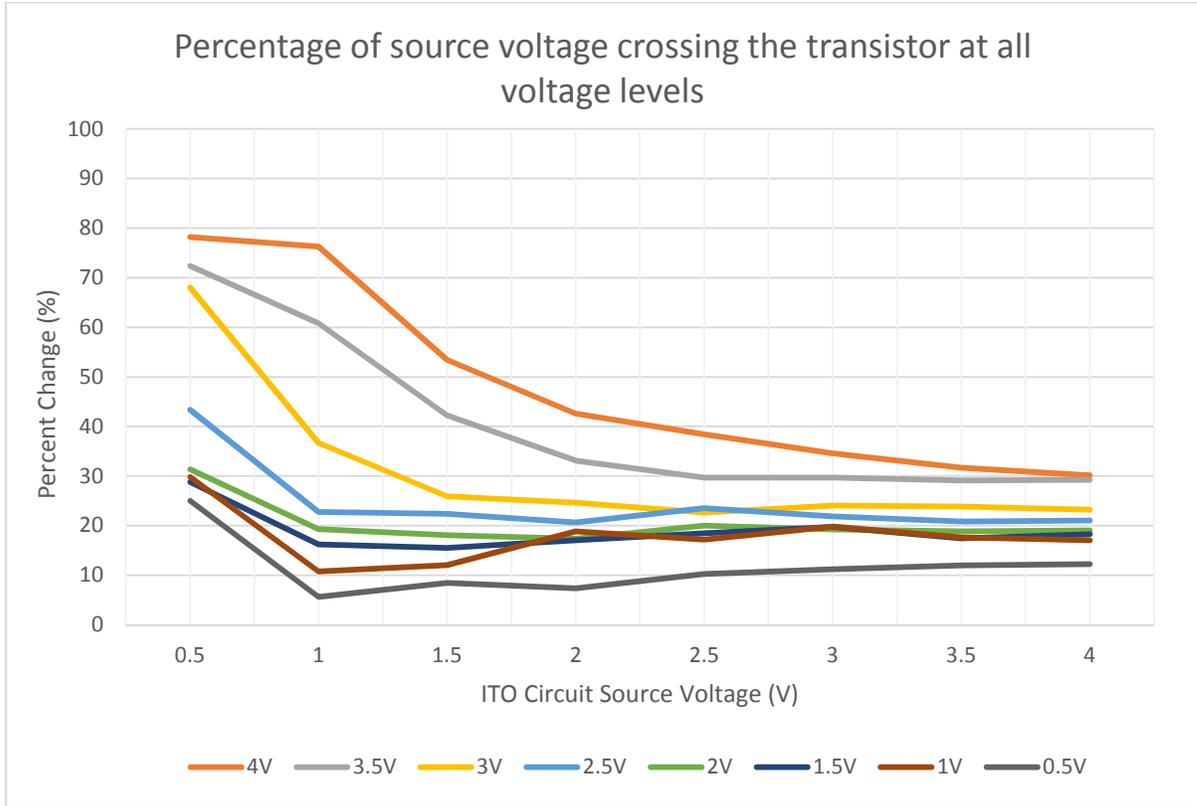


Figure 10. *Percentage of original source circuit voltage crossing the transistor at all gate and source voltage levels. Colored values indicate various gate-bias voltage levels.*

To begin, the effects of varying the copper circuit gate voltage levels are of immediate note in the above figure. In general, the percentage change is much lower for lower gate circuit input levels and is much higher for higher levels. This trend holds broadly for all ITO circuit levels, with the previously mentioned low voltage aberrations notwithstanding.

The effects of varying the ITO source circuit input level are interesting. For gating voltages higher than approximately 2.5 V, higher source voltages result in lower percentages of voltage crossing the circuit. However, for gating voltages lower than 2.5 V, the percent change is much less pronounced as source voltage increases. This observation further supports the prior observation that the effective threshold voltage for this circuit is below the 2.5 V level. It can also be seen that the difference in percent change as ITO circuit input level

increases behaves much more linearly than the same difference as copper circuit gate input level increases. Both this observation and the prior observation showing relatively consistent percentage increases as source voltage increases suggest that the transistor has not yet achieved current saturation. Further, because the ionic liquid used is unable to accommodate voltages of much greater than 4 V without suffering degradation, it is likely this IL FET design is unable to achieve current saturation at all.

## CHAPTER 3. OBSERVATIONS AND CONCLUSIONS

### 3.1 Comparisons: Standard FETs versus the IL FET

Although the quantitative performance of classical and IL FETs is very dissimilar, in considering the performance of the IL transistor, it is useful to qualitatively compare its performance to the expected performance of a more traditional unipole field-effect transistor using a solid semiconducting material for the gate. As discussed earlier, several critical parameters exist for gauging such performance including:  $V_{TH}$  required to activate the transistor, the transconductance of the transistor, and the  $V_{OV}$  present in the gate-drain circuit, among others. First, electrical diagrams of the circuits [2] are compared below in Figure 11 and then these parameters are explored in more detail in Figure 12.

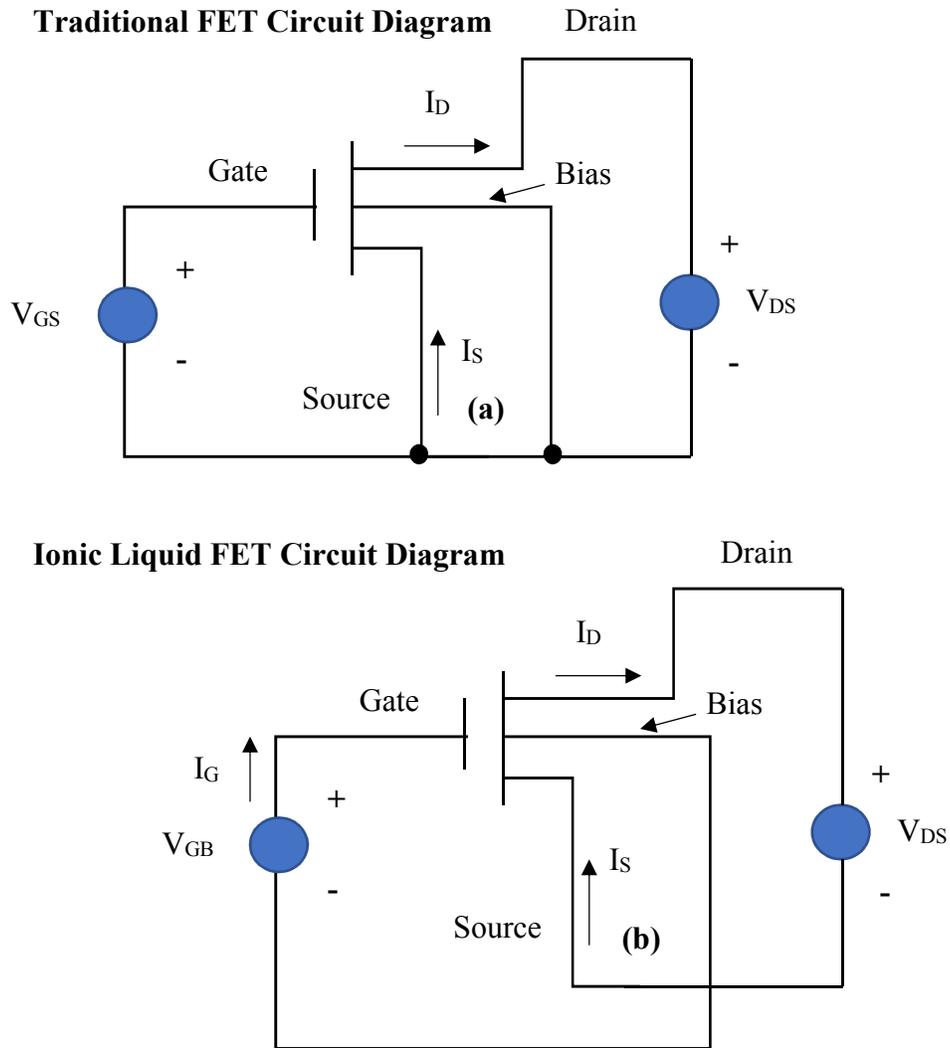


Figure 11 *Comparative circuit diagram (a) electrical connection between the two circuits (b) unconnected circuits*

As can be seen in Figure 8, a traditional design will typically include an electrical connection between the source electrode and the substrate body, used as a bias voltage. This key difference in circuits makes the concept of transconductance much more mathematically meaningful than in the case of the ionic liquid FET used in this experiment. For this reason, among others, investigating the current present was beyond the scope of this study.

Nevertheless, broadly the concept of the amount of current crossing the transistor still is interesting to consider and based on measured voltage and ohm's law an approximation of

the current crossing the IL transistor is possible. Additionally, the threshold voltage is interesting to consider as well. They are both compared in Figure 12.

### Comparison of the Idealized Behavior of the MOSFET and IL FET Devices

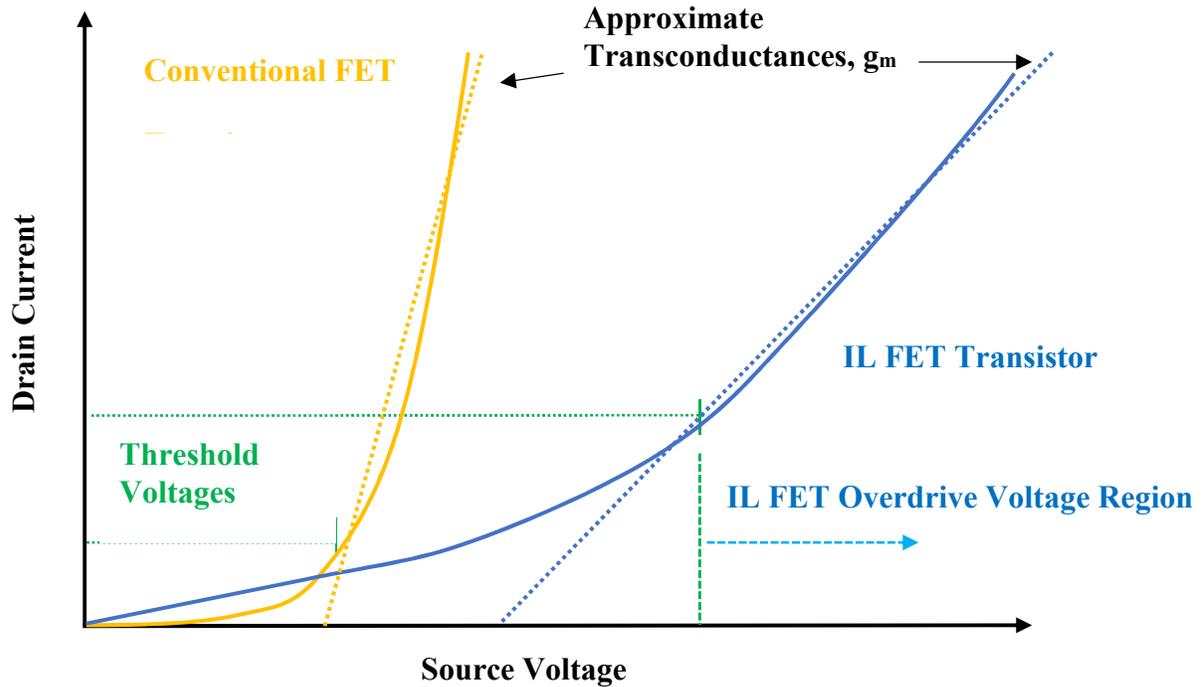


Figure 12 Comparison of MOSFET and IL FET Circuits. A qualitative comparison of the threshold voltages, approximate transconductances, and overdrive voltages of conventional semiconductor-based [2] and ionic-liquid-based field-effect transistors.

One of the main differences between the IL transistor considered here and a more conventional alternative [2] is the difference in threshold voltage required to activate the circuit, as was presented in Figure 9. A conventional transistor will typically require only a small amount of current through before reaching a threshold source voltage, after which case the drain current will respond dramatically to any further source voltage increases. As was seen earlier from the IL circuit data, this was not the case here. Rather, there was a slow linear correlation that gradually increased as source voltage increased. Nevertheless, the IL transistor investigated here did behave erratically below a source voltage of 1.5 V and this

could be viewed as an effective threshold voltage for the IL circuit for that reason. It should also be noted that this effective threshold voltage is probably the result of the geometries and manufacturing techniques unique to this experimental proof-of-concept, and is likely not a limitation of IL FET transistors in general.

Another main difference between the two types of transistors, also seen in Figure 9, is the rate at which the transistor allows current through once the threshold voltage has been reached. This transconductance effect is very pronounced in the traditional FET – once the threshold voltage has been reached the gate will allow as much source current through the transistor as is supplied, limited only by its comparatively slight resistance. The electrical resistance present in the gate, the ionic liquid itself, of the IL FET is clearly much greater. This is predictably so; the IL FET is using individual ions to conduct the current across the gate whereas the traditional transistor is simply using electrons. Because the ionic liquid used in this experiment has a mass of about 260.2 grams per mole and, by comparison, a mole of electrons has a mass of about  $5.48 \times 10^{-4}$  grams, it's easy to theorize both why the IL transistor – using much heavier carrier particles – would have a higher threshold voltage and why it would be slower to respond to increased voltages in the form of lower transconductance values. This effect is magnified even further when one also considers the effects of distance predicted by Faraday's law and the fact that the distance between electrons in a traditional design and the distance between ions in the design considered here also differs by a similar degree of magnitude. This slower response need not be considered a negative though. Rather, it raises the potential to apply these types of transistors to entirely new and diverse types of applications that have not currently been considered in which the lower transconductance can be considered an asset. This fact makes the IL circuit investigated here effectively behave as

something of a hybrid between the bipolar joint transistors previously discussed and a typical FET. Examples where this might prove useful include cases where more output sensitivity to a wide range of voltage levels above the threshold voltage is desirable, as the IL FET transistor provides more granularity in the resulting current, or where the output heat produced by a BJT device is undesirable.

Finally, the overdrive voltage previously alluded to is also interesting to consider for the two circuits. Although, in a manner analogous to transconductance, it is not directly possible to mathematically compare overdrive voltages for the two designs because of the difference in the electrical circuits present previously discussed and illustrated by Figure 8, again like conductance, the broader concept of excess voltage applied to the gate circuit is still useful to consider. In a traditional FET design based on a semiconductor material, a small amount of voltage is applied to the gate-bias circuit in order to gain a large amount of current in the source-drain circuit once the threshold voltage has been surpassed. As the gate voltage is increased, the overdrive voltage of the transistor increases. The net effect is increased stability of the carrier channel in the depletion region until current saturation is reached, and greater drain current present in the transistor. In the case of the IL FET transistor investigated here, it is expected to behave in much the same way. Indeed, the linear nature of the data previously discussed clearly in Chapter 2 supports that this IL FET does behave as described and, further, remains in the overdrive region without yet reaching current saturation. As also discussed earlier in the experimental results section, the percent voltage changes across the transistor are all low percentages as compared to a more conventional MOSFET design. This slower percentage increase of voltage change could be an interesting property of IL FETs similar in design to the one explored here; it may allow many different types of future

applications in any case where it is desirable to have a more gradual response to stimuli, rather than a more immediate switching effect.

### **3.2 Manufacturing Considerations**

It should be noted that many of the properties observed in this investigation are likely to be unique to the manufacturing process used. As previously discussed, the distance across both the source-drain and gate-bias electrodes was a major design consideration that would be an interesting area for further experimentation. In addition to being of inherent interest in their own right, these distances, as well as the materials used to construct the electrodes and the method that was used to construct the circuits are all believed to significantly have affected the precision of the results. Specifically, the distance separating the gate and bias electrodes are believed to be a source of uncertainty in the results presented here. During the course of experimentation, the IL FET was rebuilt and tested multiple times in order to verify the precision of the results. The slight differences in fabrication caused considerable variation in the resulting data. Although multiple data points were not acquired for each half-volt increment of possible gate and source voltage levels as before, and thus an amount of data captured for these earlier trials was not as large as what was previously discussed in results, sufficient testing to ensure the precision of the device was obtained. Figure 13 shows the results of three initial builds, as well as the final build from which all prior data presented here has been taken.

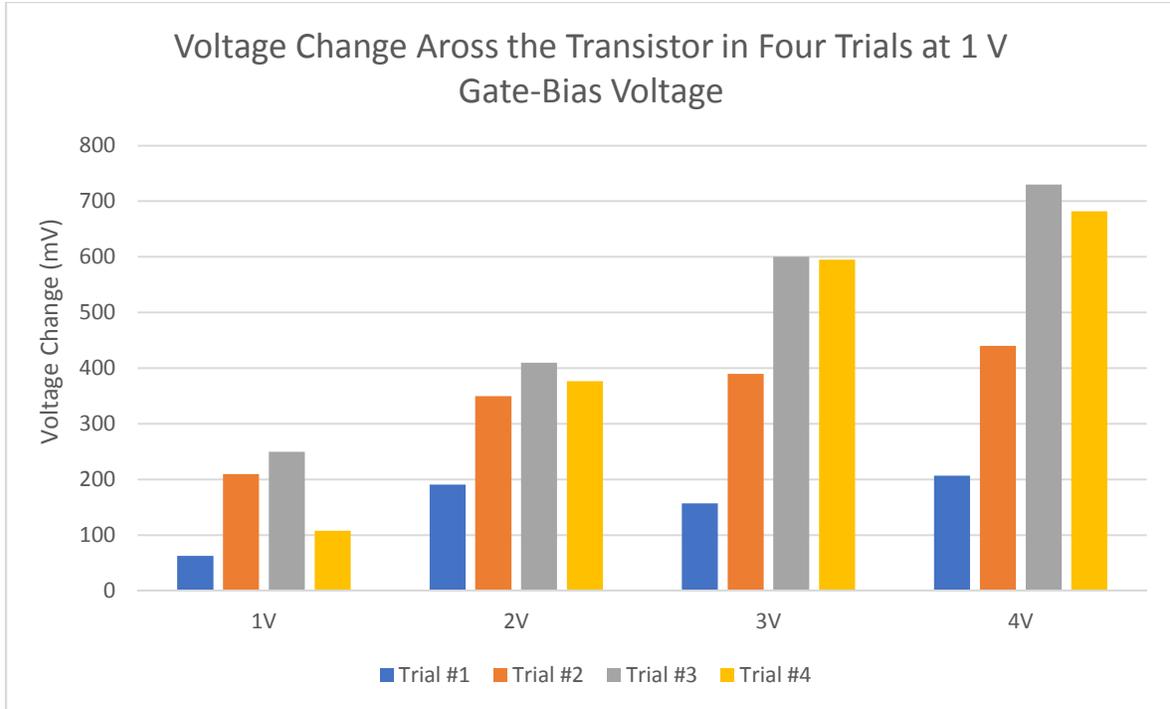


Figure 13 *Sample prior trial results taken at 1-volt gate-bias voltage. The results show net voltage change across the source-drain circuit. The trials are presented in chronological order.*

As can be seen in the above results, the transistor performance varied significantly across several of the trials. The exact positioning and location of the copper-foil electrodes used for the gate-bias circuit are believed to be the primary reason for the variance. The experimental procedure used maximized the precision of the placement of the copper to the greatest degree possible, but very small changes in its position, on the order of a tenth of a millimeter, were observed to cause significant changes in the transistor's performance. The possible variability in distance between the gate and bias electrodes in the first and second test likely made the depletion layer and carrier channel unstable and would have required higher gate voltage levels to achieve the same results as subsequent trials. The greater precision of the third and fourth trials, relative to each other, reflect improvements in the experimental process used to place and position the copper, but there is still much opportunity for improvements in the

manufacturing technique that could reduce variability in the design and allow for a higher precision device.

### **3.3 Concluding Remarks**

The concept of using an ionic liquid in a field-effect transistor has been shown to hold much promise by these results. One primary area for further study would include optimization of the distance between the various electrodes. By changing the overlapping distance between the source-drain electrodes and the interface of the ionic liquid, correspondingly larger depletion regions and carrier channels could theoretically be attained in the presence of higher gate voltages. This would allow more maximum current to flow between the source and drain electrodes. Additionally, experimenting with the distance between the gate electrode and the source-drain-ionic fluid interface would be interesting to investigate as it would potentially allow lower threshold voltages, opening up a wider range of potential applications for the transistor. Varying the type of ionic liquid used to change particle size and response time of the system would also be interesting, and any improvements in the manufacturing process to improve precision in electrode positioning would be very welcome. Ultimately, a future solid-state design of this work, taking into account the above considerations could allow the unique properties of such transistors to be capitalized on in a way that allows transistors to be used in many new and interesting ways never before conceived.

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**APPENDIX: EXPERIMENTAL DATA**

<b>Copper Circuit Voltage: 0.5 V</b>		
<b>Source Voltage (V)</b>	<b>Voltage Change (mV)</b>	<b>Standard Deviation</b>
0.5	125 ± 42.5	43.4
1	56.5 ± 37.8	38.6
1.5	127 ± 37.2	38.0
2	148 ± 23.2	23.7
2.5	257 ± 22.9	23.4
3	336 ± 40.0	40.9
3.5	419 ± 60.8	62.1
4	490 ± 45.9	46.8

<b>Copper Circuit Voltage: 1 V</b>		
<b>Source Voltage (V)</b>	<b>Voltage Change (mV)</b>	<b>Standard Deviation</b>
0.5	149 ± 26.6	27.2
1	108 ± 39.1	39.9
1.5	181 ± 23.9	24.5
2	377 ± 34.6	35.4
2.5	430 ± 30.9	31.6
3	595 ± 61.5	62.8
3.5	617 ± 55.5	56.7
4	682 ± 82.5	84.2

<b>Copper Circuit Voltage: 1.5 V</b>	
<b>Input Voltage (V)</b>	<b>Voltage Change (mV)</b>
0.5	144
1	162
1.5	233
2	341
2.5	462
3	592
3.5	611
4	730

<b>Copper Circuit Voltage: 2 V</b>	
<b>Input Voltage (V)</b>	<b>Voltage Change (mV)</b>
0.5	157
1	193
1.5	271
2	347
2.5	501
3	577
3.5	661
4	763

<b>Copper Circuit Voltage: 2.5 V</b>	
<b>Input Voltage (V)</b>	<b>Voltage Change (mV)</b>
0.5	217
1	228
1.5	336
2	413
2.5	588
3	657
3.5	729
4	841

<b>Copper Circuit Voltage: 3 V</b>	
<b>Input Voltage (V)</b>	<b>Voltage Change (mV)</b>
0.5	340
1	367
1.5	389
2	493
2.5	566
3	721
3.5	836
4	928

<b>Copper Circuit Voltage: 3.5 V</b>	
<b>Input Voltage (V)</b>	<b>Voltage Change (mV)</b>
0.5	364
1	608
1.5	633
2	662
2.5	742
3	891
3.5	1019
4	1171

<b>Copper Circuit Voltage: 4 V</b>	
<b>Input Voltage (V)</b>	<b>Voltage Change (mV)</b>
0.5	391
1	763
1.5	802
2	852
2.5	961
3	1037
3.5	1110
4	1207

<b>Voltage Change Across Transistor for Four Trials at 1V Gate Voltage</b>					
<b>Input Voltage (V)</b>	<b>Trial #1</b>	<b>Trial #2</b>	<b>Trial #3</b>	<b>Trial #4</b>	
1V	63	210	250	108	
2V	191	350	410	377	
3V	157	390	600	595	
4V	207	440	730	682	