Waveform generation in phase shift oscillators using harmonic programming techniques

Bharath Karthik Vasan
Iowa State University

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Waveform generation in phase shift oscillators using harmonic programming techniques

by

Bharath Karthik Vasan

A dissertation submitted to the graduate faculty
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

Major: Electrical Engineering

Program of Study Committee:
Randall Geiger, Major Professor
Degang Chen
Ayman Fayed
Sumit Chaudhary
Carl Bern

Iowa State University
Ames, Iowa
2013

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DEDICATION

This work is dedicated to my father, Mr. S. S. Vasan and
my mother, Mrs. Vyjayanthi Vasan.
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ABSTRACT

A novel harmonic management technique in Phase Shift Oscillators (PSO) is proposed. The technique can be used to generate multi-phase, square waves, low distortion sine waves or perform frequency multiplication or division for frequency synthesis. The technique involves weighted-summation of the PSO’s outputs to obtain an overall output that consists of the desired harmonics. A detailed derivation is provided that allows the user to choose the weights for the desired harmonic content. Robustness of the proposed technique is demonstrated using systematic analysis and simulations. In this work, the focus is on using the proposed technique to generate low distortion sine waves. A bread board prototype of a low distortion sine generator has been implemented using the proposed technique. The sine wave generator can generate -100dB Total Harmonic Distortion (THD) sine waves using extremely low cost discrete components. Simulations of on-chip sine wave generators implemented in a 0.13um CMOS technology process demonstrate using the proposed technique to generate -80dB THD sinusoids with large voltage swing.

The second part of the dissertation focuses on testing of Integral non-linearity (INL) of Analog-to-Digital Converters (ADC). The proposed algorithms reduce test cost associated with expensive hardware, and test cost associated with test time. Low cost voltage-shift generators that can enable testing of High resolution ADCs are investigated. It is shown that with the proposed shift generator and low linearity stimuli, INL of ADCs with resolution as high as 16-bit can be characterized.
The last part of the dissertation focuses on sensor interface circuits for soft elastomeric capacitors (SEC) for Structural Health Monitoring (SHM) applications. Each SEC is a flexible strain gauge, transducing a change in strain into a change in capacitance. The proposed measurement method relies on the differential measurement technique. A prototype of the proposed technique has been built to demonstrate the working under controlled strains. The circuit has a voltage sensitivity to strain of 23mV/με.
CHAPTER 1

GENERAL OVERVIEW

The dissertation focuses on three distinct topics, waveform generation using phase shift oscillators (Chapter 2), algorithms to lower test cost in linearity testing of Analog-to-Digital Converters (Chapter 3-5) and low-cost interface circuits for novel soft elastomeric capacitors (Chapter 6). The title chosen for the dissertation reflects the research in chapter 2, and is not related to chapters 3-6.

1.1 Waveform generation using phase shift oscillators

An integral part of many modern electronic systems is a waveform generator. Oscillators are often used to implement a waveform generator. An engineer, designing oscillators for Test and Measurement applications, communication systems or digital systems is faced with the challenge of optimizing the performance of the oscillator for the application. Key oscillator specifications in many applications are frequency accuracy and stability, noise, tuning behavior and harmonic distortion. Extensive research has been carried out to optimize an oscillator for the first three specifications. Effects of harmonic distortion are most commonly suppressed using a filter. To achieve sufficient suppression high Q, narrow-band filters are deployed in such systems.

The last few decades have witnessed rapid advances in CMOS Integrated Circuit (IC) technology and explosive growth in the fields of wireless communication and consumer electronics. The trend is expected to continue with more functionalities being brought together on to a single chip. Multi-standard wireless systems like fully
integrated wireless transceivers, Production Testing and Built-in-Self Test (BIST) of ICs, etc. are systems in which harmonic distortion performance of oscillators is critical. In many applications, Local Oscillator (LO) harmonics or signal generator’s harmonics have to be attenuated by over 60dB relative to the fundamental and this level of harmonic attenuation is viewed as a challenging task. Filters are often used to obtain this or higher levels of harmonic suppression. Although filters can provide harmonic suppression, the design of these filters is often challenging, they often include discrete components, and the resulting filters are often large and expensive. In many applications there is considerable pressure placed on designers to eliminate discrete components in the filters to allow complete monolithic integration of the system and to reduce the size and complexity of the filters if they are integrated. Recently methods have been introduced to suppress harmonics in sinusoidal signal generators by strategically summing multi-phase and multi-frequency externally generated square waves [1] or by using polyphase, multipath techniques [2].

In this dissertation the primary focus is on developing methods for periodic signal generation with controllable spectral characteristics by assembling or programming the harmonics components in an oscillator system. Though the periodic waveforms can be assembled to have rather rich spectral components, emphasis will be placed on periodic waveforms that are ideally sinusoidal. The oscillator system is developed around a Phase Shift Oscillator (PSO). In this work, it will be assumed that the PSOs of interest are ideally comprised of a cascade of identical blocks connected in a feedback loop. Alternatively, the PSO loops could be viewed as ring oscillators. The
PSO loops encompass rings with resonator-less stages and multiphase LC oscillators though many different types of blocks can be used to implement the PSO. The PSO is widely used to generate multiphase LO signals in the RF/Microwave field [4].

Following the introduction of Chapter 1, methods to control harmonic-distortion in oscillators are reviewed in Chapter 2. The crux of this work, programming of harmonics in PSO, is introduced in Chapter 2. With the harmonic programming method, the outputs of each stage of the PSO or a subset of the PSO outputs are weighted and summed to provide the overall output. The weights of the individual PSO outputs depend on the desired harmonics at the output. This proposed method is used to generate low distortion sine waves for Device-Interface-Boards (DIB) applications and Built-in-Self-Test applications (BIST). Using the proposed technique for multiphase signal generation frequency synthesis is also discussed.

1.2 Algorithms to reduce test-cost in linearity testing of ADCs

Linearity testing of high volume products like Analog-to-Digital Converters (ADC) is a challenging task requiring novel solutions. Recently, methods were introduced to test high resolution ADCs with low linearity ramps or sine waves [5]. In chapter 3, signal conditioning algorithms are proposed that extend the working of these algorithms to any low linearity monotonic signal. In chapter 3, an algorithm to reduce the test cost along with hardware cost is proposed. In chapter 4, Kalman Filter is included with the algorithm proposed in chapter 3 to obtain accurate estimates of the
INL of the ADC in the presence of noise. In chapter 5, low cost signal generators are proposed to generate low linearity signals to test high resolution ADCs.

1.3 Low-cost interface circuits for novel soft elastomeric capacitors

Several sensing systems have been developed over the last decade for Structural Health Monitoring (SHM) of wind turbine blades, and some have shown promise at damage detection. However, there exist yet several challenges in establishing links between sensor signal, damage state (diagnosis), and residual life (prognosis) of a wind turbine blade. In order to create a complete SHM system capable of damage diagnosis, localization, and prognosis for wind turbine blades, the authors propose a novel sensing method capable of distributed sensing [6]. The sensor is a flexible membrane composed of several soft capacitors arranged in a matrix, with the advantages of being robust, easy to install, inexpensive, capable of covering large surfaces, and involves relatively simple signal processing. By measuring changes in capacitance, it is possible to determine local strains on a structural member at pre-defined levels of precisions. Electronic interfaces for the SEC considered for this application are investigated in chapter 6. Existing data measurement methods for dense networks of sensors are limited, because of issues related to reliability, cost, resolution, noise, and data capture rate. The proposed measurement method relies on the differential measurement technique. The circuitry consists of two channels, one for the sensor and one for the reference, each of these acting as a low pass filter. Experimental results are provided for a low cost prototype that has been built to demonstrate the working under controlled strains.
I, Bharath Karthik Vasan, am the primary investigator in works presented in chapter 2-5 with the guidance of my advisor, Dr. Randall Geiger and Professor Dr. Degang Chen. In the work presented in chapter 6, I am a co-investigator.

References


CHAPTER 2

WAVEFORM GENERATION IN PHASE SHIFT OSCILLATORS USING HARMONIC PROGRAMMING TECHNIQUES

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Bharath K Vasan, Siva K Sudani, Randall Geiger and Degang Chen

Abstract

In this work, a novel technique is proposed to generate waveforms by summing and weighting some or all of the individual outputs of a Phase Shift Oscillator (PSO). This technique involves programming the harmonic content of the waveforms for various applications like test and measurement, calibration, radio frequency synthesis, frequency division, and Built-In-Self Test (BIST). By choosing the weights appropriately, multi-phase, low distortion sinusoidal signals can be produced. Alternatively, spectrally rich non-sinusoidal signals can be generated with this approach. Yet other combinations of the weights can be used to create a frequency multiplier operating at a frequency that is higher than the fundamental frequency of the PSO.

In this work, the key focus will be on using this technique to generate low distortion sinusoidal waveforms. Using the proposed method to generate sinusoidal signals, all harmonics from the 2nd up to N-2th will be absent when generated with an N-stage PSO.

Operations like frequency multiplication and frequency division are also described. Robustness of the method is demonstrated with statistical analysis and Monte-
Carlo simulations. Simulation results using commercial operational amplifier SPICE models are presented to demonstrate low distortion sine wave generation over the 2kHz~180kHz frequency range. Simulation results for on-chip low distortion sinusoidal generators are also presented.

Robustness of the method has also been experimentally verified with a sinusoidal signal generator implemented with low-cost low-performance discrete components. 3-stage and 4-stage PSOs constructed on a bread board were used to generate low distortion sinusoidal signals with a p-p output of 7V, an operating frequency of 1.5kHz and THD of -101.45 dB using off-the-shelf passive components without any attempts to either trim or match any of the discrete components.

2.1 Introduction

Existing approaches to parametric testing of Integrated Circuits (IC)[1] typically incorporate a stimulus that is spectrally pure or highly linear. This approach is invariably used in expensive high-end Automated-Test-Equipment (ATE) [2] used for testing integrated circuits used in high speed communications, medical electronics, consumer electronics, avionics, etc. Maintaining analog test signal integrity is an extremely challenging task in testing a wide variety of high performance AMS circuits. In most testing environments, the stimulus generated in the tester used for AMS testing has to not only be more pure than the Device-Under-Test (DUT) but also be delivered from the test head to the DUT without degrading its performance [3-5]. Many of the modern complex, System-On-Chips (SOCs) incorporate analog blocks that are deeply embedded in the ICs. Accessing these blocks for testing is either nearly impossible or
compromises the testing signal integrity. For standalone ICs where the signal input pins are externally accessible, one way to reduce the test signal delivery problem is to place test signal generation circuits [5] on the Device Interface Boards (DIB) close to DUT to reduce the distance between the input to the DUT and the location where the test signal is generated. In SOCs, the distance can be even further reduced if the signal generator is moved on-chip thereby providing a Built-in-Self-Test (BIST) solution.

For example, the standard approach for spectral testing of a high performance 15-bit ADC that may have a THD specification of -90dB would require a sinusoidal test signal with a THD of at least -100dB at a voltage swing that covers the entire input range of the ADC. Generating such spectrally pure sine waves is a challenging task for both DIB and on-chip applications. Due to space limitations when using existing sine wave generation circuits, DIB spectral testing solutions are typically restricted to testing at a single frequency [6]. The limited results reported by designers of on-chip sine signal generators are mostly for operation at higher frequencies with programmability, but designers are yet to achieve THD lower than -72dB at reasonable signal swings [7-8].

The proposed technique is used to design practical low cost sinusoidal signal generators for both DIB based solutions and BIST solutions. It provides a method for generating low distortion sine waves at large signal swings that can be easily programmed to operate over a wide frequency range.

Many Radio Frequency (RF) multi-standard systems like Cognitive Radios, Software Defined Radios and TV Tuners are tending towards complete silicon integration. Local oscillator signals that are used in such systems are often square waves
that provide for high Mixer Gain and good noise performance [9]. Harmonics of the square waves interact with the base band signals in the transmitters and RF signals in the receivers [9-11] producing undesired frequency components. This can be seen by considering the wideband receiver shown in Figure 2.1. In the figure, the desired band denoted by ‘D’ in blue, is to be down-converted to IF by using the LO. The LO is operating at a fundamental frequency of $f_{LO}$. The harmonics of the LO, down-convert undesired components to baseband. The figure shows the effects of the second and the third harmonics of the LO. But harmonics as high as the tenth, could down-convert undesired signals to the band of interest. A typical TV Tuner receiver system operates over the wide range of 48 MHz ~ 860 MHz.

![Figure 2.1 LO Harmonics in Wideband Receivers](image)

Figure 2.1 LO Harmonics in Wideband Receivers
The undesired components could constitute adjacent TV bands or frequencies as high as those for the carriers for GSM, WiFi standards [12].

A common solution to the distortion problem in sine wave generation circuits is to use tuned filters designed with discrete components to suppress the undesired frequency components [11]. Suppression as high as 60dBc is commonly required for suppressing the harmonics in a periodic signal generated with standard sine wave oscillators. For discrete applications, the tuned filter approach is bulky and often not cost effective. For integrated applications, the tuned filter approach is often completely impractical. Harmonic Rejection Mixers (HRM) in transmitters and receivers are used to alleviate this problem. HRM use known phase relationships between the fundamental and harmonics in a square wave to suppress harmonics. In all HRM schemes described [11-13] power hungry frequency dividers are used to generate the multiphase signals. The harmonic rejection achievable is limited by mismatch in devices. In this work, PSOs are used to generate the multiphase signals for HRM.

Frequency dividers or pre-scalers are critical blocks in frequency synthesizers and phase locked loops. A significant amount of the total power budget is consumed by these blocks in the synthesizer. A well-known strategy to mitigate the power consumption in such systems is to use a Multiply-by-N Ring Oscillator or Injection Locked Frequency Dividers (ILFD) [14]. Frequency generation using PSOs and the proposed method is discussed in this work.

The rest of the paper is arranged as follows. In Section 2.2, harmonic distortion control in conventional sine wave generators and Direct Digital Synthesizers (DDS) is
discussed. The current state-of-art in harmonic cancellation is also discussed. In Section 2.3, a PSO with a novel harmonic programming method is proposed. In Section 2.4, the factors that affect performance of the proposed method are discussed. In Section 2.5, a circuit implementation is proposed followed by simulation results for discrete implementations in Section 2.6. Experimental results are presented in section 2.7. Simulation results for an on-chip implementation of low THD sine wave generator are presented in section 2.8. The chapter is concluded in Section 2.9.

2.2 Harmonic Distortion Control in Sine Wave Generators

Conventional approaches of generating sinusoidal signals are dominantly based on using either an ideally sinusoidal oscillator or DDS. With DDS, a digital waveform generator comprised of a Digital-to-Analog Converter (DAC) and an output filter is used to generate the sinusoidal signal.

The oscillator-based circuits are often comprised of an amplifier with non-linear gain control and a linear frequency selective feedback network as shown in Figure 2.2(a). The frequency selective network is often passive but can include amplifiers as well. An example of an oscillator with a second-order series/parallel RC feedback network as the frequency selective network is the highly popular Wien Bridge oscillator. If the frequency selective network is comprised of a cascade of delay stages, the oscillator is often termed a phase-shift oscillator [15-17]. With this approach, the circuit is designed so that it ideally has a single pair of complex conjugate poles on the imaginary axis with all remaining poles of the system lying far in the left half-plane.
This pair of poles will be referred to in this work as the critical pole pair. From a practical viewpoint, the critical pole pair is placed slightly into the right half plane and inherent nonlinearities are used to limit the amplitude of the signal at the output of the oscillator. If for any reason the critical poles were to move into the LHP, oscillation would cease. The amplifier is often designed so that at small signal amplitudes the poles of the oscillator are guaranteed to lie in the RHP but at large signal amplitudes the poles of the oscillator are guaranteed to lie in the LHP. A nonlinear transfer characteristic of the amplifier is used to achieve this pole movement with signal amplitude.

With the oscillator approach, much of the effort on improving the spectral performance is on controlling the location of the critical poles by controlling both the gain and nonlinearity [15-17] of the amplifier. Generally, spectral performance is improved as the critical poles are moved closer to the imaginary axis. But movement of the poles closer to the imaginary axis results in a decrease in the magnitude of the output voltage. An abrupt saturation (or nonlinearity) of the amplifier that reduces the gain at higher amplitudes results in significant distortion whereas more gradual gain reduction with signal amplitude improves spectral purity [15]. A closely related class of sinusoidal oscillator circuits is the bandpass-based oscillators. The bandpass-based oscillator structures [8], [17] rely on precisely controlling the value of the critical pole-pair quality factor, often-termed the pole ‘Q’, to obtain spectrally pure signals. The Output Filter in Figure 2.2 (a) is used to attenuate residual harmonics that are present in the output of the oscillator and further improve the spectral performance of the output signal.
With the DDS approach, a digital representation of the sine wave is stored in a Look-Up Table (LUT). Sequential addressing of the LUT generates a Boolean sinusoidal waveform at the output of the LUT. This sinusoidal Boolean signal is applied to the input of the DAC. The output of the DAC serves as the analog sinusoidal signal. The DAC output is generally filtered with a continuous-time analog filter to reduce high-frequency spectral components.

![Block diagram (a): Conventional Oscillator (b): Conventional DDS](image)

Figure 2.2 Block diagram (a): Conventional Oscillator (b): Conventional DDS

The DDS approach is shown in Figure 2.2(b). Spectral improvement is typically done by measuring the unwanted spurs in the analog output spectrum and pre-distorting...
the input sequence stored in the LUT to cancel or reduce the unwanted spurs at the DAC’s output. Techniques proposed for the pre-distortion involve measuring the amplitude and phase [18-19] or only the amplitude [20] of the harmonic components for generating the DAC pre-distortion codes. One of the limitations with this approach is that the device measuring the amplitude and phase of harmonics of the DACs has to be very accurate over a wide range of frequencies. Another limitation is that the DAC is required to have sufficient resolution to correct for the small harmonics measured at the DAC’s output. In [20], authors model the non-linearity of the DAC using a 3rd order polynomial. Only the amplitude of harmonics is measured and phase information is obtained from the model. The method requires an accurate measuring device and is not robust at high frequencies. In [21], a filter is used to attenuate higher frequency components. The filter’s transfer function is determined by the bandwidth of signal and the desired level of attenuation of out-of-band quantization noise. A low jitter clock is mandatory to obtain high dynamic range. In [22], the authors propose a method for sampling the LUT with multiple interleaved phases to push harmonics out-of-band. The method requires a filter to attenuate out-of-band frequency components.

Harmonic cancellation is a well-known concept used in polyphase networks [23-24]. In [7], [11-12], [25], the authors exploit the relationship between the fundamental and the harmonics of a square wave for harmonic cancellation, and generate sine waves. Although square waves are digital friendly, they inherently have high harmonic content. Mismatch in rise/fall times of the square waves, incomplete settling, variations in the maximum and minimum values of the square wave, and mismatch in components
carrying out harmonic cancellation limit the effectiveness of approach in [7]. High ‘Q’ requirements of the filter add to the limitations in [25].

The proposed technique can also be used for harmonic cancellation. In a PSO designed for sinusoid generation, a simple, low cost, scheme provides amplitude stabilization. By controlling the location of the poles, sine waves at each stage’s output with modest THD are produced. The output of each stage is weighted and summed to produce low distortion sine waves. By starting with modest THD sine waves, the proposed harmonic cancellation technique is more robust to mismatch than the techniques proposed in [7], [12] and [25].

2.3 Proposed Method

In this section, a PSO is described followed by the proposed method of weighted summation of the PSO’s outputs. Tables describing harmonics that can be eliminated with an N-stage PSO, and the corresponding weights to be used, are presented.
Following this, generation of multiple outputs, with low distortion and precise phase difference, are described.

### 2.3.1 Phase Shift Oscillator

Consider an N-stage phase-shift oscillator as shown in Figure 2.3. In its simplest form, each stage is a first order integrator with a transfer function $T(s)$ and an amplitude limiting function, $f(A)$. If the stages are identical, the outputs are all time delayed versions of the output of the first stage, $X_{01}$. For identical stages, the outputs can be expressed as:

$$X_{0i}(t) = X_{01}\left(t - (i-1)\frac{T}{N}\right)$$  \hfill (1)

where $N$ is the number of stages, $T$ is the period of oscillation and $X_{01}$ is the $i^{th}$ stage output. The output waveforms are all plagued by harmonic distortion (HD). $X_{01}$ can be represented by expressing the outputs using exponential Fourier series as:

$$X_{01}(t) = \sum_{k=-\infty}^{\infty} A_k \exp\left[jk\frac{2\pi}{T}t\right]$$  \hfill (2)

where $A_k$ is $k^{th}$ harmonic’s Fourier coefficient. As the stages are identical it follows that:

$$X_{0i}(t) = \sum_{k=-\infty}^{\infty} A_k \exp\left[-j\frac{2\pi}{N}(i-1)k\right] \exp\left[jk\frac{2\pi}{T}t\right]$$  \hfill (3)

(3) is an important equation that describes the phase shift of various harmonic components at $i^{th}$ stage’s output in the PSO. The phase relationship can be written as:
\[ \Theta_{i,k} = \phi_k - \frac{2\pi}{N} (i-1)k \quad (4) \]

where \( \phi_k = \angle A_k \) and \( \Theta_{i,k} \) is the phase of the k-th harmonic in the i-th stage’s output. The condition for oscillation requires that, at the frequency of oscillation, the total phase shift across all stages in a PSO to sum to zero, and the loop gain to be unity. It has been observed that this condition has to hold good not only at the fundamental frequency of oscillation but also at all the harmonics. This forces the phase relationship described by (4). This important property of the PSO is used in the following sections to program and cancel harmonics.

### 2.3.2 Weighted Summation of PSO Outputs

The proposed method the weighted sum of the outputs of the PSO is computed to cancel HD terms. The below equation describes the operation shown in Fig. 2.4:

\[ Y(t) = \sum_{i=1}^{N} \lambda_i X_{O_i}(t) \quad (5) \]

where \( Y(t) \) is the weighted sum and the real number \( \lambda_i \) is the weight of the output \( X_{O_i} \). \( Y(t) \) can be expressed as a complex scaled version of the complex Fourier series of \( X_{01}(t) \) where the k-th harmonic is scaled by a complex factor \( \beta_k \):

\[ Y(t) = \sum_{k=-\infty}^{\infty} \beta_k A_k \exp\left[ jk \frac{2\pi}{T} t \right] \quad (6) \]

In this expression, \( \beta_k \) is the complex conjugate of \( \beta_{-k} \). The value of \( \beta_k \) for \(-\infty < k < \infty\) is specified by the user to define the desired spectral content in \( Y(t) \). The weights \( \lambda_i \) need to be determined to achieve the specified value of \( \beta_k \). Since the weights in the
circuit of Fig. 2.4 are real, there are some restrictions on the values of $\beta_k$ that can be specified. Also, since there are only $N$ weights, and since there are an infinite number of $\beta_k$ values, some additional restrictions are placed on the values of $\beta_k$.

A major emphasis in this work is in the creation of sinusoidal waveforms with low distortion which will be achieved if the harmonic terms in $Y(t)$ are small or even absent. To create an output $Y(t)$ that is void of the $k^{th}$ harmonic, $\beta_k$ (and thus $\beta_k$ too) would be set to zero.

Substituting (3) in (5) and interchanging summation signs the following is obtained:

\[
Y(t) = \sum_{k=-\infty}^{\infty} A_k \sum_{i=1}^{N} \lambda_i \exp\left[-j \frac{2\pi}{N} (i-1)k \right] \exp\left[jk \frac{2\pi}{T} t \right]
\]  

(7)

Figure 2.4 N-stage Phase Shift Oscillator with Weighted Summation of Outputs
Comparing (6) and (7) the following relationship between the weights and the distortion, for $-\infty < k < \infty$, is obtained:

$$\sum_{i=1}^{N} \lambda_i \exp \left[ -j \frac{2\pi}{N} (i-1)k \right] = \beta_k$$

(8)

Corresponding to these harmonics are the $2N-1$ equations in (8) associated with the index terms $-N+1 < k < N-1$. Consider the subset of these $2N-1$ equations corresponding to index terms $k=0, 1\ldots N-1$. From equation, (8), the relationship between the weights and the complex coefficients can be expressed in matrix form as:

$$V.W = Z$$

(9)

$$W = [\lambda_1 \lambda_2 \ldots \lambda_N]^T$$

$$Z = [\beta_0 \beta_1 \ldots \beta_{N-1}]^T$$

(10)

$$V = \begin{bmatrix}
1 & 1 & \ldots & 1 \\
1 & \Omega & \ldots & \Omega^{N-1} \\
1 & \Omega^2 & \ldots & \Omega^{2(N-1)} \\
1 & \Omega^3 & \ldots & \Omega^{3(N-1)} \\
\vdots & \vdots & \ddots & \vdots \\
1 & \Omega^{N-1} & \ldots & \Omega^{(N-1)(N-1)}
\end{bmatrix}$$

(11)

where $\Omega = \exp \left[ -j \frac{2\pi}{N} \right]$. In this expression $\Omega$ is the primitive N-th root of unity. The matrix, $V$, is a Discrete Fourier Transform (DFT) matrix that operates on the sequence represented by the $W$ matrix to produce DFT coefficients matrix, $Z$ [26]. Thus:

$$W \xrightarrow{DFT} Z$$

(12)

Since we have considered only $N$ equations from (8), the matrix $V$ is square. It is also invertible. The weight of the $i^{th}$ output of the PSO, $X_{Oi}$, can be obtained by multiplying
the left and right sides of (9) by the inverse of the matrix \( V \). It thus follows after some routine calculations that the weights can be expressed in terms of the distortion parameters as:

\[
\lambda_i = \frac{1}{N} \sum_{m=0}^{N-1} \beta_m \Omega^{-(i-1)m}
\]  

(13)

Since \( \beta_k \) is a complex number, \( \lambda_i \) obtained from (13) may be a complex weight. Complex weights cannot be realized with the system modeled by the block diagram of Fig. 2.4. In this work the proposed method is described for real weights, which can be easily realized using passive components or relative sizing of active devices. All the properties of DFT hold good for the DFT pair \((W, Z)\). Of particular relevance are the properties of conjugate symmetry and periodicity. The property of conjugate symmetry is considered first and provides necessary and sufficient criteria for obtaining a real weight vector \( Z \).

The vector \( Z \) is conjugate symmetric if

\[
\hat{\beta}_k = \hat{\beta}_{N-k}
\]

(14)

for \( k=1,2 \ldots N-1 \) where the notation \( \hat{\beta}_{N-k} \) denotes the complex conjugate of \( \beta_{N-k} \).

It can be shown that if the vector \( Z \) is conjugate symmetric, then the weights given by (13) are all real.

By restricting the weights to satisfy (14), equation (8) will be satisfied for \( k=1,2 \ldots N-1 \). But (8) must be satisfied for all \(-\infty < k < \infty\). It can be shown that if the \( \beta \) sequence is periodic with period \( N \), then (8) will be satisfied for all \( k \). This periodicity property can be expressed as

\[
\beta_{k+N} = \beta_k \quad t = 0,1,2,\ldots
\]

(15)
Summarizing, equations (14) and (15) give conditions for the Z sequence that will guarantee real weights.

The implications of the periodicity constraint can be illustrated with a simple example. For example, in a 5-stage PSO, N=5, so the scaling for the second harmonic, k=2, is the same as the scaling for the seventh harmonic, k=2+5. Correspondingly, the scaling for the third harmonic, k=3, is the same as the scaling for the eighth harmonic, k=3+5, and so on.

2.3.3 Low Distortion Sine Wave Generation

To generate a pure sine wave, the energy at all harmonics but the fundamental should be zero. With the architecture of Fig. 2.4, it follows that the waveform Y(t) will be void of the k\(^{\text{th}}\) harmonic if the corresponding $\beta_k$ vanishes. A low distortion sinusoidal waveform can be generated by judiciously choosing the weights so that the corresponding $\beta_k A_k$ are sufficiently small.

Using the complex conjugate property required to obtain real weights, the following relations can be written. For the fundamental the following expression holds:

$$\beta_1 = \hat{\beta}_{N-1}$$

(16)

For the harmonic distortion components, k=2, 3…N-2:

$$\beta_2 = \hat{\beta}_{N-2}$$

$$\beta_3 = \hat{\beta}_{N-3}$$

$$\vdots$$

(17)
And, for the dc component:

$$\beta_0 = \beta_N$$

(18)

From (16), (17) and (18) it can be observed that for $W$ to be real the only condition imposed on the fundamental is that scaling factor of the fundamental should be equal to the complex conjugate of the scaling factor of $N-1^{th}$ harmonic. The condition on the dc component and the other harmonic components are independent of that of the fundamental. Thus they can be set to zero independently, to leave the fundamental and $N-1^{th}$ harmonic component scaled by the same magnitude. The higher harmonics corresponding to the fundamental and $N-1^{th}$ harmonic as dictated by the periodicity property are also scaled by the same magnitude. This is described by the following equation:

$$\beta_k = \begin{cases} 
P\exp[-j\phi], & k=1+N.t \\
P\exp[j\phi], & k=N-1+N.t \\
0, & \text{otherwise}
\end{cases} \quad t = 0,1,2...$$

(19)

where $P$ is the desired magnitude scaling of the fundamental and $\phi$ is the desired phase of the fundamental. Thus with a $N$-stage PSO and weighted summation of the outputs given by (19), the output will be void of harmonic distortion components up to the $N-2^{th}$. The weights are real and are given by inverse DFT operation on the DFT coefficients vector chosen according to (13). Table 2.1 describes the harmonics that can be eliminated using the proposed method by setting a maximum number of the $\beta_k$ coefficients to 0 for PSOs with $N=3$ to $N=10$. In this table, the voided harmonics are
identified for harmonics up to the 12\textsuperscript{th}. The table can be easily extended to include higher harmonics.

For the calculation of weights, consider the situation where $P=1$, $\phi=0$ in (19). The weights are then calculated using (13). For $N=3$ to $N=10$ stages, the weights on each output to cancel the harmonics described in Table 2.1 are tabulated in Table 2.2. Implementing these weights using circuit components will result in incomplete voiding of spectral components due to variations in the values of the circuit components though the residual harmonic terms can be very small for a good circuit design. In Section 2.4 implementation of the weights along with the effects of non-idealities are discussed. Fully differential, N-stage PSOs can be interpreted as a single ended 2N stage PSOs and the results obtained in Table 2.1 and Table 2.2 can be directly applied.

**Table 2.1 Harmonic Cancellation for N-stage PSO using proposed method**

<table>
<thead>
<tr>
<th></th>
<th>Number of stages</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>3</td>
</tr>
<tr>
<td>DC Component</td>
<td>X</td>
</tr>
<tr>
<td>Fundamental</td>
<td>✓</td>
</tr>
<tr>
<td>2\textsuperscript{nd} Harmonic</td>
<td>✓</td>
</tr>
<tr>
<td>3\textsuperscript{rd} Harmonic</td>
<td>X</td>
</tr>
<tr>
<td>4\textsuperscript{th} Harmonic</td>
<td>✓</td>
</tr>
<tr>
<td>5\textsuperscript{th} Harmonic</td>
<td>✓</td>
</tr>
<tr>
<td>6\textsuperscript{th} Harmonic</td>
<td>X</td>
</tr>
<tr>
<td>7\textsuperscript{th} Harmonic</td>
<td>✓</td>
</tr>
<tr>
<td>8\textsuperscript{th} Harmonic</td>
<td>✓</td>
</tr>
<tr>
<td>9\textsuperscript{th} Harmonic</td>
<td>X</td>
</tr>
<tr>
<td>10\textsuperscript{th} Harmonic</td>
<td>✓</td>
</tr>
<tr>
<td>11\textsuperscript{th} Harmonic</td>
<td>✓</td>
</tr>
<tr>
<td>12\textsuperscript{th} Harmonic</td>
<td>X</td>
</tr>
</tbody>
</table>

**X**: Harmonic Cancelled, **✓**: Harmonic Not affected
Table 2.2 Weights for Harmonic Cancellation in an N-stage

<table>
<thead>
<tr>
<th>Number of stages</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\lambda_1)</td>
<td>0.667</td>
<td>0.500</td>
<td>0.400</td>
<td>0.333</td>
<td>0.286</td>
<td>0.250</td>
<td>0.222</td>
<td>0.200</td>
</tr>
<tr>
<td>(\lambda_2)</td>
<td>-0.333</td>
<td>0.000</td>
<td>0.124</td>
<td>0.167</td>
<td>0.178</td>
<td>0.177</td>
<td>0.170</td>
<td>0.162</td>
</tr>
<tr>
<td>(\lambda_3)</td>
<td>-0.333</td>
<td>-0.500</td>
<td>-0.324</td>
<td>-0.167</td>
<td>-0.064</td>
<td>0.000</td>
<td>0.039</td>
<td>0.062</td>
</tr>
<tr>
<td>(\lambda_4)</td>
<td>na</td>
<td>0.000</td>
<td>-0.324</td>
<td>-0.333</td>
<td>-0.257</td>
<td>-0.177</td>
<td>-0.111</td>
<td>-0.062</td>
</tr>
<tr>
<td>(\lambda_5)</td>
<td>na</td>
<td>na</td>
<td>0.124</td>
<td>-0.167</td>
<td>-0.257</td>
<td>-0.250</td>
<td>-0.209</td>
<td>-0.162</td>
</tr>
<tr>
<td>(\lambda_6)</td>
<td>na</td>
<td>na</td>
<td>na</td>
<td>0.167</td>
<td>-0.064</td>
<td>-0.177</td>
<td>-0.209</td>
<td>-0.200</td>
</tr>
<tr>
<td>(\lambda_7)</td>
<td>na</td>
<td>na</td>
<td>na</td>
<td>na</td>
<td>na</td>
<td>0.178</td>
<td>0.000</td>
<td>-0.111</td>
</tr>
<tr>
<td>(\lambda_8)</td>
<td>na</td>
<td>na</td>
<td>na</td>
<td>na</td>
<td>na</td>
<td>na</td>
<td>0.177</td>
<td>0.039</td>
</tr>
<tr>
<td>(\lambda_9)</td>
<td>na</td>
<td>na</td>
<td>na</td>
<td>na</td>
<td>na</td>
<td>na</td>
<td>na</td>
<td>0.170</td>
</tr>
<tr>
<td>(\lambda_{10})</td>
<td>na</td>
<td>na</td>
<td>na</td>
<td>na</td>
<td>na</td>
<td>na</td>
<td>na</td>
<td>na</td>
</tr>
</tbody>
</table>

na: not applicable

Figure 2.5 Multi-phase low distortion sine wave generation
2.3.4 Multiphase Low Distortion Sine Wave Generation

Many applications require multiple sinusoidal signals with a precise phase relationship [11-13], [27-28]. If the PSO stages are ideal, multiple sets of weights and summing devices can be used to generate multiple sine waves with low distortion and a particular phase relationship. Figure 2.5 describes the concept of using multiple weighted summation blocks. (19) is modified to:

\[
\beta_{w,k} = \begin{cases} 
P_{w,\exp}[-j\phi_w], & k = 1 + N.t \\
P_{w,\exp}[j\phi_w], & k = k-1 + N.t \\
0, & \text{otherwise}
\end{cases}
\]

where \(w=1,2,3\ldots M\) is the index of the \(w^{th}\) weighted summation block and \(M\) is the number of weighted summation blocks. The desired phase relationship between different blocks can be set by appropriately choosing \(\phi_w\).

2.3.5 Multiphase Signal Generation for Harmonic Rejection Mixing

In all HRM schemes described [11-13] power hungry frequency dividers are used to generate the multiphase signals. In Section 2.3.3 it has been shown that with a 4-stage fully differential PSO harmonics up-to 6\(^{th}\) can be cancelled. Certain higher harmonics like 11\(^{th}\), 13\(^{th}\), 19\(^{th}\), 21\(^{th}\), and so on are also suppressed. By starting with lower harmonics in PSO, the energy in the harmonics can be suppressed to lower levels with the proposed method. The PSO can be used to generate the multiple phases to be used with HRM to enable complete integration of the wideband architecture. PSO’s could offer the following benefits
(a) Wave shaping to generate square waves/quasi-sine waves thereby decreasing the overall harmonic content.

(b) Power optimization when used with an Injection Locking Scheme[30]

An implementation of the HRM mixer with proposed PSO is shown in Figure 2.6. The weighted summation is performed in the Mixer with weights assigned to the tail current sources. A cascade of PSOs can be used as described in [29].

2.3.6 Frequency Generation for Frequency Division/Multipliers

It has been shown in Section 2.3.3 that using the proposed harmonic programming scheme, higher harmonics can be extracted. Consider the following example of a 3-stage PSO (N=3).

Figure 2.6 PSO for Harmonic Rejection Mixing
From (16), (17) and (19), it can be seen that to extract the third harmonic and its multiples we can set:

\[ \beta_1 = \beta_2 = 0 \]

\[ \beta_0 = 1 \]

Using (13) we can obtain the weights as:

\[ \lambda_1 = \lambda_2 = \lambda_3 = \frac{1}{3} \]

The weights from (23) extract the third harmonic and its multiples from a 3-stage PSO. The fifth harmonics and its multiples can be extracted from a 5-stage PSO. Selective frequencies can also be extracted using the proposed technique as described in (16), (17) and (18). This would enable both power efficient frequency divider design and frequency multipliers for high frequency generation. Injection locking schemes can be accommodated with the proposed method for frequency division [29-30]

### 2.4 Performance Limitations

The harmonic cancellation is exact as shown in Table 2.1 only when the weights are precisely as given by (13), the PSO stages are perfectly matched, and the summing device is linear. Real circuits are plagued by mismatch and non-idealities. This would affect the degree of suppression of the harmonics with the proposed method. The factors that affect harmonic suppression can be broadly classified into non-idealities in the PSO and non-idealities in the summing network.
2.4.1 Non-idealities in PSO

The individual delay stages in the PSO shown in Fig. 2.3 are ideally identical and if nonlinearities are ignored, they are characterized by a transfer function $T(s)$. In a real circuit, the passive and active devices used to implement $T(s)$ will vary from one PSO stage to another due to inherent mismatch present in real components. In a typical PSO stage, this mismatch will occur in the components used to implement the DC gain as well as the poles and zeros of $T(s)$. There will also be mismatch in the amplitude stabilization function in each stage. In an ideal PSO, the output of each stage has identical spectral components with a fixed time-delay in the output from one stage to the next. When mismatch occurs, the spectral components at each output will not be precisely identical and the time delay property will be only approximate. This mismatch will cause the amplitude and phase of the fundamental and its harmonics to deviate from the ideal relationship described in (3). A mathematical analysis of the effects of mismatch in the PSO is quite tedious. The effects of the mismatch in the PSO, however, in the generation of spectrally pure sine waves can be small as will be verified with a later discussion of experimental and simulation results.

2.4.2 Non-idealities in Summing Network

The summing network can be implemented with active components or passive components. An operational amplifier (op-amp) based summing amplifier is an example of an active component-based summing network. Current state-of-the-art op-amps have excellent linearity up to the megahertz frequency [31-32] range. By choosing an Opamp
with low distortion, high open-loop gain at the frequency of oscillation, and high slew rate, the overall distortion of the summing network can be minimized. The other source of error is due to rounding-off of the weights described by (13) and the mismatch of the weights.

Mismatch in weights lead to amplitude and phase errors in the desired harmonic at the output. If it is assumed that the stages of the PSO are identical, equation (8) rewritten below remains valid:

\[
\sum_{i=1}^{N} \lambda_i \exp \left[ -j \frac{2\pi}{N} (i-1)k \right] = \beta_k
\]  

(24)

Errors in the weights used in the weighted summation will now be considered. Let each weight, \( \lambda_i \), be expressed as the sum of a nominal component and an error component as given by:

\[
\lambda_i = \lambda_{i,S} + \lambda_{i,e}
\]  

(25)

The nominal component of the weight is obtained using (13). By definition, the \( k \)th harmonic in \( Y(t) \) is the product of \( \beta_k \) and \( A_k \). The errors in the weights result in an error, \( A_{k,e} \), in the Fourier coefficient of the \( k \)th harmonic of \( Y(t) \). Multiplying both sides of (24) by \( A_k \), it follows that:

\[
A_k \sum_{i=1}^{N} \frac{\lambda_{i,S} (1 + \frac{\lambda_{i,e}}{\lambda_{i,S}}) \exp \left[ -j \frac{2\pi}{N} (i-1)k \right]}{\lambda_{i,S}} = \beta_k A_k + A_{k,e}
\]  

(26)

Normalizing the above variables the above expression can be expressed as:

\[
\sum_{i=1}^{N} \lambda_{i,S} \delta \left\{ \cos \left[ \frac{2\pi}{N} (i-1)k \right] - j \sin \left[ \frac{2\pi}{N} (i-1)k \right] \right\} = \varepsilon_k
\]  

(27)
where $\delta_i = \lambda_{i,e}/\lambda_{i,S}$ is the normalized error in the $i^{th}$ stage’s weight and $\epsilon_k = A_{e,k}/A_k$ is the normalized error in the $k^{th}$ harmonic’s Fourier coefficient. It is assumed that the errors $\delta_i$ are uncorrelated random variables with zero mean and standard deviation $\sigma_{i,W}$. The normalized error in the $k^{th}$ harmonic component becomes a random variable. Since the variable of interest is the power in the $k^{th}$ harmonic, the distribution of the variable, $|\epsilon_k|^2$ is observed. It can be shown that the expectation is given by:

$$E[|\epsilon_k|^2] = \sum_{i=1}^{N} (\sigma_{i,W}\lambda_{i,S})^2$$

(28)

Obtaining a closed form expression for the variance for any $N$-stage PSO is not straightforward. For a three stage PSO, with weights with the same standard deviation $\sigma_W$, for harmonics that are non-multiples of 3:

$$Var[|\epsilon_k|^2] = 3\sigma_w^4 \sum_{i=1}^{N} (\lambda_{i,S})^4 + 3\sigma_w^4 \sum_{i\neq k}^{N} (\lambda_{i,S})^2 (\lambda_{k,S})^2 - \sigma_w^4 \left( \sum_{i=1}^{N} (\lambda_{i,S})^2 \right)^2$$

(29)

For harmonics that are multiples of 3:

$$Var[|\epsilon_k|^2] = 2\sigma_w^2 \sum_{i=1}^{N} (\lambda_{i,S})^2$$

(30)

The above equations can be used with a particular implementation of the summing network to decide how to choose weights for a certain mean and variance in $|\epsilon_k|^2$. It is important to note that in (28) and (29) by reducing $\sigma_W$ both the mean and variance can be reduced. Consider a summing network that is implemented with an operational amplifier on-chip as shown in Figure 2.7.
The weighting for each output of the PSO is set by gain for each of the inputs. The output is given by:

\[ V_{OUT} = - \left( \frac{R_F}{R_1} X_{O1} + \frac{R_F}{R_2} X_{O2} + \frac{R_F}{R_3} X_{O3} + \ldots + \frac{R_F}{R_N} X_{ON} \right) \]  (31)

where \( R_i = R_F / \lambda_i \). It is assumed that the only non-ideal effects are those due to local random variations in the sheet resistance of the resistor. The resistor is assumed to be rectangular with length, \( L \) and width, \( W \). As discussed in section 2.3.3, harmonic cancellation is only affected by the relative accuracy of the weights. Hence the variation in the value of \( R_F \) is neglected. Random variations in the input resistors, \( R_1 \) to \( R_N \) are considered. It can be shown that if all the resistors are equally sized, the variance of the normalized error in \( i^{th} \) weight is given by [33]:

\[ \sigma^2_w = \frac{1}{A_r} \left( \frac{A_p}{R_{SH}} \right)^2 \]  (32)
where, $A_k$ is the area of resistor $R$, $A_p$ is the process parameter that characterizes the random local sheet resistance variation and $R_{SH}$ is the nominal value of sheet resistance. For a desired variance in the error of $k^{th}$ Fourier coefficient, the area to be allocated to the resistors can be obtained using (32). A similar approach can be followed for fully differential implementation or an implementation based on passive components as shown in Figure 2.8. For example, consider a 3-stage PSO. From Table 2.1 it can be seen that the weights to cancel the third harmonic and its multiples are in the ratio 1:2:1. This can be implemented as, $R_1=R$, $R_2=0.5*R$ and $R_3=R$ in Figure 2.8.

The following example demonstrates how (29) can be used estimate the mean error in $k^{th}$ harmonic’s power in the output of weighted summation. Consider a 3-stage PSO, $N=3$. It will be assumed that the error in the weights are independent, identically distributed random variables with zero mean and standard deviation of 1%. Let the fundamental be $0\text{dBV}$ and the third harmonic before cancellation be $-50\text{dBV}$. From (29) and Table 2.2 then:
\[
E \left[ \frac{A_{e3}}{A_3} \right]^2 = (0.01)^2 \left( \frac{1}{3^2} + \frac{1}{3^2} + \frac{2^2}{3^2} \right)
= 6.667 \times 10^{-5}
\]
\[=-41.76\text{dB}\] (33)

From the above estimate it can be inferred that the third harmonic at the output would be suppressed from -50dBV to -91.76dBV on an average, with 1% error in weights. The error in the fundamental’s power is negligible. Table 2.3 summarizes the mean suppression in desired harmonics for various stages based on weights in Table 2.1 for low distortion sine wave generation. The errors are assumed to be independent, identically distributed variables with standard deviation varying from 0.1% to 10%.

<table>
<thead>
<tr>
<th>Weights error sigma</th>
<th>0.10%</th>
<th>0.50%</th>
<th>1%</th>
<th>5%</th>
<th>10%</th>
</tr>
</thead>
<tbody>
<tr>
<td>N=3</td>
<td>61.76</td>
<td>47.78</td>
<td>41.76</td>
<td>27.78</td>
<td>21.76</td>
</tr>
<tr>
<td>N=5</td>
<td>63.97</td>
<td>49.99</td>
<td>43.97</td>
<td>29.99</td>
<td>23.97</td>
</tr>
<tr>
<td>N=6</td>
<td>64.77</td>
<td>50.79</td>
<td>44.77</td>
<td>30.79</td>
<td>24.77</td>
</tr>
<tr>
<td>N=7</td>
<td>65.44</td>
<td>51.47</td>
<td>45.44</td>
<td>31.47</td>
<td>25.44</td>
</tr>
<tr>
<td>N=8</td>
<td>66.02</td>
<td>52.04</td>
<td>46.02</td>
<td>32.04</td>
<td>26.02</td>
</tr>
</tbody>
</table>

In Table 2.3 it can be observed that a 1% error in weights results in approximately 40dB mean harmonic suppression for the 3-stage PSO. But with more number of stages the suppression increases. Error in the proposed method due to mismatch in PSO is studied by Monte Carlo simulations for a 3-stage PSO and 5-stage PSO implemented with discrete components. Monte-Carlo simulations are also used to guide the design of on-chip PSO. The lower harmonics, especially the second and the third harmonic, are
observed to study the effectiveness of the proposed method. The results are presented in the simulation results section.

2.5 Discrete Circuit Implementation

The proposed method is demonstrated for applications in DIB based testing using the circuit in Figure 2.9. An opamp based inverting integrator is used to implement the frequency selective networks.

![Figure 2.9 Schematic for simulations for discrete implementation](image)

A diode-based amplitude stabilization circuit [15] provides gain control for each stage.

The transfer function, $T(s)$, of each delay stage in the PSO is:
\[ T(s) = -\frac{R_f / R_{IN}}{1 + sC_fR_f} \]  

(34)

Since each stage is an inverting integrator, (4) becomes:

\[ \Psi_{i,k} = \phi_k - (\pi + \frac{\pi}{N})(i-1)k \]  

(35)

The consequence of (35) is that in an N-stage PSO, the order of the outputs differs from that described in (3). The weighted summation is implemented using an op-amp based summing amplifier as shown in Figure 2.9. The summing network uses two amplifiers to implement negative and positive weights. The summing network provides two options that are important for low distortion sine wave generation. Firstly, a simple first-order filter can be accommodated by including capacitor \( C_G \) as shown in Figure 2.9. This filter can provide significant attenuation of higher harmonics thereby lowering the THD. \( R_G \) can be used to amplify the signal to obtain a larger signal swing. Secondly, the op-amp allows various complex loads to be driven with the summing circuit.

### 2.6 Simulation Results for Discrete Implementation

The proposed circuit was simulated using the Spectre simulator in Cadence Virtuoso. Transient analysis and periodic steady state analysis were used to observe the harmonic components with and without harmonic cancellation. Simulations were carried out using both behavioral models for the opamps and commercial opamp macromodel subcircuits. Behavioral models were used to demonstrate the basic working of the proposed method. Simulations with commercial opamp macromodel subcircuits were
carried to study the effects of the opamp’s frequency dependent distortion. 3-stage, 5-stage and 8-stage PSOs were considered with the simulations.

### 2.6.1 Simulations with Behavioral Models

The opamp in each integrator stage of the 3-stage PSO was modeled as a behavioral opamp from ahdlLib (Figure 2.9). Behavioral model opamps were also used in the summing circuit. The supply voltage was set at +/-2.5V. Components values were set as follows: \( R_f = 10k\Omega \), \( R_{\text{IN}} \), and \( C_f \) were set such that the oscillation frequency is 2.7kHz and the voltage swing at the output of each stage of the PSO is 3Vpp. The resistors in the amplitude stabilization network, \( R_T \) and \( R_M \), were 25k\Omega each. Diodes D1 and D2 were made from diode-connected pnp transitors available in a 0.5u CMOS process. The resistances in the summing amplifier were \( R = 50k\Omega \). The first-order filter is disabled by disconnecting \( C_G \) and setting \( R_G \) for a unity gain. The weights for the summation circuit for \( N=3, 5, 6, 7, 8 \) & 9 were obtained from Table 2.2.

A transient analysis was performed on the PSOs. The data was processed in MATLAB using a non-coherency correction algorithm [34] to obtain accurate frequency spectrum for each case. DFT plots obtained using the Fast Fourier Transform (FFT) of the PSO output, \( X_{O1}(t) \), and the output of the weighted summation operation, \( Y(t) \), are shown in Figure 2.10-2.15.

In Figure 2.10, the blue DFT spectrum is of the PSO output. It can be observed that the spectrum is dominated by odd order harmonics with the third harmonic being the most dominant followed by the fifth. After weighted summation of the outputs using the
proposed method, the third harmonic and its multiples are cancelled as described in Table 2.1. This can be seen in the red FFT spectrum. The fifth harmonic is the highest un-cancelled harmonic.

Figure 2.10 DFT Spectrum for 3-stage PSO

Figure 2.11 DFT Spectrum for 5-stage PSO
Figure 2.12 DFT Spectrum for 6-stage PSO

Figure 2.13 DFT Spectrum for 7-stage PSO
Figure 2.14 DFT Spectrum for 8-stage PSO

Figure 2.15 DFT Spectrum for 9-stage PSO
Table 2.4 Behavioral Simulations: Distortion Performance Summary

<table>
<thead>
<tr>
<th>Number of Stages</th>
<th>W/O HD Cancel</th>
<th></th>
<th>W. HD Cancel</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Amp.(dBV)</td>
<td>THD(dB)</td>
<td>Amp.(dBV)</td>
<td>THD(dB)</td>
</tr>
<tr>
<td>3</td>
<td>-2.2</td>
<td>-49.5</td>
<td>-2.2</td>
<td>-62.7</td>
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<tr>
<td>5</td>
<td>-2.2</td>
<td>-38.41</td>
<td>-2.2</td>
<td>-73.34</td>
</tr>
<tr>
<td>6</td>
<td>-2.2</td>
<td>-58.4</td>
<td>-2.2</td>
<td>68.34</td>
</tr>
<tr>
<td>7</td>
<td>-2.2</td>
<td>-32.4</td>
<td>-2.2</td>
<td>83.33</td>
</tr>
<tr>
<td>8</td>
<td>-2.2</td>
<td>-45.93</td>
<td>-2.2</td>
<td>-75.26</td>
</tr>
<tr>
<td>9</td>
<td>-2.3</td>
<td>-27.82</td>
<td>-2.3</td>
<td>-92.17</td>
</tr>
</tbody>
</table>

In Figure 2.14, for N=8, the highest dominant harmonic after harmonic suppression is the seventh harmonic. The output voltage’s amplitude and THD are tabulated in Table 2.4 for spectrum of $X_{o1}(t)$ without harmonic suppression and with harmonic suppression using the proposed method. The resulting THD improvement can be observed in the Table 2.4. It can also be observed that the THD at the output of the PSO increases with the number of stages in the PSO for the same signal swing and oscillation frequency.

2.6.2 Simulations with Opamp Macromodels

In this section, the effect of frequency dependent op-amp distortion on harmonic supression is studied. Commercial LF356, OPA134 and OPA627 macromodel subcircuits from Texas Instruments [35-37] are used for the simulations. The Gain Bandwidth (GBW), Slew Rate (SR) and Quiescent Current ($I_Q$) are tabulated in Table 2.5. OPA134, with 8MHz GBW, is chosen for the opamp in the integrator for the PSO core to operate over a large frequency range. 1N4009 rectifier diodes with sub-circuit macro-models were used for the linearization diodes in the integrator.
LF356 macro-models were used for the amplifiers in the summing circuit. The supply voltage was set to +/-15V. \( R_F \) and \( C_F \) in the integrator were adjusted to obtain a 4Vpp signal swing at oscillation frequencies of \( f=2\text{kHz}, 10\text{kHz}, 20\text{kHz}, 100\text{kHz} \) and 180kHz. The resistor values of \( R_F=10\text{k}\Omega \) and \( R_T = R_M = 200\text{k}\Omega \) were used in the simulations. The resistance in the summing amplifier was set at \( R = R_G=50\text{k}\Omega \). The first-order filter can be disabled by disconnecting \( C_G \) and setting \( R_G \) for a unity gain. Periodic Steady State (PSS) analysis is used to obtain harmonic components of the oscillation frequency.

At each of the aforementioned frequencies the THD of the sine wave obtained after harmonic suppression was noted. The simulation was repeated for OPA134 and OPA627 macro-model circuits used in the summing network. The results for a case with the OPA134 in the summing network are summarized in Table 2.6. A plot comparing the performance of the LF356, OPA134 and the OPA627 is shown in Figure 2.14.

Table 2.6 shows the odd harmonics with the OPA134 in the summing network for frequency of oscillation set to \( f=10\text{kHz} \). The symmetric nature of the amplitude limiter circuit generates very low even order harmonics which were of the order -160dBV. Hence they are not included in the table. It can be observed that after harmonic suppression using the proposed method, the third harmonic drops from -54dBV to -99.6dBV.

<table>
<thead>
<tr>
<th>Opamp specifications</th>
<th>GBW(MHz)</th>
<th>SR(V/\mu s)</th>
<th>( I_Q )(mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LF356</td>
<td>5</td>
<td>12</td>
<td>5</td>
</tr>
<tr>
<td>OPA134</td>
<td>8</td>
<td>20</td>
<td>4</td>
</tr>
<tr>
<td>OPA627</td>
<td>16</td>
<td>55</td>
<td>7.5</td>
</tr>
</tbody>
</table>
Table 2.6 3-stage PSO with HD Suppression, OPA 134 in Summing Network, f=10kHz

<table>
<thead>
<tr>
<th>Frequency Component</th>
<th>W/O HD Cancel (dBV)</th>
<th>W. HD Cancel (dBV)</th>
<th>W. HD Cancel, Filter (dBV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HD1</td>
<td>6.38</td>
<td>6.38</td>
<td>12.7</td>
</tr>
<tr>
<td>HD3</td>
<td>-54.4</td>
<td>-99.6</td>
<td>-100.5</td>
</tr>
<tr>
<td>HD5</td>
<td>-91.3</td>
<td>-91.3</td>
<td>-96.2</td>
</tr>
<tr>
<td>HD7</td>
<td>-76.7</td>
<td>-76.7</td>
<td>-84.5</td>
</tr>
<tr>
<td>HD9</td>
<td>-93.7</td>
<td>-125.3</td>
<td>-140.6</td>
</tr>
<tr>
<td>HD11</td>
<td>-94.8</td>
<td>-94.9</td>
<td>-106.5</td>
</tr>
<tr>
<td>THD(dB)</td>
<td>-60.75</td>
<td>-82.91</td>
<td>-96.82</td>
</tr>
</tbody>
</table>

The ninth harmonic is significantly attenuated too. The other harmonic components are not affected as expected. The THD improves from -60.75 dB to -82.91dB. The THD after suppression with the LF356, OPA134 and OPA627 opamps at the five frequencies is plotted in Figure 2.16.

Figure 2.16 3-Stage: THD vs. Frequency, 4Vpp
It can be observed that the performance of the three op-amps is comparable at frequencies up to 20kHz. At higher frequencies the nonlinearity of LF356 in the summing network dominates the output spectrum. OPA134 and OPA627 perform better than LF356 at higher frequencies due to their better SR and GBW. For next set of simulations, the core PSO is unchanged. \( R_G \) and \( C_G \) are chosen such that the fundamental’s amplitude after harmonic cancellation is 8Vpp.

Simulations with the OPA134 and OPA627 opamps were performed at the same 5 frequencies. The results are plotted in Figure 2.17. \( R_G \) sets the dc gain to 2.82(9dB). This results in a 12dBV fundamental at the frequency of oscillation. The lower order harmonics, 2\(^{nd}\) and 3\(^{rd}\), are not affected but the harmonics fifth and higher are attenuated by at least 5dB. The result is an overall THD improvement of at least 15dB.
Table 2.7 5-stage PSO with HD Cancellation, OPA 134 in Summing Network, f=10kHz

<table>
<thead>
<tr>
<th>Frequency Component</th>
<th>W/O HD Cancel (dBV)</th>
<th>W. HD Cancel (dBV)</th>
<th>W. HD Cancel, Filter (dBV)</th>
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<tr>
<td>HD1</td>
<td>6.07</td>
<td>6.07</td>
<td>12.47</td>
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<tr>
<td>HD3</td>
<td>-44.3</td>
<td>-105.7</td>
<td>-104</td>
</tr>
<tr>
<td>HD5</td>
<td>-77</td>
<td>-117</td>
<td>-127</td>
</tr>
<tr>
<td>HD7</td>
<td>-73</td>
<td>-129</td>
<td>-136</td>
</tr>
<tr>
<td>HD9</td>
<td>-93</td>
<td>-92</td>
<td>-102</td>
</tr>
<tr>
<td>HD11</td>
<td>-85.4</td>
<td>-85.3</td>
<td>-96.9</td>
</tr>
<tr>
<td>THD(dB)</td>
<td>-50.3</td>
<td>-90.5</td>
<td>-107.6</td>
</tr>
</tbody>
</table>

The various harmonics are tabulated in column 3 of Table 2.7. The filter enables obtaining THD performance of better than -95dB for frequencies as high as 100kHz. At higher frequencies the distortion performance is well below -80dB. Results from simulations with a 5-stage PSO are shown in Table 2.7, Figure 2.18 and Figure 2.19. Table 2.7 shows the odd harmonics with OPA134 in the summing network, for frequency of oscillation set to f=10kHz. The even order harmonics are omitted in the table as they are in the order of -160dBV. It can be observed in Table 2.7 that after harmonic cancellation using the proposed method, the third harmonic, the fifth harmonic and the seventh harmonic are significantly attenuated. At f=10kHz and 4Vpp signal swing, the THD improves from -50.3dB to -90.5dB as shown in third column of Table VI. In Figure 2.18, the performance of LF356, OPA134 and OPA627 in the summing network are compared. The trends are similar to that observed in Figure 2.16.
At frequencies greater than 20kHz, the OPA134 and OPA627 opamps perform better than the LF356. With the filter enabled and signal swing set at 8Vpp, the harmonics at f=10kHz with the OPA134 are tabulated in the fourth column of Table 2.7. The first-
order filter enables obtaining THD of -107.6dB. In Figure 2.19, the THD performance with the OPA134 and OPA627 op amps over the five frequencies is plotted. Harmonic suppression with the proposed method with a simple first-order filter results in a THD of better than -90dB at frequencies as high as 180kHz with the OPA627.

2.6.3 Robustness Study of Discrete Implementation

To study the robustness of the proposed method to non-idealities in the PSO and mismatch errors in summation network, Monte Carlo (MC) analysis was performed on the 3-stage and 5-stage PSO. To simulate mismatch, resistance and capacitance were modeled with a Gaussian distribution with $3\sigma$ values of 1% and 5% of their nominal values. Mismatch in diodes and opamps were not considered for the MC runs. The frequency of oscillation was fixed at $f=10kHz$ and a voltage swing at 8Vpp. The first-order filter was enabled. A total of 100 runs were performed in the Monte Carlo analyses for the 3-stage and 5-stage PSOs.

The performance of the weighted summation for the nominal case is tabulated in the third column of Table 2.6 for the 3-stage PSO. Mismatch in passive components introduces a second harmonic in $X_{O1}$ and $V_{OUT}$. The second harmonic (HD2) in $V_{OUT}$ for 1% mismatch and 5% mismatch is observed, and a histogram of HD2 with mismatch is plotted in Figure 2.20. The mean HD2 with 1% and 5% mismatch are -93dBV and -79dBV respectively. The third harmonic attenuation, termed as HD3 Attenuation, in $V_{OUT}$ for 1% mismatch and 5% mismatch is observed, and a histogram of HD3 Attenuation with mismatch is plotted in Figure 2.21.
Figure 2.20 HD2 in $V_{OUT}$, $f=10$ kHz, 8Vpp, (a): 1% mismatch (b) 5% mismatch

Figure 2.21 HD3 Attenuation, $f=10$ kHz, 8Vpp, (a): 1% mismatch (b) 5% mismatch

The mean HD3 Attenuation with 1% and 5% mismatch are 40dB and 28dB respectively.

The mean HD3 attenuation of 28dB with 5% mismatch is sufficient to allow the next highest energy harmonic to dominate, typically a higher frequency harmonic. It can be
estimated that with 5% mismatch, the fundamental around 12dBV, the second harmonic hovering around -79dBV and other harmonics lesser than -80dBV, the overall THD would be around -91 dB. Under similar conditions with 1% mismatch, the THD can be estimated to be as low as -105dB.

The overall distortion in $V_{\text{OUT}}$, is measured by observing the THD for 1% mismatch and 5% mismatch. The THD for 1% and 5% mismatch are plotted against 100 MC runs in Figure 2.22 for the 3-stage PSO. The mean THD with 1% mismatch and 5% mismatch is -93dB and -85dB respectively. Monte Carlo simulations for the 5-stage PSO are performend at $f=10\text{kHz}$ and 8Vpp signal swing. The THD obtained for 1% and 5% mismatch are plotted in Figure 2.23. The mean THD with 1% mismatch and 5% mismatch are -94dB and -81dB respectively.

![3-Stage:MC Simulations](image)

Figure 2.22 3-stage Monte Carlo, $f=10 \text{kHz}$, 8Vpp
Mismatch in diodes and opamps would also affect the achievable harmonic suppression. Cancellation of even harmonics, especially HD2 in PSO core, depends on the symmetry of amplitude stabilization function and the matching of this function across stages. Matched diodes can ensure symmetry in each stage. Ensuring matching across stages is a more challenging task.

2.7 Experimental Results

A prototype of a three stage PSO was built on a breadboard. Figure 2.24 shows the schematic of the 3-stage PSO and the weighted summation circuit. Each stage is an opamp based integrator. LF356N opamps were used in the integrator, buffer stage and the summing network. 5% tolerance passive components were used in the entire circuit with no attempt being made to match any components. 1N4001 diodes were used in the amplitude stabilization structure. The passive component values used were, $R_{IN}=4.9\,\text{k}\Omega$, $R_f=10\,\text{k}\Omega$, $C_f=10\text{nF}$, $R_T=R_M=200\,\text{k}\Omega$, $R=4.7\,\text{k}\Omega$. 
The weighted summation circuit has an inherent gain of 3. The DFT for $X_{O1}$, $V_{OUT}$ and VF were analyzed using the Audio Precision SYS2722. The data is processed in MATLAB using a non-coherency correction algorithm proposed in [34]. In Figure 2.25-27, the DFT spectrum of $X_{O1}, V_{OUT}$ and VF are plotted respectively.
It can be observed from Figure 2.25 and Figure 2.26 that all the frequency components in the summed output rise by approximately 9dB in Figure 2.26 except for the third harmonic @ f=8.212 kHz which drops by a net 26dB. With suppression of the third harmonic, distortion in the output spectrum is dominated by the fifth harmonic. A first-order passive filter followed by a low-pass, second-order, Sallen-Key filter with 3dB frequencies at the oscillator’s frequency of f=2.737 kHz was designed. The DFT Spectrum after filtering of the signal VF is as shown in Figure 2.27.

![FFT](image)

Figure 2.25 Expt. Results: DFT Spectrum of Oscillator’s output, $X_O$
Figure 2.26 Expt. Results: DFT Spectrum of Summer's output, $V_{\text{OUT}}$

Figure 2.27 Expt Results: DFT Spectrum of Filter's output, $V_F$
The spectrum is of an ultra-pure sine wave with a Spurious Free Dynamic Range (SFDR) of 103.5dB. If a low-pass third-order filter, were placed at X₀₁, the THD of the filtered signal would only be -82dB [38]. By suppressing the third harmonic, the proposed method has made filtering more effective.

For a sine wave generator that can work at higher frequencies, the summing network was changed to the one shown in Figure 2.28. The opamp in the 3-stage PSO’s integrator stage was replaced with the OPA134. Buffer opamps and the opamps in the summing network were replaced with the OPA134. Four oscillation frequencies were chosen for the experiments, f=4.3kHz, 6.4kHz, 8.6kHz and 29kHz. 5% tolerance passive components were used. Component values of R₉, R₉, R₉ were the same as those used in Figure 2.24. Rᵢᵣₙ was around 4.9kΩ and was used to adjust the pole location and the signal swing of the PSO. Resistor, R=50kΩ, was used in the summing network. The oscillation frequency was varied by changing C₉.

Figure 2.28 Expt. Results: 3-Stage PSO with Summing N/W + 1st Order Filter
The poles of the PSO were adjusted for each of the frequencies to set the signal swing. $R_G$ and $C_G$ were chosen for each frequency case to set the pole location and the final signal swing to 7Vpp. The results are plotted in Figure 2.29. The THD of the 3-stage PSO based sine wave generator is around -83dB over a wide frequency range shown in Figure 2.29. In Figure 2.27, for $f=2.7\text{kHz}$, a first-order filter and a second-order Sallen-Key filter were used to drop the THD to -100dB. The same filter solution can be used over the audio frequency, 2kHz-20kHz, to obtain -100dB sine waves. This performance gain is obtained at a negligible cost of the power and area overhead of a filter.

To demonstrate third and the fifth harmonic suppression, the quasi four-stage PSO shown in Figure 2.30 was set-up on a breadboard. The cancellation scheme described in Table 2.1 and Table 2.2 requires an eight stage PSO to cancel the third and
the fifth harmonics. The 8-stage can be viewed as a 4-stage fully differential structure and single ended version of the 4-stage can be realized as shown in Figure 2.30. The weighted summation circuit has an inherent gain of sqrt(2). In Figure 2.32-34, the DFT spectrum of $X_{O1}, V_{OUT}$ and $VF$ are plotted respectively.

Figure 2.30 Expt. Results: 4-Stage PSO Prototype

Figure 2.31 Expt. Results: 4-Stage PSO Prototype
Figure 2.32 Expt. Results: DFT Spectrum of Oscillator’s output, V1

Figure 2.33 Expt. Results: DFT Spectrum of Summer’s output, VOUT
It can be observed from the above figures that all frequency components rise by approximately 9 dB in Figure 2.33 but for the third harmonic @ f=4.788 kHz which drops by 22 dB and the fifth harmonic @ f=7.98 kHz that drops by 29 dB. A cascade of two first-order filters follows the output of the cancellation block. The 3-dB frequencies were set close to the oscillator’s frequency of f=1.596 kHz. The FFT Spectrum after filtering of the signal VF is as shown in Figure 2.29. The spectrum is of an ultra-pure sine wave with a SFDR of 105.44 dB.

The proposed sine wave generator can generate a -82 dB sine wave at f=29 kHz with a simple first-order filter. Few works have focused on techniques to generate low distortion sine wave generators in discrete implementations. The Wien Bridge oscillator, with amplitude stabilization provided by an incandescent bulb, is a widely used circuit to
generate low distortion sine wave in discrete implementations [6]. Well known drawbacks of using light bulbs for amplitude stabilization are long response time to amplitude tuning, sensitivity to filament’s properties, and limited frequency range of operation. A diode based amplitude stabilization scheme as shown in Figure 2.6 for the Wien Bridge results in an oscillator with modest THD of over -60dB. They are not well suited for DIB and BIST applications.

2.8 On-chip low distortion signal generation

The Phase Shift Oscillator (PSO) implementation proposed in section 2.7 relied on a gain limiter circuit to provide amplitude stabilization in each stage. It is well known that transistor’s inherent non-linear behavior can be made use of to provide amplitude stabilization [39-40]. For the on-chip version of the proposed method, fully-differential, first-order delay stages are considered. Transistor circuits in each stage realize the desired transfer function of the frequency selective and also function as amplitude stabilization circuits. In integrated form, the term “ring oscillator” is often used instead of PSO to denote a cascaded feedback loop of identical phase shift stages used to build oscillators. No attempt will be made here to distinguish between a ring oscillator and a PSO. With this clarification in notation, the ring oscillator was implemented in a 0.13um CMOS process with 3.3 V transistors. Simulation results show that the oscillator achieves a low THD of -82dBc producing a 2 Vpp signal while consuming a total of 2.5mA of current.
2.8.1 Architecture of the low distortion sine wave generator

A three-stage ring oscillator forms the core of the sine wave generator. Summing is performed by a high speed Operational Transconductance Amplifier (OTA) in a feedback configuration. The outputs of the Ring Oscillator were buffered using a simple PMOS source follower to mitigate the effects of mismatch due to differences in loading.

Figure 2.35 On-chip sine wave generator – 3-stage PSO with source follower

Figure 2.36 On-chip Sine wave generator-OTA based Summer
2.8.2 Delay Stage

In any fully differential circuit, left-right symmetry or matching of “half-circuits” is important to suppress even harmonics. But in real circuits mismatch of components is unavoidable and sufficient resources have to be allocated to mitigate the effects of mismatch. Through Monte-Carlo Simulations of the Ring Oscillator designed to operate at low MHz frequencies, it has been observed that by allocating more area to linear loads, the even harmonics can be suppressed. The delay stage consists of a PMOS differential amplifier with a resistor load in parallel with a capacitor. A tail current source that can be adjusted sets the quiescent current for the stage. The resistor is a polysilicon resistor available in the CMOS process. Metal-Insulator-Metal (MIM) capacitors are chosen for the capacitor. An array of the capacitors is used to vary the frequency in discrete steps. The sheet resistance of the resistor has a +/- 20% processing tolerance. Programmability in the tail current source and capacitor array ensures oscillations over the targeted frequency range. Each delay stage consumes 100uA quiescent current. The transconductance of input pair under dc conditions is 85uS. The load resistance, $R_L$, is set to 20kΩ

2.8.3 Source Follower

A conventional source follower with PMOS input and PMOS current source is used to buffer the output of the delay stages. The schematic of a source follower cell is shown in the Fig. 2.38. The source follower is designed to drive 15kΩ resistive loads of the OTA summing network. Monte Carlo simulations were performed for each source follower cell to ensure the second harmonics are sufficiently low. The bulk of the
sources are tied to the sources to avoid mismatch of transconductance due to bulk effects ($g_{mb}$). Each source follower cell consumes 200uA quiescent current. The transconductance of input under dc conditions is 0.5uS.

![Diagram](image)

Figure 2.37 On-chip Sine wave generator – Delay Stage

![Diagram](image)

Figure 2.38 On-chip Sine wave generator – Source Follower Cell
2.8.4 OTA based Summing amplifier design

The OTA is a two stage, fully differential Miller compensated architecture with output Common Mode Feedback (CMFB). The OTA is designed to drive large resistive loads and capacitive loads as high as 20pF. The unit resistor, R, in the feedback network is 30kΩ. The OTA is compensated for a feedback factor, β=1/4. Loop gain characteristics of the OTA are listed in Table 2.8.

Table 2.8 OTA Performance Summary

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_Q$</td>
<td>1.4mA</td>
</tr>
<tr>
<td>$\beta$</td>
<td>0.25</td>
</tr>
<tr>
<td>Loop GBW</td>
<td>18MHz</td>
</tr>
<tr>
<td>Loop DCG</td>
<td>92dB</td>
</tr>
<tr>
<td>Loop PM</td>
<td>60°</td>
</tr>
<tr>
<td>$C_L$</td>
<td>5pF</td>
</tr>
</tbody>
</table>

The sine wave generator consumes a total quiescent current of 2.5mA.

2.8.5 Simulations Results

All simulations were carried out in the Cadence Virtuoso IC design environment with a Process Delivery Kit (PDK) for a 0.13um CMOS process made available through MOSIS. Transient simulation and steady state simulations were carried out to analyze the spectrum of the sine waves generated. Transient simulations must be carried out for long periods to allow accurate settling of the waveforms. Extreme care must be taken to ensure uniform sampling for running the DFT in order to make interpolation errors negligible. In contrast, Harmonic-Balance (HB) simulations allow analyzing the
spectrum in steady state with consuming very little simulation time in comparison with transient simulations. With the Harmonic Balance method the circuit is compactly represented using a truncated Fourier series. Efficient numerical methods solve for these Fourier coefficients. This is of particular interest in our proposed method as we would like to observe Fourier coefficients to measure the energy in various harmonic components.

Table 2.9 shows results obtained from a nominal simulation of the ring oscillator operating at fosc=3MHz. The first five harmonics are recorded; the other harmonic components are in the noise floor. Using the proposed method with the three-stage PSO, the 3rd harmonics and it multiples can be cancelled. The even harmonics are expected to be at the algorithmic noise floor due to the fully differential implementation. Table 2.9 summarizes the results. It can be send that third harmonic drops by a total 23 dB (Gain =3). It is eventually limited by the third harmonic of the summing network. The signal swing at the output is 2Vpp.

<table>
<thead>
<tr>
<th>Frequency Component</th>
<th>W/O HD Cancel (dBV)</th>
<th>W. HD Cancel (dBV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HD1</td>
<td>-9.331</td>
<td>0.3</td>
</tr>
<tr>
<td>HD2</td>
<td>-158</td>
<td>-153</td>
</tr>
<tr>
<td>HD3</td>
<td>-68.24</td>
<td>-82</td>
</tr>
<tr>
<td>HD4</td>
<td>-176</td>
<td>-172</td>
</tr>
<tr>
<td>HD5</td>
<td>-108</td>
<td>-99</td>
</tr>
<tr>
<td>THD(dB)</td>
<td>-58.91</td>
<td>-83.24</td>
</tr>
</tbody>
</table>
Mismatch of devices is going to limit the amount of suppression of the third harmonic. Mismatch is also going to limit the amount of suppression of the second harmonic. In the design, programmability and good layout techniques can ensure that errors due to process variations have negligible effect on the amount of suppression of the harmonics. Local variations due to random mismatch affect the harmonic suppression attainable. Monte-Carlo (MC) runs with only mismatch errors enabled are carried out for two cases. The first case is a signal swing of 3Vpp which is set by adjusting the tail current source. 100 MC runs are carried out. The second case is a signal swing of 2Vpp. The THD for each of the case at the output, along with the second and third harmonic components are recorded. The results are summarized are summarized in Table 2.10-2.11. The THD, fundamental and first two harmonics for each of the 100 runs is recorded in Figure 2.39 and Figure 2.40.

Table 2.10 Simulation results: Monte-Carlo, Vpp=3.17V

<table>
<thead>
<tr>
<th></th>
<th>Min</th>
<th>Max</th>
<th>Mean</th>
</tr>
</thead>
<tbody>
<tr>
<td>THD(dB)</td>
<td>-77.43</td>
<td>-69.6</td>
<td>-74.29</td>
</tr>
<tr>
<td>HD1(dBV)</td>
<td>3.58</td>
<td>4.3</td>
<td>3.99</td>
</tr>
<tr>
<td>HD2(dBV)</td>
<td>-100.9</td>
<td>-67.04</td>
<td>-80.1</td>
</tr>
<tr>
<td>HD3(dBV)</td>
<td>-75.66</td>
<td>-70.22</td>
<td>-72.25</td>
</tr>
</tbody>
</table>

Table 2.11 Simulation results: Monte-Carlo, Vpp=2V

<table>
<thead>
<tr>
<th></th>
<th>Min</th>
<th>Max</th>
<th>Mean</th>
</tr>
</thead>
<tbody>
<tr>
<td>THD(dB)</td>
<td>-85.34</td>
<td>-74.5</td>
<td>-81.59</td>
</tr>
<tr>
<td>HD1(dBV)</td>
<td>0.927</td>
<td>1.107</td>
<td>0.266</td>
</tr>
<tr>
<td>HD2(dBV)</td>
<td>-106.9</td>
<td>-74.94</td>
<td>-88.14</td>
</tr>
<tr>
<td>HD3(dBV)</td>
<td>-87</td>
<td>-80.2</td>
<td>-83.46</td>
</tr>
</tbody>
</table>
Figure 2.39 Simulation Results: MC, Voltage Swing=3.1V pp

Figure 2.40 Simulation Results: MC, Voltage Swing=2V pp
2.8.6 Results Discussion

Simulation results show that with the proposed sine wave generator, 82dB sine waves at large signal swings can be obtained. It should be pointed out that no filter has been used in the proposed signal generator unlike the third-order passive filter used by Elsayed [7]. Comparing the normalized voltage swing at the output, it can be observed that the proposed signal generator can produce low THD sine waves at large signal swings. The THD performance obtained is orders of magnitude better than the best numbers reported in the literature. A simple, low-Q filter can further enhance the THD performance with a small drop in voltage swing. This has been demonstrated in the discrete low distortion generator as described in the experimental results section.

Table 2.12 Comparison with State-of-Art

<table>
<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>$f_{out}$ (MHz)</td>
<td>3MHz</td>
<td>10MHz</td>
<td>10.7MHz</td>
<td>18.7MHz</td>
<td>25MHz</td>
<td>40.7 MHz</td>
<td>1 MHz</td>
</tr>
<tr>
<td>$V_{pp}/V_{dd}$ ratio</td>
<td>600m/1</td>
<td>190m</td>
<td>2.2m</td>
<td>68m</td>
<td>14.3m</td>
<td>53m</td>
<td>166m</td>
</tr>
<tr>
<td>Technology</td>
<td>0.13μm</td>
<td>0.13μm</td>
<td>0.35μm</td>
<td>0.35μm</td>
<td>0.8μm</td>
<td>0.35μm</td>
<td>0.35μm</td>
</tr>
<tr>
<td>$V_{DD}$ (V)</td>
<td>3.3</td>
<td>1.2</td>
<td>3.3</td>
<td>3.3</td>
<td>2</td>
<td>3.3</td>
<td>3.3</td>
</tr>
<tr>
<td>THD (dB)</td>
<td>-82/-75</td>
<td>-57/72*</td>
<td>-53</td>
<td>-55</td>
<td>-43.6</td>
<td>-69</td>
<td>-72</td>
</tr>
</tbody>
</table>

2.9 Conclusion

A new method to generate low distortion sinusoidal signals has been proposed. The theory presented in the paper demonstrates how an N-stage PSO with the proposed approach can be used to suppress the first N-2 harmonic components in the individual outputs of the PSO. The suppression scheme does not involve measuring the amplitude and phase of the harmonic components. The method operates over a large frequency
range, and can produce multiple outputs with precise phase relationships. Simulation results presented validate the proposed approach. Robustness simulations showed that even with only 5% precise passive components, significant improvement in distortion performance can be obtained. The results using the harmonic cancellation technique can provide significant improvements in THD over a wide frequency range. Experimental results are presented to demonstrate how the proposed technique can be used to produce -100dB THD sine wave with inexpensive components that operates over a wide range of frequencies. Simulation results for an on-chip oscillator designed in a 0.13um CMOS process are presented. The results show that the proposed technique can be used to generate sine wave with -80dB THD at large signal swings.

References


[37] "Precision High-Speed Difet ® Operational Amplifiers - OPA627" datasheet for OPA627


CHAPTER 3

ADC INTEGRAL NON-LINEARITY TESTING WITH LOW LINEARITY MONOTONIC SIGNALS

Extended Version of a paper published in IEEE International Instrumentation and Measurement Conference (I2MTC), 2011

Bharath K Vasan, Randall Geiger and Degang Chen

Abstract

Methods to test the integral non-linearity (INL) of ADCs using any monotonic signal with low linearity are proposed. Two methods that estimate the INL of the ADC by removing the error due to non-linearity in the stimulus are described. Signals, with linearity dramatically lesser than the ADC under test, can be used to accurately estimate the INL of the ADC. Simulation results show that the maximum INL estimation error for testing 14-bit ADCs using with 36 dB pure sinusoids and 7-bit linear exponential signals is around 0.6 LSB

3.1 Introduction

Quasi-static testing of Analog to Digital Converters (ADCs) is done using the “histogram method” [1]. This method requires the stimulus signal to be 3 or 4 bits more linear, or spectrally more pure than the ADC under test. For high resolution ADCs, generating such accurate signals is very challenging. The procedure is carried out on expensive instruments called Automated Test Equipments (ATEs) thus driving up the
test cost. A test procedure that can employ low cost test equipment can provide significant savings on the test cost.

Built in Self-Test (BIST) solutions to quasi-static testing is another application where low cost testing resources are desired. Stringent requirements are imposed on signal generators. The signal generators are required to be on-chip with small area and power overhead.

Recent works have proposed alternate approaches to carrying out ADC’s INL testing. The authors in [6] propose using low linearity ramps to estimate the INL of high resolution ADCs. In [7]-[8] using low spectral purity sinusoids have been proposed. In [9] low precision Dynamical Element Matching DACs are used to test the INL of high resolution ADCs. In [10] low spectral purity sinusoids are used to do spectral testing of high resolution ADCs. In [11] authors propose using simple circuitry to generate exponential signals to test the INL and DNL of high resolution ADCs. The inexpensive signal generators make the above approaches well suited not only for on-chip implementations for BIST but also in production testing environments to be used instead of expensive signal generators.

In this work we propose an algorithm that can use any monotonic signal with linearity much lesser than the ADC under test to estimate the INL. The paper is organized as follows. In section II, INL testing with monotonic signals with a known PDF is discussed. In section III testing with monotonic signals with low linearity is discussed. Two methods to identify to remove the input non linearity are described. In section IV we demonstrate the working of the proposed methods for low linearity
exponential signals and low spectral purity sinusoids using MATLAB simulations. We conclude the paper in section V.

3.2 INL Testing with Linear Signals

3.2.1 Probability Density Function of Commonly Used Signals

Histogram based test algorithms conventionally use a highly linear ramp or a spectrally pure sine wave. The PDF of the input signal is assumed to be known. In the test procedure a large number of samples of the input signal are collected using the ADC under test. A pure sine wave can be represented as:

\[ y = A \sin(\omega t) + B \]  

(1)

Either random sampling or non-coherent sampling can be used to collect the samples. Assuming a very high resolution ideal ADC, the resulting voltage distribution can be described by:

\[ y = A \sin(x) + B \]  

(2)

The random variable, \( 'x' \), can be treated as though it is uniformly distributed in the interval \( \left[ \frac{-\pi}{2}, \frac{\pi}{2} \right] \):

\[ x \sim \text{Uniform} \left[ \frac{-\pi}{2}, \frac{\pi}{2} \right] \]  

(3)

From (2) and (3), the well-known PDF of the variable of interest, ‘\( y \)’, can be derived using 2.18 in [2] as:
Using the same analogy as in (2) and (3) an ideal ramp can be represented as:

\[ y = x: \quad x \sim \text{Uniform}[x_1, x_2] \]  

(5)

The PDF of the linear ramp signal can be derived as:

\[
f_r(y) = \begin{cases} 
\frac{1}{x_2 - x_1} & x_1 \leq y \leq x_2 \\
0 & \text{otherwise}
\end{cases}
\]  

(6)

Using the analogy as in as in (2) and (3) an exponential signal can be represented as:

\[ y = D - C \cdot \exp\left(-\frac{x}{\tau}\right): \quad x \sim \text{Uniform}[x_1, x_2] \]  

(7)

The PDF of the exponential signal can be derived as:

\[
f_r(y) = \begin{cases} 
\frac{\tau}{x_2 - x_1} \cdot \frac{1}{(D - y)} & y_1 \leq y \leq y_2 \\
0 & \text{otherwise}
\end{cases}
\]  

(8)

where,

\[ y_1 = D - C \cdot \exp\left(-\frac{x_1}{\tau}\right), \quad y_2 = D - C \cdot \exp\left(-\frac{x_2}{\tau}\right) \]

In general, for any signal \( g(x) \) that is a monotone, the variable ‘\( x \)’ can be expressed as a uniform variable over a range \([x_1, x_2]\). The PDF of the signal \( y=g(x) \) can then be obtained using Theorem 2.18 in [2]. For the ADC INL test procedure, the interval \([x_1, x_2]\) is chosen such that all the codes of the ADC are hit.
3.2.2 Estimating the INL of the ADC

With the PDF of the stimulus well defined the ADC’s INL can be tested as described in [1] and [2] - [4]. The following notations will be used in the paper.

- \( n \): Resolution of the ADC under test
- \( N \): \( 2^n \), number of distinct output codes
- \( T_k \): \( k^{th} \) transition level between code \( k-1 \) and \( k \) of the ADC
- \( V_k \): Cumulative histogram count associated with \( T_k \) where

\[
V_k = \frac{\sum_{i=0}^{k-1} H_i}{N_s}, k = 1, 2, 3...N - 1
\]

(9)

- \( H_i \): Total number of samples received in code \( i \), \( i=0, 1, 2...N-1 \)
- \( N_s \): Total number of samples

ADC Input range: (0, 1)

Consider a signal \( y \) with PDF \( f_Y(y) \). The probability, \( Q_K \), of a measurement \( y < T_K \) is:

\[
Q_K = P(y < T_K) = \int_{-\infty}^{T_K} f_y(y) dy
\]

(10)

\( Q_K \) can be estimated using the cumulative histogram count;

\[
V_k \approx \int_{-\infty}^{T_K} f_y(y) dy
\]

(11)

From the above expression an estimate of the transition level, \( T_K \) can be obtained. For the pure sine wave described in (2)-(4) we have the well-known expression:

\[
\hat{T}_K = -A \cos(\pi V_k) + C
\]

(12)
For the linear ramp described in (5) and (6) we have:

\[ \hat{T}_k = V_k \]  

(13)

For the exponential signal described in (7) - (8) we have:

\[ \hat{T}_k = D + (y_1 - D).\exp[-(x_2 - x_1)V_k / \tau] \]  

(14)

The INL based on end point fit line is estimated using the formula:

\[ I\hat{N}L_k = \frac{\hat{T}_k - \hat{T}_1}{\hat{T}_{N-1} - \hat{T}_1}.(N - 2) - k, k=2,3,...,N-2 \]  

(15)

The overall INL is given by:

\[ I\hat{N}L = \max( |I\hat{N}L_k| ) \]

### 3.3 Testing With Non-Linear Signals

Real world signals have some amount of non-linearity in them which alters the distribution of the input signal. This results in errors in the transition level estimates expression described in (12)-(14). This error can be identified by using functionally related excitations (FRE) - based ADC INL testing algorithms [6]-[9]. In our work we use two non-linear signals, one being the voltage shifted version of the other to excite an ADC. The functional relationship here is a simple voltage shift. The algorithms that are developed are based on the FRE approaches described in [6] - [7].

#### 3.3.1 Stimulus Error Identification and Removal (SEIR) algorithm:

The error in transition level estimate due to the non-linearity in the input signal can be approximated using orthogonal basis functions as shown.
\[ T_k = \hat{T}_k + \sum_{j=1}^{M} a_j F_j \left( \hat{T}_k \right) + \epsilon \]  

(16)

where,

\( \hat{T}_k \): Transition level estimates with stimulus error

\( a_j \): Co-efficient of the \( j^{th} \) basis function \( F_j(t) \)

Since the ADC range is normalized the transition levels are in the range (0, 1). Over this interval sinusoidal basis functions or shifted Legendre’s polynomial basis functions can approximate the errors due to non-linearity. Two estimates of the transition levels are obtained for the two non-linear signals.

\[ T_k^{(1)} = \hat{T}_k^{(1)} + \sum_{j=1}^{M} a_j F_j \left( \hat{T}_k^{(1)} \right) + \epsilon \]  

(17)

\[ T_k^{(2)} = \hat{T}_k^{(2)} + \sum_{j=1}^{M} a_j F_j \left( \hat{T}_k^{(2)} \right) - \alpha + \epsilon \]  

(18)

\( \alpha \) is the constant voltage shift between the excitations. A Least Squares method can then be used to estimate all the basis function coefficients and the voltage shift, \( \alpha \).

\[ \{ \hat{a}_j, \hat{\alpha} \} = \]  

\[ \arg \min \{ \sum_{k=1}^{N-1} \left[ T_k^{(2)} - \hat{T}_k^{(1)} \right] + \sum_{j=1}^{M} a_j [ F_j(\hat{T}_k^{(1)}) - F_j(\hat{T}_k^{(2)})] + \alpha \} \]  

(19)

With the basis functions’ coefficients and voltage shift estimated, (16) or (17) can be used to identify the transition levels from which the INL can be estimated using (15).

### 3.3.2 Stimulus Error Removal (SER) algorithm:

The algorithm uses two estimates of transition levels obtained using (11) for the two nonlinear signals to extract equivalent histogram vectors, \( \hat{H}_j \)'s. These vectors are
used in algorithm described in [7] to obtain estimates of ADC’s INL and DNL. The algorithm is described below:

Cumulative histogram vectors, $C_k^{(1)}$ and $C_k^{(2)}$, are calculated using the following expression:

$$
C_{k-1}^{(1)} = N_s \hat{T}_k^{(1)} \\
C_{k-1}^{(2)} = N_s \hat{T}_k^{(2)}, k = 1, 2, 3... N-1
$$

(20)

Equivalent histogram vectors, $\hat{H}_j^{(1)}$ and $\hat{H}_j^{(2)}$, are calculated from the cumulative histogram vectors using the recursive relation:

$$
\hat{H}_j^{(1)} = C_j^{(1)} - C_{j-1}^{(1)} \\
\hat{H}_j^{(2)} = C_j^{(2)} - C_{j-1}^{(2)}, j = 1, 2, 3... N-2
$$

(21)

The first elements are initialized as:

$$
\hat{H}_0^{(1)} = C_0^{(1)}, \hat{H}_0^{(2)} = C_0^{(2)}
$$

With the above information, the algorithm for low-linearity ramp signals, [7], can be directly used to accurately estimate the INL of the ADC under test. The code-width of the ADC is defined as:

$$
cw_i = \frac{H_{i, S}}{H_{i, IDEAL}}, i = 1, 2, 3..N-2
$$

(22)

where,

$$
H_{i, S} = \frac{\hat{H}_i^{(1)} + \hat{H}_i^{(2)}}{2}
$$

(23)
\[ H_i^{\text{IDEAL}} = \sum_{j=0}^{i-1} \frac{\hat{H}_j^{(2)} - \hat{H}_j^{(1)}}{\hat{\alpha}} + \frac{\hat{H}_i^{(2)} - \hat{H}_i^{(1)}}{2} \]  

(24)

where, \( \hat{\alpha} \) is the estimated voltage shift given by (25)

\[
\hat{\alpha} = \frac{N - 2}{\sum_{i=1}^{N-2} \frac{H_i^{\hat{\alpha}}}{\sum_{j=0}^{i-1} \hat{H}_j^{(2)} - \hat{H}_j^{(1)} + \frac{\hat{H}_i^{(2)} - \hat{H}_i^{(1)}}{2}}}.
\]

(25)

From the code widths \( cw_i \), the INL of the ADC can be calculated using the expressions:

\[
DNL_i = cw_i - 1, i = 1, 2, 3...N - 1
\]

\[
INL_i = \sum_{j=1}^{i} DNL_j
\]

(26)

The methods described above can be extended to any monotonic signal with low linearity. The shape of the low linearity signal is known beforehand but the non-linearity present in it is not known. Assuming the non-linearity in the signal is zero the approach proposed in Section II can be used to obtain an estimate for the transition level \( T_K \). The errors due to the non-linear component can then be modeled as in (16) and the SEIR algorithm can used to estimate the INL. Alternatively, the approach proposed in SER algorithm can be used to estimate the INL.

### 3.4 Simulation Results

Simulations in MATLAB have been carried out to verify the working of the two proposed algorithms. Transition levels of a 14-bit ADC are characterized using a resistor
string representation. The ADC is randomly generated and the INL of the ADCs tested to be 5~6 LSBs. Input additive noise of 0.5 LSBs is included to simulate ADC’s device noise.

3.4.1 Low Linearity Exponential Signals

The input signal is modeled as shown in (7). A non-linearity as shown in Figure 3.1 is added to the input. The signal is now 7-bit linear. A voltage shift of 200 LSBs is used to create two versions of the signal. The two signals are sampled in time to collect a total of 262144 samples per signal. 36 Sinusoidal basis functions are used to characterize the nonlinearity in the input by the SEIR algorithm. The INL plot and the estimation error using SEIR and SER algorithm are as shown in Figure 3.2.

3.4.2 Imprecise Sinusoids

Sinusoids with randomly generated harmonic distortion components are used as a stimulus. The FFT spectrum of the stimulus used is shown in Figure 3.3. The Total Harmonic Distortion of the signal is around 36 dB. A voltage offset of 200 LSBs is used to obtain two versions of the imprecise sinusoid. 36 sinusoidal basis functions are used in the SEIR algorithm to characterize the nonlinearities. A total of 262144 samples of the input are collected over the entire ADC range for each of the sinusoids. The INL plot and the estimation error using SEIR and SER algorithm are as shown in Figure 3.4.
Figure 3.1 Non Linearity in Exponential Signal

Figure 3.2 INL Estimation with low linearity exponential signals
Figure 3.3 Spectrum of the Imprecise Sinusoidal Excitation

Figure 3.4 INL Estimation with Imprecise Sinusoids
3.4.3 Results Discussion

From Figure 3.3 we see that the FRE-based methods accurately estimate the INL of the 14-bit ADC with a maximum INL estimation error of around 0.4 LSB for both the SEIR method and the SER method. In Figure 3.4 we observe that sinusoid that is only 36 dB pure can be used to estimate the INL of the 14-bit ADC. The maximum INL estimation error is only about 0.6 LSB for both the methods. The results suggest that the any low linearity monotonic signal with linearity around 6-bits can be used to test the INL of 14-bit ADCS with an accuracy of more than 14-bits. This would allow simple signal generators suggested in [12] and [13] to accurately test the INL of 14-bit ADCs. The method’s robustness to noise in test environment, amount of non-linearity present in the signal, non-linearity present of the voltage shift, etc. are currently being investigated.

3.5 Conclusion

In this work we have proposed an algorithm that can use any low linearity monotonic signal to test the INL of high resolution ADCs. Unlike the conventional method this method requires very simple signal generators thus offering a cost saving in the hardware resources required for production testing. The method also lends itself well to BIST solutions as these simple signal generators can be implemented on–chip with low overhead.

References


CHAPTER 4
LINEARITY TESTING OF ADCS USING LOW LINEARITY STIMULUS AND KALMAN FILTERING

Extended version of a paper published in the IEEE International Conference on Circuit and Systems-2010

Bharath K Vasan, Randall Geiger and Degang Chen

Abstract

Traditional linearity testing of ADCs involves using a spectrally pure or a highly linear stimulus, along with a large number of samples per code to average out the effects of noise. Test-equipments need to house expensive instruments to provide the highly linear stimulus. The large number of samples required for the procedure results in long test times. These two factors are prime contributors to the test cost. In this paper, algorithms which use low linearity stimuli and a Kalman Filter to reduce both the hardware resources and the test time for the test procedure have been proposed. Simulations results for a 14-bit ADC show that a 7-bit linear stimulus with one sample per code can be used to measure the INL of the ADC with a maximum estimation error of 1 LSB.

4.1 Introduction

Static performance testing of Analog to Digital Converters is one of the most challenging tasks in mixed signal circuit testing. Code density testing [1]-[2] is the
standard method for measuring the static performance parameters, INL and DNL of the ADC under test. Conventional code density testing involves spectrally pure or highly linear stimulus that are typically 3 or more bits more linear than the ADC under test. Large numbers of samples are collected to average out noise for better measurement precision and accuracy. During production test, code density testing is carried out using very expensive Automated Test Equipments (ATE). Considering the fact that ADCs are high volume products, any small saving on hardware resources and/or test time for a single ADC will have a huge impact on the entire test procedure cost. Recently introduced methods [3]-[4] for linearity testing of ADCs dramatically relax the linearity requirements on signal generators. It has been shown in [5] that with the knowledge of input noise and error sources in the circuit, Kalman Filter can be used along with code density testing to obtain better estimates of INL of ADCs. In the current work, two methods that use two low linearity stimuli, SEIR and the algorithm in [4] (denoted as SER algorithm), are used with a Kalman filter to obtain accurate estimates of INL with small number of samples. The computational complexity of these two new methods is not of concern given the available computation power in today’s computers. The fewer number of samples required by the proposed algorithms to achieve a fixed accuracy, directly results in the reduction of test time, as it reduces the data acquisition time. The rest of the chapter is organized as follows. Section 4.2 briefly discusses the Kalman Filter. Section 4.4 and section 4.5 review the SEIR algorithm and the SER algorithm respectively. Kalman Filter to be used in conjunction with SEIR/SER algorithms is
proposed in section 4.6 for the two algorithms. Section 4.7 presents simulation results and section 4.8, the conclusion.

### 4.2 Kalman Filter

The Kalman Filter is an efficient recursive estimator based on linear dynamical systems. The essence of the filter is to obtain estimates of the state variables from noisy measurement data. The state variables and the measurement variables are represented by the following dynamical system of equations (discrete case):

\[
\begin{align*}
\text{State Model:} & \quad \dot{x}_k &= A\dot{x}_{k-1} + Bu_k + w_k \\
\text{Measurement Model:} & \quad y_k &= H\dot{x}_k + v_k \\
\end{align*}
\]

where, \( \dot{x}_k \) = state variable, \( y_k \) = measurement variable, \( u[k] \) is a known vector. \( w[k] \) is the process noise and \( v[k] \) is the measurement noise. \( w[k] \) and \( v[k] \) are assumed to be white Gaussian and uncorrelated to each other. \( Q \) is the process noise covariance and \( R \) the measurement noise covariance.

Kalman Filter algorithm predicts the state variable at the current time step, using the estimate of the state variable from previous time step and current measurement. Kalman filter uses the knowledge of the model specified in (1) to make this prediction.

**Kalman Filter Algorithm:**

The Kalman filter algorithm consists of two steps, measurement update and the time update as shown below:
Measurement update

\[ \text{Step 1: } K[k] = P^*[k]H^T(HP^*[k]H^T + R)^{-1} \]
\[ \text{Step 2: } \hat{x}[k] = \hat{x}^*[k] + K[k](y[k] - H\hat{x}^*[k]) \]  
\[ \text{Step 3: } P[k] = (1 - K[k]H)P^*[k] \]  

Time update

\[ \text{Step 4: } \hat{x}^*[k+1] = A\hat{x}^*[k-1] + Bu[k-1] \]
\[ \text{Step 5: } P^*[k+1] = AP[k-1]A^T + Q \]  

The filter has to be initialized before executing the above steps in recursion. The state variable, \( \hat{x}[0] \), is initialized to zero. The error covariance matrix, \( P[0] \), is initialized to zero. These variables serve as the \emph{a priori} estimate for 1\textsuperscript{st} time step. The Kalman gain, \( K[k] \), the \emph{a posteriori} estimate \( \hat{x}[k] \) and the \emph{a posteriori} covariance \( P[k] \) of the estimate are calculated in measurement step using the model and the current measurement. The \emph{a priori} for the next time step (k+1\textsuperscript{th}) are calculated in the time update step. For a detailed description of the Kalman filter please refer to [6] and [8].

In [5] algorithms were proposed that combined Kalman Filter with the conventional histogram method to improve the efficiency of the procedure. The method requires a highly linear or spectrally pure stimulus. The algorithm was adapted for Flash ADCs and Pipelined ADCs. In this work, combining Kalman filter with methods that use low-linearity stimulus is proposed.

\subsection*{4.3 Notations used in the paper}

The following notations will be used for the ADC under test in this chapter:

\( n \): Resolution of the ADC under test,
$N$: $2^n$, number of distinct output codes

$T_k$: $k^{th}$ transition level between code $k-1$ and $k$ of the ADC

$t_k$: Cumulative histogram count associated with $T_k$ where

$$t_k = \frac{\sum_{i=0}^{k-1} H_i}{N_s}, k = 1, 2, 3...N-1$$

(4)

$H_i$: Total number of samples received in code $i$,

$i=0, 1, 2...N-1$

$N_s$: Total number of samples

ADC Input range: (0, 1)

The INL$_k$ is estimated using the formula:

$$INL_k = \frac{T_k - T_1}{T_{N-1} - T_1} \cdot (N - 2) - k, k=2,3,...,N-2$$

(5)

4.4 SEIR Algorithm

The SEIR algorithm uses two low-linearity sinusoidal excitations, one being a voltage shifted version of the other. Two sets of histogram data, $H_k^{(1)}$ and $H_k^{(2)}$, are obtained from the two excitations. The transition times, $t_k^{(1)}$ and $t_k^{(2)}$ corresponding to $H_k^{(1)}$ and $H_k^{(2)}$, are calculated using (4). The equivalent transition times, $\hat{t}_k^{(1)}$ and $\hat{t}_k^{(2)}$, are obtained using steps described in [3]. Substituting in (4) we get two estimates of transition levels:
\[ T_k^{(1)} = \hat{t}_k^{(1)} + \sum_{j=1}^{M} a_j F_j(\hat{t}_k^{(1)}) + \epsilon \]  \hspace{1cm} (6)

\[ T_k^{(2)} = \hat{t}_k^{(2)} + \sum_{j=1}^{M} a_j F_j(\hat{t}_k^{(2)}) - \alpha + \epsilon \]  \hspace{1cm} (7)

\( \alpha \) is the constant voltage shift between the two sinusoidal excitations. ‘\( \epsilon \)’ is the unmodeled error which is considered negligible. Equation (6) and (7) represent the transition levels of the same ADC. Therefore, \( T_k^{(1)} \) and \( T_k^{(2)} \) can be eliminated from (6) and (7) and a least squares method can be used to obtain an estimate of all basis function coefficients and the shift, \( \alpha \), as described in (8).

\[
\{ \hat{a}_j, \hat{\alpha} \} = \arg \min \left\{ \sum_{k=1}^{N} [\hat{t}_k^{(1)} - \hat{t}_k^{(2)}] + \sum_{j=1}^{M} a_j [F_j(\hat{t}_k^{(1)}) - F_j(\hat{t}_k^{(2)}) + \alpha]^2 \right\} \hspace{1cm} (8)
\]

With the basis functions’ coefficients and voltage shift estimated, the transition levels of the ADC can be estimated using (6) or (7). The INL of the ADC can then be estimated using (5).

4.5 SER Algorithm

The SER algorithm uses histogram data from two low-linearity ramps, one being the shifted version of the other, to remove the stimulus error and characterize the INL of the ADC. The stimuli are two low-linearity monotonic excitations; one being a voltage shifted version of the other. The equivalent transition times, \( \hat{t}_k^{(1)} \) and \( \hat{t}_k^{(2)} \) are obtained using steps as described in [4].
Cumulative histogram vectors, $C_k^{(1)}$ and $C_k^{(2)}$, are calculated using the following expression:

\[
C_{k-1}^{(1)} = Ns\hat{I}_k^{(1)} \\
C_{k-1}^{(2)} = Ns\hat{I}_k^{(2)}, k = 1, 2, 3... N-1
\]  

(9)

Equivalent histogram vectors, $\hat{H}_j^{(1)}$ and $\hat{H}_j^{(2)}$, are calculated from the cumulative histogram vectors using the recursive relation:

\[
\hat{H}_j^{(1)} = C_j^{(1)} - C_{j-1}^{(1)} \\
\hat{H}_j^{(2)} = C_j^{(2)} - C_{j-1}^{(2)}, j = 1, 2, 3... N - 2
\]  

(10)

The first elements are initialized as:

\[
\hat{H}_0^{(1)} = C_0^{(1)}, \hat{H}_0^{(2)} = C_0^{(2)}
\]  

(11)

With vectors $\hat{H}_j^{(1)}$ and $\hat{H}_j^{(2)}$ the SER algorithm for low-linearity ramp signals, [5], can be directly used to accurately characterize the INL of the ADC under test. The code-width of the ADC is defined as:

\[
cw_i = \frac{H_i^s}{H_i^{\text{IDEAL}}}, i = 1, 2, 3... N - 2
\]  

(12)

where,

\[
H_i^s = \frac{\hat{H}_i^{(1)} + \hat{H}_i^{(2)}}{2} \\
H_i^{\text{IDEAL}} = \sum_{j=0}^{i} \frac{\hat{H}_j^{(2)} - \hat{H}_j^{(1)}}{\hat{\alpha}}
\]  

(13)

where $\hat{\alpha}$ is the estimated voltage shift given by:
\[ \hat{\alpha} = \frac{N - 2}{\sum_{i=1}^{N-2} \tilde{H}_i^5} \]  

(14)

From the code widths \( c_{wi} \), the INL of the ADC can be calculated using the expressions:

\[
DNL_i = c_{wi} - 1, i = 1, 2, 3...N - 1
\]

\[
INL_i = \sum_{j=1}^{i} DNL_j
\]

(15)

4.6 Kalman Filter for SER/SEIR

SEIR and SER algorithms employ low linearity stimulus to estimate INL \( K \). The errors in estimating INL \( K \), include error due to noise, error due to non-constancy in voltage-shift, \( \alpha \), and error due to input non-linearity. The error due to non-constancy in voltage shift is assumed to be negligible for the resolution of ADC chosen [3]. The error due to noise and nonlinearity is lumped together to give us the measurement equation:

\[
\hat{INL}[k] = INL[k] + \nu[k]
\]

(16)

\( \hat{INL}[k] \) is the INL estimated with KF, \( INL[k] \) is the INL with errors obtained with SEIR or SER algorithm and \( \nu[k] \) is the measurement noise with zero mean and variance \( R \). Comparing (1) and (16) we see that matrix, \( H=[1] \).

The state model chosen is as described in [5]:

\[
\hat{INL}[k] = \hat{INL}[k-1] + DNL[k]
\]

(17)
In the above model the approximation made is that DNL[k] is a Gaussian random variable with zero mean and variance Q. Comparing (1) and (16) we see that matrix, A=[1], B=[0].

In flash ADCs, mismatch among components and comparator offset errors result in nonlinear transfer characteristics. With careful design and layout techniques these errors can be made independent of each other, thus making DNL[k] of the ADC identically distributed and independent. The variance of the process noise is the covariance of DNL[k] and is given by Q. Q along with measurement noise covariance, R, has to be estimated and initialized for the Kalman Filter. R can be estimated by characterizing the test environment. Q can be estimated by measuring the DNL[k] for a couple of ADCs in the batch to be tested [5]. For other segmented architecture ADCs, segments can be identified with independent errors and the above procedure can be followed to model the system for application of Kalman Filter.

4.7 Simulation Results

The low linearity stimulus used for simulations is 7-bit linear, generated from simulations of signal generator circuit suggested in [7]. The second ramp is shifted from the first ramp by 150 LSBs. Transition levels of a 14-bit ADC are characterized using a resistor string representation. The ADC is randomly generated. The INL of the ADCs tested to be 0.5LSB to 14LSB. Input additive noise of 0.5 LSBs is included to simulate ADC’s device noise. The Kalman Filter is initialized as described after (3). R is set to $(0.7\text{LSB})^2(0.7 \text{LSB}) = 1.83\text{e-9}$. Q is set to $(0.125\text{LSB})^2(0.125\text{LSB}) = 5.8\text{e-11}$. 
The simulations have been carried out for standard deviation of additive input noise, $\sigma_{\text{noise}}$, and different number of samples per code, $N_s$. 24 sinusoidal basis functions are used to characterize the non-linearity of the stimulus with SEIR. Algorithms, SEIR, SEIR+KF are run on randomly generated 1000 ADCs. The mean and the standard deviation of the maximum estimation error are recorded. The same procedure is repeated for SER and SER+KF.

Figure 4.1: INL estimation with and without Kalman Filter
Figure 4.1 shows a plot of the true INL[k] of the ADC with those estimated using SEIR, and the proposed algorithm, SEIR-KF. The INL[k]s are estimated with Ns = 8 samples per code for an input noise and a $\sigma_{\text{NOISE}} = 0.5$ LSB. The first plot shows true INL[k] along with those obtained with SEIR and SEIR-KF. The second plot is a zoomed in version of the first plot over a few bins. In the Error plot the improvement in the estimation error for the SEIR-KF is evident. Similar trends can be observed in plots of SER and SER-KF algorithms.

Table 4.1: Mean of Maximum INL estimation Error, NS=8

<table>
<thead>
<tr>
<th>$\sigma_{\text{NOISE}}$</th>
<th>0.25</th>
<th>0.5</th>
<th>1</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>SEIR</td>
<td>0.4916</td>
<td>0.709</td>
<td>1.042</td>
<td>1.59</td>
</tr>
<tr>
<td>SEIR+KF</td>
<td>0.3621</td>
<td>0.477</td>
<td>0.698</td>
<td>1.113</td>
</tr>
<tr>
<td>SER</td>
<td>0.4955</td>
<td>0.714</td>
<td>1.055</td>
<td>1.622</td>
</tr>
<tr>
<td>SER+KF</td>
<td>0.3637</td>
<td>0.495</td>
<td>0.768</td>
<td>1.147</td>
</tr>
</tbody>
</table>

Table 4.2: Mean of Maximum INL estimation Error, NS=4

<table>
<thead>
<tr>
<th>$\sigma_{\text{NOISE}}$</th>
<th>0.25</th>
<th>0.5</th>
<th>1</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>SEIR</td>
<td>0.691</td>
<td>0.991</td>
<td>1.487</td>
<td>2.228</td>
</tr>
<tr>
<td>SEIR+KF</td>
<td>0.4649</td>
<td>0.627</td>
<td>0.923</td>
<td>1.504</td>
</tr>
<tr>
<td>SER</td>
<td>0.696</td>
<td>1.055</td>
<td>1.505</td>
<td>2.322</td>
</tr>
<tr>
<td>SER+KF</td>
<td>0.4645</td>
<td>0.626</td>
<td>0.967</td>
<td>1.604</td>
</tr>
</tbody>
</table>
Table 4.3: Mean of Maximum INL estimation Error, NS=2

<table>
<thead>
<tr>
<th>σ_{NOISE}</th>
<th>0.25</th>
<th>0.5</th>
<th>1</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>SEIR</td>
<td>0.9634</td>
<td>1.397</td>
<td>2.088</td>
<td>3.229</td>
</tr>
<tr>
<td>SEIR+KF</td>
<td>0.5945</td>
<td>0.81</td>
<td>1.247</td>
<td>2.133</td>
</tr>
<tr>
<td>SER</td>
<td>0.9725</td>
<td>1.411</td>
<td>2.1231</td>
<td>3.288</td>
</tr>
<tr>
<td>SER+KF</td>
<td>0.6078</td>
<td>0.828</td>
<td>1.2616</td>
<td>2.06</td>
</tr>
</tbody>
</table>

Table 4.4: Mean of Maximum INL estimation Error, NS=1

<table>
<thead>
<tr>
<th>σ_{NOISE}</th>
<th>0.25</th>
<th>0.5</th>
<th>1</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>SEIR</td>
<td>1.39</td>
<td>1.95</td>
<td>2.93</td>
<td>4.49</td>
</tr>
<tr>
<td>SEIR+KF</td>
<td>0.879</td>
<td>1.07</td>
<td>1.652</td>
<td>2.75</td>
</tr>
<tr>
<td>SER</td>
<td>1.426</td>
<td>1.99</td>
<td>3.011</td>
<td>4.608</td>
</tr>
<tr>
<td>SER+KF</td>
<td>0.919</td>
<td>1.12</td>
<td>1.782</td>
<td>3.042</td>
</tr>
</tbody>
</table>

Table 4.1-4.4 summarizes the results of the simulations carried out in MATLAB. From the table it can be concluded that using a Kalman filter improves the performance by at least 0.13 LSB (For NS=8, σ_{NOISE} = 0.25 LSB with SEIR-KF). For the case of σ_{NOISE} = 2 LSB and NS=1 sample per code, the improvement in the performance is as high as 1.7 LSBs (With SEIR-KF).

The maximum error in INL estimation that is acceptable during testing is often dictated by the target application of the ADC. For example, consider a case where the maximum acceptable estimation error is 1 LSB and the noise in the tester setup has a standard deviation of around 0.5 LSB. From the table, the SEIR algorithm and SER algorithm would require at least NS=4 to achieve the level of performance. With the proposed
approach, Ns=1 can be used to achieve the same level of accuracy that SEIR algorithm or SER algorithm achieves with Ns=4. The trade-off here is a slight increase in computational complexity. But this is negligible given the computation power of today’s PCs. Thus the data acquisition time and hence the test time is scaled by 4. This method also employs a low linearity stimulus, thus obviating the need for a spectrally pure or a highly linear stimulus.

4.8 Conclusion

Optimizing static performance testing by using Kalman Filter with two low-linearity stimulus based linearity testing algorithms has been discussed. A simple model for linearity testing of ADCs with low linearity stimulus and Kalman Filter has been developed. By employing the SEIR algorithm and SER algorithm with a Kalman Filter it has been shown that test cost can be reduced by reducing both test time and hardware resources.

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CHAPTER 5

SIGNAL GENERATORS FOR COST EFFECTIVE BIST OF ADCS

Extended version of the paper published in IEEE European Conference on Circuit Theory and Design-2009

Bharath K Vasan, Jingbo Duan, Chen Zhao, Randall Geiger and Degang Chen

Abstract

Conventional approach to linearity testing of ADCs requires a signal generator that is more linear than the device under test (DUT). Recently introduced ADC testing algorithms dramatically relax the linearity requirements on the signal generator in exchange for maintaining a known functional relationship between two unknown nonlinear test signals. Signal generators that can be used to generate the two non-linear signals are discussed from a Built-in-Self-Test (BIST) perspective. A simple voltage shift is used as the functional relationship between the two non-linear signals. A conservative analysis of the constancy of the voltage shift predicts that the generated signals can be used to test ADCs with resolution ranging between 11 and 16 bits.

5.1 Introduction

Traditional quasi static linearity testing of analog to digital converters (ADC) requires signals that are 3 to 4 bits more linear than the ADC under test. The challenge of generating highly linear or spectrally pure stimulus signals with a very small die area
is one of the biggest challenges in developing practical methods for Built in Self-Test (BIST) of ADCs[1]-[2]. For this reason, quasi static linearity BIST of even a 12-bit ADC is almost never attempted in commercial products. Recently, methods for high-resolution ADC testing have been introduced [3] – [5] that dramatically relax the linearity requirements of the test signal generators. Measured results have been presented [3] that make use of stimuli that are only 7-bit linear to test 16-bit ADCs and simulation results indicate that even lower levels of linearity could be used. In this work, two imprecise nonlinear but functionally related excitations (FRE) were applied to the ADC under test to obtain two sets of correlated output data. From these two sets of data, the linearity of the device under test (DUT) can be accurately extracted. The dramatic reduction in linearity requirements of the signal generator offers potential for overcoming one of the major challenges in practically implementing BIST for high-performance ADCs. Specific requirements on the functional relationship between the two nonlinear excitations must be met to use this approach for testing. One functional relationship that can be used is a constant shift. Practically, two low linearity ramps, the second being shifted by a small voltage from the first, can serve as the two FRE test signals. With this approach, the requirement on the linearity of the stimulus is replaced with the requirement of constancy of the shift between the two signals. A constant shift can be viewed as generating the second signal by adding a small offset to the first. This paper focuses on the design of signal generators that can add a small but constant offset voltage to a given signal. The constancy requirements for different ADC resolution requirements are discussed in section 5.2. Simple and practical signal generators that can
be used for BIST of ADCs are presented in section 5.3. Different methods of adding the voltage offset are considered in section 5.4, simulation results in section 5.5. The paper is concluded in section 5.6.

5.2 Constancy Requirement

Shift-based non-linear FRE testing offers trade-offs between linearity in the test signal generator and constancy of the voltage-shift [3]-[5]. The voltage-shift constancy requirement is strongly dependent upon the specific characteristics of the FRE testing algorithm.

The following notations will be used for the ADC under test in this chapter:

\( n \): Resolution of the ADC under test, ADC Input range: \((0, 1)\)

\( N \): \(2^n\), number of distinct output codes

\( T_k \): \(k^{th}\) transition level between code \(k-1\) and \(k\) of the ADC

\( t_k \): Cumulative histogram count associated with \(T_k\) where

\[
t_k = \frac{\sum_{i=0}^{k-1} H_i}{N_s}, k = 1, 2, 3...N - 1
\]

\( H_i \): Total number of samples received in code \(i\),

\( i = 0, 1, 2...N-1 \)

\( N_s \): Total number of samples

The identification error, \(e_{T_k}\), in the \(k^{th}\) transition level, \(T_k\), is given by[4]:

\[
e_{T_k} = -\frac{1}{\alpha} \int_{0}^{T_k} N(t)dt
\]
where, \( \hat{I}_k \) is the estimated cumulative histogram count with non-constant voltage shift, \( \alpha \) is the constant part of the voltage-shift, \( N(t) \) is the non-constant part of the voltage-shift.

The resultant INL estimation error, \( e_{INL_k} \), is then given by:

\[
e_{INL_k} = e_{iT} \cdot \frac{N - 2}{T_{N-2} - T_0}
\]

(3)

The maximum INL estimation error is then given by:

\[
\max |e_{INL_k}| = \frac{2^n - 2}{\alpha} \cdot \max \left| \int_{0}^{\tau} N(\tau) d\tau \right|
\]

(4)

The maximum error can be estimated using the above expression only if the shape of the non-constant part of the voltage-shift, \( N(t) \) is known. Typically 1\(^{st}\) order and 2\(^{nd}\) order functions of the integral of \( N(t) \) can be used to estimate the maximum error. Consider the following two cases:

Case 1: \( N(\tau) = \Delta_1 \)

where, \( \Delta_1 \) results in a linear non-constant part for the voltage-shift.

The maximum INL estimation error is then given by evaluating (4):

\[
\max |e_{INL_k}| \leq \frac{2^n - 2}{\alpha} \cdot \frac{\Delta_1}{2}
\]

(5)

Case 2: \( N(\tau) = \Delta_2 (\tau - 0.5) \)

where, \( \Delta_2 \) results in a second order non-constant part for the voltage-shift.

The maximum INL estimation error is then given by evaluating (4):

\[
\max |e_{INL_k}| \leq \frac{2^n - 2}{\alpha} \cdot \frac{\Delta_2}{4}
\]

(6)
(6) gives the most stringent estimate for the constancy of the voltage shift. The maximum INL estimation error is then bound by 0.25LSB if the following condition is satisfied:

\[
\frac{\Delta_1}{\alpha} < \frac{1}{2^{n-19}} \text{ (ppm)}
\]  

(7)

With Case 2 the condition becomes:

\[
\frac{\Delta_2}{\alpha} < \frac{1}{2^{n-20}} \text{ (ppm)}
\]  

(8)

where \(\alpha\) is the nominal value of the voltage shift (offset voltage), \(n\) is the resolution of the ADC under test and \(\Delta\) is the maximum change in the shift over the full scale input range. From (7) and (8) it can be observed that for a 16-bit ADC the constancy has to be smaller than 8 ppm when \(N(t)\) is a 1st order function, and 16 ppm when \(N(t)\) has parabola shape. (7) is more stringent than the one used in the original paper. This estimate has been used to predict the INL estimation error. Note that this expression is not dependent upon the linearity of the excitation. Although not stated here, there are some readily satisfied restrictions on the high spatial frequency content of the excitation [3].

![Figure 5.1 Ramp generation- charging/discharging capacitor](image_url)
With this approach, the requirement on the linearity of stimulus signals is completely replaced by a requirement on the constancy of the voltage shift. Practically, $\alpha$ is typically around 0.1% to 1% of the full scale range [3].

5.3 Simple Ramp Generator Circuits

Simple circuits like the one shown below can be used to generate a ramp-like signal. The PMOS transistor P1 acts as a current source. Switches s1 and s0 are used to initiate the charge and discharge of the capacitor C. For BIST implementation, the capacitor area must be small. The output is termed “ramp-like” because the non-ideal transistor P1 and the nonlinear part of the capacitor C will introduce modest nonlinearities that cause the output to differ from an ideal ramp output. This ramp-like signal can be used as one of the two inputs for a shift-based FRE testing strategy.

A standard analog summing circuit can be used to introduce a shift in the ramp-like signal by adding a small dc voltage to the ramp-like signal.

![Figure 5.2 Simple Ramp Generator Circuit](image)
Figure 5.3 Offset in an Inverting Amplifier

The circuit of Figure 5.2 shows one such op-amp based summing circuit. The shift can be added by either closing switch s2 or by closing switch s3. If the gain of the op-amp is sufficiently high, this circuit will provide a constant dc offset but if the op amp gain is not sufficiently high, nonlinearities in the operational amplifier will introduce small nonlinearities in the shift. It is well-known that the offset voltage of an operational amplifier invariably introduces an undesirable shift in the output voltage of most op-amp based circuits. If the offset voltage of an operational amplifier can be controlled by a switch, however, the offset voltage change from when the switch is open to when the switch is closed will provide two signals that are ideally different by a constant shift. The circuit diagram for such a ramp generator is as shown in Figure 5.2 where switch s3 is used to intentionally introduce mismatch internal to the operational amplifier. The offset voltage in an operational amplifier is comprised of two parts, the systematic part and the random part. The random part, caused by random mismatches and process variations, is not of concern to us. This is because it would be common to both ramp-like signals. Likewise, the systematic part which is common to both ramp-like signals is not
of concern either. The difference in the systematic part, which is under the designer’s control, can be changed to introduce the desired offset (shift) in the output voltage. The input-referred offset voltage for the ramp-like signal generator of Figure 5.2 is shown explicitly in Figure 5.3 where it has been assumed that a constant voltage source VOS can be used to model the offset effects. If we define \( V_{OS1} \) and \( V_{OS2} \) to be the offset voltages before and after \( s3 \) is closed respectively, and assume \( A_{OL} \) is not affected by \( s3 \), it follows that the difference in the two ramp-like signals is given by the expression.

\[
V_D = (V_{OS2} - V_{OS1}) \frac{1 + \frac{R_F}{R_1}}{1 + (1 + \frac{R_F}{R_1}) \frac{1}{A_{OL}}} \\
\approx (V_{OS2} - V_{OS1})(1 + \frac{R_F}{R_1}) \quad A_{OL} \to \infty
\]  

(9)

If \( A_{OL} \) is affected by \( s3 \) or if \( A_{OL} \) is nonlinear, the shift predicted by (3) is not valid. These concerns are germane in this BIST application because of the requirements given in (7) that the shift be really constant for testing high resolution ADCs.

5.4 Internal Introduction of Voltage Shift

Figures 5.4, 5.5 show two conventional two-stage amplifiers. They are named BUF1 and BUF2 respectively. BUF1 has a standard five transistor first stage followed by a common source second stage. BUF2 in Figure 5.5 has a higher dc gain and uses a cascode amplifier for the first stage and a common source amplifier for the second stage. Any mismatch in a nominally symmetric circuit will introduce offset. The switches \( \phi1-\)
\( \phi_3 \) and \( \Theta_1-\Theta_6 \) shown in the amplifiers of Figure 5.4 and 5.5 introduce offset in different ways in the first stage of the amplifiers.

Figure 5.4 BUF1, Five-Transistor First Stage

Figure 5.5 BUF2- Telescopic-Cascode First Stage
One is generated with all switches open and the second with exactly one switch closed. For example, closing switch \( \phi_1 \) introduces a bias current mismatch between the left and right sides of the circuit, closing switch \( \phi_2 \) introduces a mismatch in the PMOS loads, and closing switch \( \phi_3 \) causes an effective mismatch in the differential input pair. Correspondingly, in the amplifier of Figure 5.5, \( \Theta_1 \)–\( \Theta_4 \) introduce bias current mismatch. For notational convenience, cascode current sources are depicted as ideal current sources in this figure. \( \Theta_5 \) introduces a mismatch in the differential input pair and \( \Theta_6 \) changes the bulk voltage of M6 thus causing a mismatch in the PMOS loads.

### 5.5 Simulation Results

All amplifiers have been designed in the 0.18\( \mu \) CMOS process with a supply of 1.8V. The ramp-like input is 1V full scale. The shift values that are used are in the range from 1mV to 4mV. The resistors in the feedback amplifier are 1M\( \Omega \). All switches are single n-channel transistors with a switch control voltage of 3.3V. In the results tables shown, a ‘1’ indicates which switch is closed. The maximum deviation in the shift over the full scale input range was simulated and expression (7) was used to obtain the equivalent number of bits (NOB), \( n_{EQ} \), of an ADC that can be tested with this signal generator. Since in this BIST application, the ramp-like shift generators are used for quasi static testing of ADCs, the speed of the operational amplifier is of little concern. Hence the Gain Bandwidth product requirements on the two stage op-amp can be relaxed. Table 5.1 summarizes the DC gain, Gain Bandwidth and Power dissipation of each of the amplifiers. It can be observed that changing the source of internal offset and
changing the amplifier gain plays a big role on the constancy of the shift with ADC BIST capability ranging from under 6 bits to in excess of 16 bits with these amplifiers.

Table 5.1: Amplifier Key Specifications

<table>
<thead>
<tr>
<th></th>
<th>DC Gain(dB)</th>
<th>GBW(MHz)</th>
<th>Power(mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>BUF1</td>
<td>87</td>
<td>40</td>
<td>0.18</td>
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<tr>
<td>BUF2</td>
<td>116</td>
<td>36</td>
<td>0.27</td>
</tr>
</tbody>
</table>

Table 5.2: BUF1-Simulation Results- Equivalent NOB, $n_{EQ}$, estimation

<table>
<thead>
<tr>
<th>φ1</th>
<th>φ2</th>
<th>φ3</th>
<th>α(mV)</th>
<th>$n_{EQ}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>3.8</td>
<td>11.5</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>3.5</td>
<td>14.4</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>3.4</td>
<td>15.1</td>
</tr>
</tbody>
</table>

Table 5.3: BUF2-Simulation Results- Equivalent NOB, $n_{EQ}$, estimation

<table>
<thead>
<tr>
<th>θ1</th>
<th>θ2</th>
<th>θ3</th>
<th>θ4</th>
<th>θ5</th>
<th>θ6</th>
<th>α(mV)</th>
<th>$n_{EQ}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<td>13.8</td>
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<td>0</td>
<td>0</td>
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Comparing the results in Table 5.3 with those in Table 5.2, it can be observed that significant improvements in the linearity of the shift can be attained through a more optimal choice of biasing voltages and power dissipation. Most importantly, it can be
concluded from these tables that practical signal generators can be designed that are useful for BIST of ADCs with resolution ranging from 6 bits to nearly 18 bits using the FRE approach with the shift relationship.

5.6 Conclusion

Simple signal generator circuits that can be used for practical BIST of ADCs using the shift operator in the FRE approach to testing have been introduced. Simulation results indicate that these signal generators can be used for linearity testing of ADC whose resolution range from 11 bits to 16 bits.

References


CHAPTER 6
MEASUREMENT INTERFACE SOLUTIONS FOR SOFT ELASTOMERIC CAPACITORS IN STRUCTURAL HEALTH MONITORING APPLICATIONS

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Huanhuan Zhang, Bharath K Vasan, Yulong Shi, Simon Laflamme, Hussam Saleem,
Randall Geiger and Degang Chen

Abstract
This work discusses a novel sensor network for strain sensing over large surfaces for Structural Health Monitoring (SHM). The sensor network consists of an array of Soft Elastomeric Capacitors (SEC). Each SEC behaves as a surface strain gauge, responding with a change in its capacitance to a local strain stimulus. Requirements for low-cost, measurement interfaces are discussed. Continuous-time and discrete-time based measurement circuit prototypes are presented. Experimental results show that the proposed solution can be easily programmed to measure strain as small as $14.6 \mu\varepsilon$.

6.1 Introduction
Structural health monitoring (SHM) of large-scale systems, including civil, mechanical, and aeronautic structures (Eg. wind turbines, bridges, aircraft), has substantial potential for both a large societal and economic impact. For instance, SHM of wind turbine blade could dramatically reduce cost associated with operation and
maintenance of blades, consequently reducing cost associated with energy production [1-2]. Correspondingly, SHM of bridges, buildings, and aircraft could be used to dramatically reduce the risk of failure of these structures that could result in a catastrophic event. However, SHM solutions are not broadly implemented. This is due to the general complexity of the SHM task, where existing solutions are either technically too complex to implement at large scale, or are economically difficult to justify [3-5]. To realize the full potential of SHM methods, it is fundamental to develop cost-effective sensing solutions, capable of direct damage diagnosis, localization, and prognosis [6, 7].

As a possible solution, the authors have proposed a bio-inspired sensory membrane, constituted by an array of soft elastomeric capacitors (SEC) [8]. The SECs are fabricated from a SEBS polymer matrix, doped with titanium dioxide (TiO2) to enhance the permittivity of the material. The nanomaterial mix is sandwiched between compliant electrodes, fabricated using a similar mix with added carbon black. The sensory membrane is an inexpensive sensing solution, mechanically robust, chemically and environmentally stable, easy to apply, and leads to direct signal processing by directly measuring strain. The proposed sensing material has shown great promise at tracking strain and detecting cracks on wood and concrete specimens [8-10]. In order to attain broad implementation of the sensing solution, it is fundamental to pair the sensing materials with an inexpensive data acquisition system.

Soft elastomeric sensors have previously been proposed for SHM of civil structures [11], [12], [13], [14]. Popular applications include carbon nanotubes within
the elastomeric substrate to create resistance-based strain sensors [15], [16]. Capacitance-based film-type sensors have also been proposed, which include applications to humidity [17], [18], pressure [19], strain [20], [21], and tri-axial force [22] measurements. The proposed SEC differs from literature by combining both a large physical size and high initial capacitance, resulting in a larger surface coverage and higher sensitivity. The SEC constitutes a promising candidate for strain sensing over large surfaces.

Compared with other existing sensing solutions, the proposed sensor is an alternative to fiber optics. With both fiber optic sensors and the SEC technology, strain data can be measured over large systems. The SEC network offers the advantages of being 1) cost-effective; 2) operable at low frequencies; 3) mechanically and environmentally robust; 4) low-powered; 5) easy to install onto surfaces; and 6) customizable in shapes and sizes.

The performance of the SEC sensor is strongly dependent upon the performance of electronic circuits that provide a read-out of the sensor array. With strain information being encoded in very small changes in capacitance, a readout circuit that accurately provides an output signal dependent upon the small capacitance changes is required. With the requirement for very accurately and rapidly making a large number of very small capacitor difference measurements with minimally intrusive electronics in the presence of large parasitics and environmental noise, a dedicated integrated circuit solution is required. There has been considerable work reported on the electronics required for differential capacitive sensors that can accurately measure very small
capacitance differences since there are a large number of transducers that encode the sensing information in capacitor differences [25-28]. Much of this work, has focused on the difference of two capacitors rather than on the "neighbor-capacitor" difference of a large capacitor array. Very few of the works in the past have focused on applications where the total change in capacitance is a very small fraction of the nominal capacitances [29]. In this work, architectural solutions for conducting measurements of the SEC sensor are presented. This method will result in inexpensive sensing hardware, and can lead to substantial improvement in existing SHM methods. The chapter is organized as follows. Section 6.2 discusses the composition of Soft Elastomeric Capacitors (SEC). Section 6.3 discusses the sensitivity of a typical SEC and requirements of a system to measure very small changes in capacitance due to strain. In section 6.4 two systems to convert changes in capacitance to digital data are discussed. In section 6.5 experimental results are presented. In section 6.6 conclusions are drawn.

### 6.2 Soft Elastomeric Capacitors

The sensor used for constituting the flexible strain gauge network consists of a soft elastomeric capacitor (SEC). The resulting sensor consisted of a robust elastomeric film fabricated from an inexpensive nanoparticle mix. It is capable of covering large areas. Specifically, the dielectric of the capacitor is fabricated from a thermoplastic elastomer matrix, poly-styrene-co-ethylene-co-butylene-co-styrene (SEBS), doped with titanium dioxide (TiO2) to increase the materials permittivity and robustness with respect to mechanical tampering. The compliant electrodes are fabricated with the same
SEBS mixed with carbon black (CB) particles. Figure 6.1 shows the picture of a single SEC. The process is initiated by the fabrication of a SEBS/toluene solution. Part of this solution is used to create the nanoparticle mix, in which TiO2 particles are added and dispersed using an ultrasonic tip. The resulting mix is drop-casted on a glass slide, and dried over 5 days to allow complete evaporation of the solvent. Meanwhile, the remaining SEBS/toluene solution is used to create the compliant electrodes. Here, CB particles are added instead of TiO2 to create a conductive mix. Finally, the CB mix is sprayed or painted on both surfaces of the dried polymer. The surface to be monitored is sanded, painted with a primer and a thin layer of epoxy is applied on which sensors are adhered.

Figure 6.1 Soft-Elastomeric-Capacitor (SEC)

Figure 6.2 SEC on a surface to be monitored
6.3 Electro-Mechanical Model of the SEC

The nominal value of the capacitance of the SEC can be obtained using the plate capacitance equation:

$$C = \varepsilon_0\varepsilon_r \frac{A}{h}$$  \hspace{1cm} (1)

where $C$ is the capacitance, $\varepsilon_0$ is the vacuum permittivity, $\varepsilon_r$ is the permittivity of polymer and $d$ is the thickness. $A = w \times l$ is the sensor’s area. $w$, $l$ and $h$ are the width, length and the thickness of the sensor respectively.

The strain is unidirectional along the length of the sensor as the sensor is glued to the surface. The Poisson ratio of pure SEBS materials has been reported to be 0.49 [23]. The elastomer can be assumed to be incompressible, where the volume stays constant.
with the strain. Let $\Delta l$ be the change in the length due to the applied strain. The new capacitance value can then be shown to be:

$$C_{\text{new}} \approx \frac{\varepsilon_0 \varepsilon_r A}{h} \left(1 + 2 \frac{\Delta l}{l} \right)$$  

(2)

The change in capacitance is given by:

$$\Delta C = C_{\text{new}} - C = \frac{\varepsilon_0 \varepsilon_r A}{h} \left(2 \varepsilon \right)$$  

(3)

where, $\varepsilon$ is the applied strain given by

$$\varepsilon = \frac{\Delta l}{l}$$  

(4)

The gauge factor (GF), defined as the ratio of normalized change in capacitance to the applied strain, is given by:

$$GF = \frac{\Delta C / C}{\varepsilon} = 2$$  

(5)

The sensitivity of the sensor is given by:

$$\frac{\Delta C}{\Delta l} = 2 \frac{\varepsilon_0 \varepsilon_r w}{h}$$  

(6)

The equation allows programming of the sensitivity. For the SEC shown in Figure 6.1, $C=700\text{pF}$, $w=l=70\text{mm}$, $h=0.3\text{mm}$ giving a sensitivity of $20\text{pF/mm}$.

One of the standard resistive strain gauges systems is the Vishay MicroMeasurement, CEA-06-500UW-120. It can measure strain as small as $1\mu\varepsilon$. For SHM, detecting a strain of less than $20 \mu\varepsilon$ is targeted with SEC interface and data acquisition system. This corresponds to a $40\text{ppm}$ change in the nominal value of the capacitance.
(5). To measure a strain of 1με, 2ppm changes have to be detected by acquisition system.

6.4 Proposed low-cost interfaces and data acquisition solution for SEC

As shown in section 6.3, a sensor interface has to be high precision to estimate response of the SEC due to strain. This imposes the following requirements on the measurement circuitry:

1. High Resolution > 15-bit resolution on ΔC relative to nominal SEC capacitance
2. High Immunity to noise and parasitic capacitances
3. Track slow varying changes in baseline/nominal capacitance with temperature and humidity
4. Moderate data capture rate (one sample per ms for each SEC)

It can be shown that the capacitance or more specifically the capacitance change of the SEC patch is determined by several factors. These factors jointly contribute to the actual value of the capacitance. The following model of the SEC separates the effects of these different factors:

\[ C_T = C_N + C_R + C_P + C_E + C_S \]  \hspace{1cm} (7)

where, \( C_T \): total capacitance, \( C_N \): nominal capacitance, \( C_R \): random capacitance, \( C_P \): parasitic capacitance, \( C_S \): capacitance change due to stress, \( C_E \): capacitance change due to environmental effects like temperature, pressure, humidity, etc. \( C_N \) is given by (1) where all parameters in this equation are the nominal or design values. Process variations during the manufacturing process results in \( C_R \). In the manufacturing process
used for the development of prototype SECs, the random value is a random variable with a standard deviation of around 10% of $C_N$. Parasitic capacitances between the capacitance electrodes and other conductors in the set-up constitute $C_P$. This component could be as high as 10% of $C_N$ and is strongly dependent upon how the SEC is mounted and connected to the sensing device and the instrumentation circuitry. Environmental effects like temperature, humidity, etc. which are assumed to be slowly varying constitute $C_E$. $C_E$ could be as large as $C_P$. $C_S$, the component to be measured, is due to the strain on the SEC sensor. As described in section 6.3, the change in the capacitance due to strain stimulus is small and can be much less than other components in (6). The magnitude and required measurement resolution of $C_S$ is strongly application dependent. To measure $C_S$ accurately, the unwanted components must be calibrated out.

6.4.1 Continuous time (CT) Measurement circuit

The block diagram of the proposed continuous time measurement circuit in its simplest form is as shown in Figure 6.4. This is actually a bridge network with the NULL-ADJUST block completing the bridge. The lower part of the bridge can be viewed as a first order RC filter. The filter is driven by a sine wave. The frequency of the sine wave should be under 2 kHz for high sensitivity of the SEC [24]. The excitation frequency is set to approximately the pole frequency of the filter to achieve a rather large change in the RMS voltage at the output of the filter with changes strain.
The output of the RC filter, $V_{\text{SIG}}$, is one of the inputs to a programmable gain amplifier (PGA). The $V_{\text{CANC}}$ signal from the NULL-ADJUST block serves as the other input to the amplifier. The PGA must have high common mode signal rejection and should be able to be programmed for gains of 10000 or larger. An Analog-to-Digital Converter (ADC) samples the output of the amplifier and converts it to a digital output. The ADC must have sufficient resolution and dynamic range. The measurement method consists of two operations, a NULL operation and a MEASURE operation. The NULL operation essentially balances the bridge prior to making a measurement.

**NULL operation**

The filter’s pole is a function of the resistance $R$ and the capacitance of the SEC at a reference time instant $t_0$, designated as $C_1(t_0)$. It is assumed that the NULL operation
is carried out at time when there is no-strain or when a bias strain is present. This can be modeled as

$$C_{1,0} = C_X + C_{1,S}(t_0)$$

(8)

where

$$C_X = C_N + C_R + C_P + C_E$$

(9)

and where $C_{1,S}(t_0)$ is the bias strain which could be 0. A $V_{CANC}$ sine wave signal is generated using the NULL-ADJUST block to cancel the signal, $V_{SIG}$, that appears at the output of the filter. The NULL-ADJUST block consists of a Digital to Resistance Converter (DRC) and a Digital to Capacitance Converter (DCC) to adjust the amplitude and phase of $V_{CANC}$ signal to match the amplitude and phase of $V_{SIG}$. The digital codes, termed CALCODES, of the DRC and DCC contain information regarding $C_X$ and $C_{1,S}(t_0)$. The CALCODES corresponding to the SEC are stored in a register. A frequency domain representation of the phasor $V_{SIG}(j\omega)$ corresponding to the voltage $V_{SIG}$ is given by the expression:

$$V_{SIG}(j\omega) = T_0(j\omega) V_{IN}(j\omega)$$

(10)

where $T_0(j\omega)$ is the transfer function of the first-order RC filter prior to the application of the stress that is to be measured and $V_{IN}(j\omega)$ is the input voltage phasor. It follows from a basic circuit analysis that $T_0(j\omega)$ can be expressed as:

$$T_0(j\omega) = \frac{1}{1 + j\omega RC_X (1 + \frac{C_{1,S}(t_0)}{C_X})}$$

(11)
At the end of the NULL operation there will be a residual imbalance in the bridge which can be modeled as:

\[ V_{\text{CANC}} = V_{\text{SIG},N} + \varepsilon_{\text{RES}} \]  \hspace{1cm} (12)

where ‘\( \varepsilon_{\text{RES}} \)’ is the residue in the NULL operation. After calibration, we have the CALCODES: DRC and DDC.

**MEASURE operation**

CALCODES corresponding to the SEC determined during the NULL adjustment are loaded into the NULL-ADJUST block. \( V_{\text{CANC}} \) is now given by (12). When a strain or change in strain occurs, the capacitance changes from the value obtained at NULL to \( C_1(t_1) \) due to the strain present at time, \( t=t_1 \). It is assumed that \( C_X \) component of the capacitor remains constant, and the only change is due to the change in stress. Thus,

\[ C_1(t_1) = C_X + C_{1,s}(t_1) \]  \hspace{1cm} (13)

\( V_{\text{SIG}}(j\omega) \) signal changes to:

\[ V_{\text{SIG}}(j\omega) = T_i(j\omega) \cdot V_{\text{IN}}(j\omega) \]  \hspace{1cm} (14)

where

\[ T_i(j\omega) = \frac{1}{1 + j\omega R_C X (1 + \frac{C_{1,s}(t_1)}{C_X})} \]  \hspace{1cm} (15)

The output of the amplifier with gain, \( K \), is given by:

\[ V_{\text{out}} = K \cdot (V_{\text{SIG}} - V_{\text{CANC}}) \]  \hspace{1cm} (16)
The frequency of oscillation is set to $\omega=1/RC_X$. It can be shown that if $\varepsilon_{RES}$ is negligible, the amplitude of $V_{out}$ is approximately:

$$|V_{out}| \approx K|V_{IN}| \frac{1}{\sqrt{2}} \left( \frac{C_{1,S}(t_0) - C_{1,S}(t_1)}{C_X} \right)$$

(17)

It can be observed from (17) that all measured $\Delta C_{1,S}(t)$ are referenced to $C_{1,S}(t_0)$. $C_{1,S}(t_0)$ has to be periodically refreshed (nulled) to compensate for changes in temperature and humidity and to ensure that the ADC does not over range. The refresh rate is decided by the application and by the environment in which the SECs are deployed. The amplitude of the signal from the smallest change in capacitance should be greater than the residue described in (13). If thermal noise from the first order filter is the only contributor to the residue in (13), then to measure 2ppm changes in the 700pF SEC, $V_{IN}$ would be required to be greater than 2V. The acquisition can be designed to achieve this. It should be noted that an input sinusoid signal with high total harmonic distortion (THD) can result in large residues and is highly undesirable.

The implementation of the proposed sensor network consists of an array of adjacently placed SECs connected to a single NULL-ADJUST module. The SECs in the module are sequentially measured in time using the programmable gain amplifier (PGA) and the ADC in the module. The block diagram is shown in Figure 6.5. CALCODES for each SEC are stored in a register during the NULL operation. During the MEASURE operation, the CALCODE for the SEC that is active is loaded. This is followed by data acquisition using the ADC. The next SEC is then switched along with its CALCODES, and the data acquisition is repeated. It is assumed that the multiplexing from one SEC to
another is done at a fast rate, $F_{SW}$. With fast multiplexing, we can generate the following matrix:

$$
[\Delta C] = \begin{bmatrix}
\Delta C_{1,S}(t_1) & \Delta C_{1,S}(t_2) & \cdots & \Delta C_{1,S}(t_n) \\
\Delta C_{2,S}(t_1) & \Delta C_{2,S}(t_2) & \cdots & \Delta C_{2,S}(t_n) \\
\vdots & \vdots & \ddots & \vdots \\
\Delta C_{N,S}(t_1) & \Delta C_{N,S}(t_2) & \cdots & \Delta C_{N,S}(t_n)
\end{bmatrix}
$$

(18)

If the NULL operation is performed under no-strain conditions (no bias strain) for the N-SECs then:

$$
C_{i,S}(t_0) = 0 \quad i = 1, 2, \ldots N
$$

(19)

With the condition in (19), from the matrix in (17) we can extract not only the temporal capacitance change information (column wise subtraction), we can also extract spatial capacitance difference (row wise subtraction).

Typical requirements in implementing such a system are listed below:

1. Programmable signal generator with high spectral purity and programmable frequency for ADC clock synchronization
2. Sufficient resolution (depends on desired dynamic range) in NULL-ADJUST block and fast tuning algorithm implementation
3. Programmable Gain amplifier with high gain option, excellent linearity and common mode suppression
4. ADC with true static and dynamic 15/19 bit performance up-to 50kHz
5. Fast Multiplexers with excellent matching and linearity
6.4.2 Discrete time (DT) Measurement circuit

A circuit schematic of a stray-insensitive circuit that provides an output voltage proportional to the difference of two adjacent capacitors $C_1$ and $C_2$ is shown in Figure 6.6, where $V_{IN}$ is a constant DC and where $\phi_1$ and $\phi_2$ are complimentary non-overlapping clocks. The measurement method once again consists of two operations, a NULL operation and a MEASURE operation. In the NULL operation, appropriate
calibration ensures that the output is zero or very little residue similar to (13). In the Measure operation, the change in voltage due to the change in capacitance appears at the output. The output during phase $\phi_2$ is given by:

$$V_{OUT} = \frac{\Delta C}{C_F} * V_{IN} * (1 + \frac{R_F}{R_{IN}})$$

(20)

where, $\Delta C = C_2 - C_1$. The clock speed has to be less than 2 kHz for high sensitivity [24]. $V_{IN}$ can be chosen based on the desired signal to noise ratio as described in section 6.4.1. The desired gain can be set using $C_F$ and feedback amplifier’s gain. Care has to be taken in choosing switch sizes, especially the switch around $C_F$, to reduce errors due charge injection.

Figure 6.6 Implementation of the DT Measurement Circuit
6.5 Experimental Results

6.5.1 Continuous time (DT) Measurement circuit

To demonstrate the applicability of the method, a test circuit based upon the offset null structure of Fig 6.4 was constructed to test the SEC under controllable strain. The offset null was implemented manually and the output voltage of the amplifier was sampled with an Audio Precision SYS-2722 Audio Analyzer. The SYS-2722 computed the Discrete Fourier Transform (DFT) and the magnitude of the fundamental were used as the output. Since a large number of time-domain samples are taken for computing the DFT, this approach inherently minimizes noise issues associated with both the thermal device noise in the amplifier which is referred to as “kT/C” noise and the interference noise. The test setup is shown in Fig.6.7. On the left is the SEC constrained on both the left and right side. Strain was applied with a bar at the center using the wing nuts to accurately control vertical position. On the right are the scales used to measure the turns of the wing nuts. They are labeled in degrees which correspond to με. In this setup, we have 14.6 με/deg. Test results are shown in Figure 6.8.

Figure 6.7 Test setup for measuring strain
This circuit has an output of approximately 23mV/µε. Although the relationship between angle of the wing nut and the strain is quadratic, it can be shown that the response is linear with small changes in angle of the wing nut. This is observed in the Fig 6.8. Even larger responses can be obtained by increasing the gain of the instrumentation amplifier and by automated zeroing of the bridge amplifier.

### 6.5.2 Discrete time (DT) Measurement circuit

A discrete time prototype of the circuit in Fig.6.6 has been set-up on a breadboard with MAX326 switches and LT1151 operational amplifiers. The non-overlapping clocks are generated using a triangle wave generator and op-amps as comparators as shown in Fig. 6.9. The circuit schematic implemented on the breadboard is shown in Fig.6.10. The frequency of the clocks is set to f=1kHz.
Figure 6.9 Non-overlapping clock generator

Figure 6.10 Discrete Time circuit schematic
The switches are chosen to have low parasitic capacitance to minimize charge injection errors. The operational amplifier, LT1151, is a zero drift amplifier with very low offset voltage. The NULL operation is performed using two inputs $V_{IN1}$ and $V_{IN2}$. In the MEASURE operation, an output that is proportional to the change in capacitance is sampled and amplified by the gain stage (20). The working of the circuit has been verified using capacitance changes as small as 0.5pF. Testing the circuit with the controlled strain with the set-up in 6.7 is underway.

6.6 Conclusion

Structural Health Monitoring using novel Soft Elastomeric Capacitors (SEC) has been discussed. For SHM applications the desired strain values to be measured are low as 20ppm. Novel architectural solutions have been discussed to achieve this performance. Simple, low-cost prototypes have been built to realize an interface for measuring very small changes in strain. The proposed continuous-time measurement circuit can measure strains as low as $14.6 \mu \varepsilon$.

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CHAPTER 7

SUMMARY

In chapter 2 of the dissertation, a novel harmonic programming technique for PSOs has been proposed. The technique involves a simple operation of weighted summation of PSO outputs. The method can be used to generate low THD sine waves and for frequency multiplication or division. The weighted summation can be implemented using active or passive components. The proposed technique can operate over a wide frequency range. A bread board prototype has been constructed to demonstrate generation of -100dB THD sine waves. The proposed method has also been used to demonstrate on-chip low THD sine wave generation. The technique can decrease the burden on filtering to suppress harmonics. BIST of analog circuits will be closer to reality with this technique. Complex System-on-Chip designs with ring oscillators can easily generate low THD sine waves for BIST of other blocks on the SOC.

In chapter 3-4, new algorithms for testing high resolution ADCs with low linearity signals have been proposed. Unlike conventional methods, this method requires very simple signal generators thus offering a cost saving in the hardware resources required for production testing. Optimizing static performance testing by using Kalman Filter with two low-linearity stimulus based linearity testing algorithms has been discussed. A simple model for linearity testing of ADCs with low linearity stimulus and Kalman Filter has been developed. By employing the SEIR algorithm and SER algorithm with a Kalman Filter it has been shown that test cost can be reduced by
reducing both test time and hardware resources. Low-cost signal generators to generate signals for the new algorithms are proposed in chapter 5. Simulation results indicate that these signal generators can be used for linearity testing of ADC whose resolution range from 11 bits to 16 bits. ADCs continue to be one of ICs produced in large volumes. Small saving in test procedures can result in significant savings in the overall test cost.

Cost effective Structural Health Monitoring (SHM) solutions are the key to effective automation of damage assessment in large scale systems. Sensor networks using novel soft elastomeric sensors are a step towards this goal. The SECs respond to a strain stimulus with a change in their capacitance. In chapter 6, sensor interface circuits to measure the change in capacitance of the SEC and to convert them to digital output are proposed. A simple, low-cost prototype has been built to realize an interface for measuring strain as small as 14.6 με.